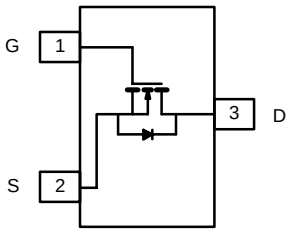
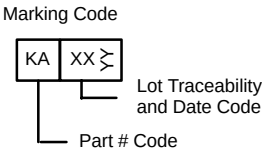
SI1302DL

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.480 @ V_{GS} = 10 V	0.64
	0.700 @ V_{GS} = 4.5 V	0.53

SOT-323
SC-70 (3-LEADS)



Top View



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**5 secs**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	0.64	0.60	A
	T_A = 70°C		0.51	0.48	
Pulsed Drain Current		I_{DM}	1.5		
Continuous Diode Current (Diode Conduction)[a]		I_S	0.26	0.23	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	0.31	0.28	W
	T_A = 70°C		0.20	0.18	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	355	400	°C/W
	Steady State		380	450	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	285	340	

Notes
a. Surface Mounted on 1” x 1” FR4 Board.

SI1302DL

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 70°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	1.5			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 0.6 A		0.410	0.480	Ω
		V_{GS} = 4.5 V, I_D = 0.2 A		0.600	0.700	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 0.6 A		0.75		S
Diode Forward Voltage[a]	V_{SD}	I_S = 0.23 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 0.6 A		0.86	1.4	nC
Gate-Source Charge	Q_{gs}			0.24		
Gate-Drain Charge	Q_{gd}			0.08		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 30 Ω I_D ≅ 0.5 A, V_{GEN} = 10 V, R_G = 6 Ω		5	10	ns
Rise Time	t_r			8	15	
Turn-Off Delay Time	$t_{d(off)}$			8	15	
Fall Time	t_f			7	15	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 0.23 A, di/dt = 100 A/μs		15	30	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.