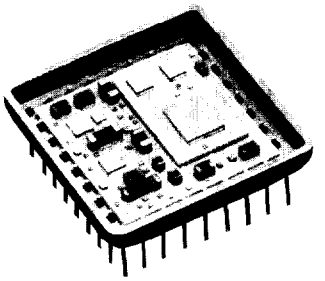
NATEL

One-Inch Square, Single 5 Volt Powered R/D Converter with Reference Oscillator Microprocessor Compatible 16-bit Hybrid

HRD1416

Features

- **Built-In Reference Oscillator**
- **One Inch Square 32 pin Hermetic Package**
- **True Single Supply . . . 5 Volts Only** (prevents ground-loop problems)
- **1.3 Arc-minute Accuracy**
- **75 mW Power Dissipation**
- **BIT Output** (Built-In Test)
- **Analog Velocity Output** (use as tachometer)
- **Reference Synthesizer** (compensates for resolver phase shift)
- **No 180 degree "False Lock-up"**
- **Very High Tracking Rate** (1800 °/sec for high frequency option)
- **DIR** (direction) **and CO** (carry outputs) (for revolution counting)
- **MIL-STD-883 Processing Is Available**



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar panel control systems

Description

Designed primarily for use within a resolver of size 15 or larger, the **Model HRD1416** is contained in a 1-inch square hermetically-sealed package. Since the converter generates it's own AC reference signal, all that is required to complete the "resolver-to-digital system" is connection to a resolver. **Model 1416** operates from a single 5 V-dc power supply (including the built-in oscillator) and consumes only 15 mA of current. The low power dissipation of 75 mW not only makes the Natel **1416** run cool, but puts less strain on the user's power supply, thereby improving component and system MTBF. The **1416** is compatible with 8- and 16-bit microprocessors and has a high frequency option with higher tracking speed and wider bandwidth. Additional superior features of the **1416** include Built-in Test, Reference Synthesizer, an anti-180 deg lock-up circuit, DIR "direction" and CO "carry" digital outputs (for revolution counting), and an analog velocity (tachometer) output.

Model 1416 generates a 0.5 or 1.0 V-rms reference signal with up to 10 mA-rms drive allowing "direct" connection to a resolver. The converter resolver input (.5 V-rms nominal) is a direct coupled "voltage follower" high impedance input, eliminating load dependent errors. The **1416** will directly interface with nearly any resolver having a transformation ratio of approximately 2-to-1 or 1-to-1.

Model 1416 is a Type-II tracking converter with zero velocity lag error. An internal reference synthesizer permits improved dynamic accuracy by reducing the effects of "speed voltages" at high rotational speeds. The accuracy of the converter is maintained with signal-to-reference phase shifts of up to ±45 degrees. An anti-180° false lock-up circuit is used to assure that the converter does not get locked into an angle 180 degrees from the true angle when a step function of 180 degrees is applied. Transferring data from the **1416** is eased through the use of a transparent latch with three-state outputs configured as two independently enabled 8-bit bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory mapped data interface and control with most popular 8- and 16-bit microprocessors and single-board computers.

A built-in test (BIT) feature provides a logic "1" when the tracking error exceeds ±1°. Monitoring of converter dynamics is facilitated through the availability of analog signals corresponding to converter tracking velocity and instantaneous tracking error. The velocity output is a high-quality characterized analog signal that can be used instead of a mechanical tachometer in many servo and control systems.

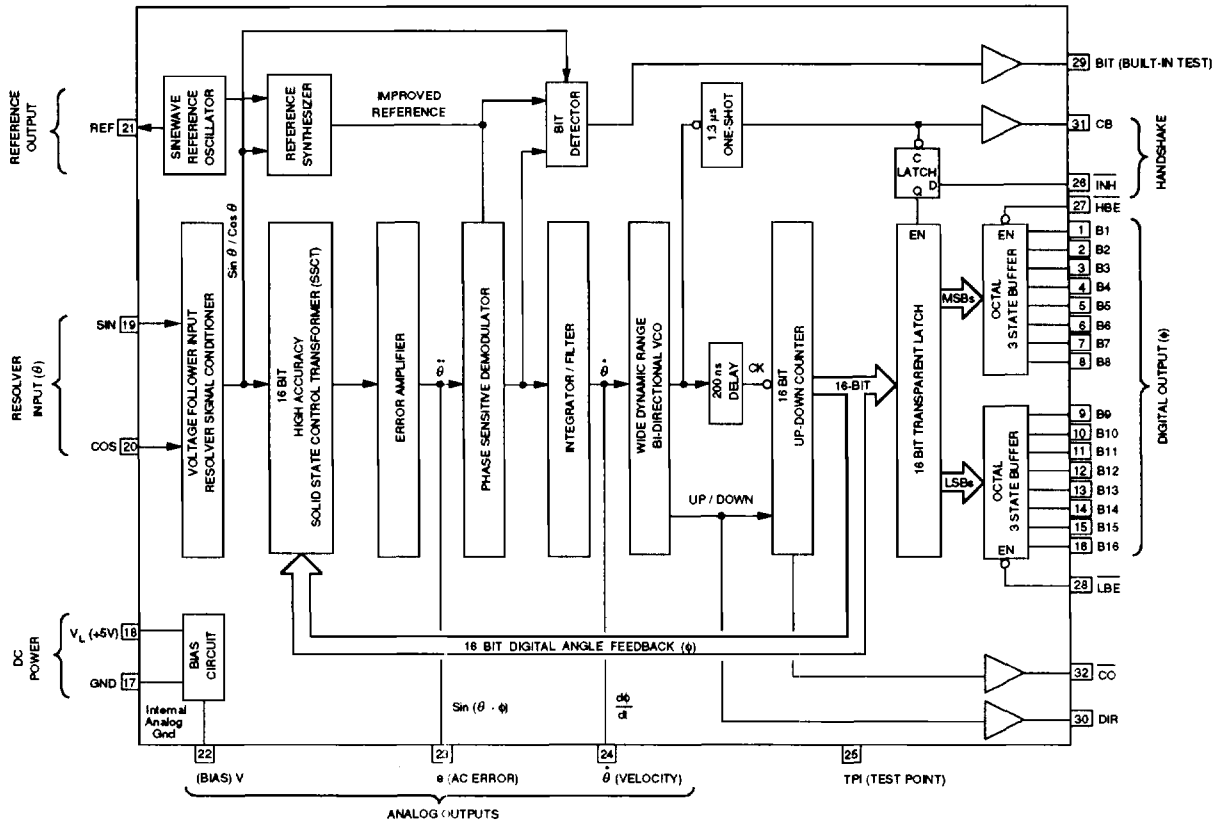


FIGURE 1 1416 Block Diagram

The operation of the **Model 1416** is illustrated in the functional block diagram of Figure 1. The **1416** is a high-gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (Φ) and the resolver input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage (e), according to the following trigonometric identity:

$$\text{"e"} = \sin(\theta - \Phi) = \sin\theta\cos\Phi - \cos\theta\sin\Phi$$

When the error voltage goes to null, $\sin(\theta - \Phi)$ is zero, which makes the angle θ equal to the angle Φ. Thus, the digital output represents the input shaft angle. Once synchronized, the output angle always tracks the input shaft angle without any lag error for constant velocity input.

The input "signal conditioner" accepts low level resolver signals $\sin\theta$ and $\cos\theta$, which are applied to the "solid state control transformer" (SSCT) discussed above. Output of the SSCT goes to "Error Amplifier". The output is applied to a "phase-sensitive demodulator" that is used to determine the polarity (phase) of the error signal "e" with respect to reference signal. Instead of using the reference signal REF as applied to the resolver, **Model 1416** generates an improved reference internally. The "reference synthesizer" obtains this improved reference from $\sin\theta$ and $\cos\theta$ signals and uses the REF (out) for coarse phase determination only.

Use of the improved reference for demodulating allows the **Model 1416** to better reject quadrature components in the error signal "e". The demodulated error signal is applied to an "integrator / filter" which, in addition to ripple and noise filtering, provides the first integration required for the Type II servo loop. The integrator / filter is also used for appropriate gain and phase compensation for loop stability (optimized for low over-shoot and fast setting time). The "wide dynamic range bi-directional VCO" performs a voltage-to-frequency conversion whose pulses or counts are accumulated in the "16-bit up-down counter". The up-down counter performs the second integration in the Type II loop. The input to the VCO inherently provides an analog indication of the digital output rate of change (velocity).

The "16-bit transparent latch" provides a means of holding the digital output steady during data transfer, while allowing the converter to continuously track the input angle. The "1.3 µs one shot" provides an output pulse (CB) for every LSB of output change. It is also used as a clock or gate for the inhibit $\overline{\text{INH}}$ "latch" to prevent attempted "data read" commands during an up-down counter output transition. The "200 ns delay" is used to prevent a race condition between the CB (Converter Busy) output and $\overline{\text{INH}}$ input.

The "3-state buffer" output is split into two 8-bit bytes to allow interfacing on both 8- and 16-bit data bus systems. The "BIT detector" provides a fault indication as well as help in eliminating false 180 degree digital output readings. The following pages provide more detailed technical discussions for some of these functions.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic conditions, the **1416** utilizes a "reference synthesizer" to correct for a phase difference between the signal and reference signals of up to ±45°.

Conventional tracking resolver-to-digital converters use a phase-sensitive demodulator to detect the phase and amplitude of the error voltage, sin (θ–Φ). One of the functions of the demodulator is to reject quadrature components in the error signal (e). A phase-sensitive demodulator rejects any quadrature signal (signal 90° out of phase) only if the synchro input and its reference are exactly in phase. Zero degree phase shift between reference and signal inputs is not practical in most applications using resolver-to-digital converters. Quadrature signal voltage can result from any of the following:

- dynamic resolver "speed voltages," – a quadrature signal that is proportional to the shaft rotational speed
- resolver "null voltages"
- capacitive coupling between resolver lines
- differential phase shift in resolver lines

This quadrature voltage will cause angular error as a variable offset if there is a phase difference between input signals and reference. For example for a 400 Hz resolver with a 30° phase shift rotating at 2.5 rps (900° / sec), the dynamic error due to speed voltage would be 0.17 degree or 10 arc-minutes!

Natel's **Model 1416** greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages from the resolver are combined to obtain an in-phase internal reference. Together with the internal reference voltage (to determine phase) this improved reference is used for demodulating the error voltage.

Built-in Test (BIT)

A BIT signal (pin 29) provides an over-velocity or fault indication output signal. The error voltage of the converter is monitored continuously, and when the tracking error exceeds approximately 1 degree (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0." Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn on – BIT output will return to logic "0" when the converter synchronizes to correct input angle ±1°
- Step-input – Instantaneous input changes greater than ±1° until the converter synchronizes
- Over velocity condition
- Excessive shaft angle modulation
- Loss of signal – Sin and Cos and / or REF
- Converter malfunction – any converter failure which prevents synchronization to the input angle

From above discussion it is apparent that the BIT output not only serves to self-test the converter but also provides an indication of the operation of the resolver transmission system as well.

No 180 False Lock-up

An additional function of the "BIT Detector" (built-in-test detector), incorporated into the **Model 1416** is to eliminate "false 180° digital output readings", during instantaneous 180° input step changes. "180° false lock-up" can occur in most resolver-to-digital converters whenever the resolver input angle is "electronically switched" or stepped from one angle to another by 180 degrees. This occurrence is most common in applications where the input is being supplied by a digital-to-resolver converter and the MSB (180° bit) is turned "ON" or "OFF."

The reason this occurs in most resolver-to-digital converters is because the "solid-state control transformer" (SSCT) used in the conversion process can produce two (2) "nulls" at the error output "e" for a given digital feedback angle. This is easily understood by trigonometric identity:

$$\sin[(\theta - \Phi) + 180] = -\sin(\theta - \Phi)$$
$$= \sin(\theta - \Phi)$$

when

$$(\theta - \Phi) = \text{zero}$$

Since error output "e" is a sine function (see theory of operation) this creates a possibility of a second null and the converter locking-up 180 degrees away from the true angle.

Natel's **Model 1416** gets around this problem by continuously monitoring the sin θ and cos θ signals and comparing the phase relationship with the digital output angle and reference signal. When a 180 degree input step is applied, the internal BIT-detect circuit is activated, which forces an error in the converter loop to move the digital output angle to the corect reading. As soon as the digital output is properly phased with the shaft angle input, this "intentional error" is removed from the converter loop.

True Single-Supply 5 V-dc Operation

One of the most outstanding features of the **Model 1416** is the single +5 V-dc power supply requirement. This feature simultaneously eliminates both unwanted "ground loop" problems and allows the elimination of ±15 V-dc power supplies in an all-digital system.

Without the single supply operation, systems that use separate analog and digital grounds for ±15 V-dc and +5 V-dc power, as many systems do, would be faced with potential ground loop problems. The result is usually excess noise on either the analog or digital supplies, which limits the effectiveness of single-point grounding schemes. These ground loops would be present with a converter that used both ±15 and +5 V-dc power because the analog (±15 V-dc) and digital (+5 V-dc) power supplies are referenced to different grounds while most multiple supply converters have only a single internal ground. The **1416** takes the agony out of these difficult systems problems by operating entirely within the digital power and ground rails of your system.

All internal circuitry is designed to operate with power supply voltage of as low as 4.5 V-dc. This is made possible by using high signal-to-noise ratio amplifiers and a unique design approach incorporated into a custom LSI chip. No performance specification is sacrificed due to the single 5 V-dc operation. In fact, the **1416** offers the most advanced design features ever available in any Resolver-to Digital converter.

Operating with a 5 V-dc supply, the converter typically requires only 15 mA of current. This low power operation results in a typical junction-to-ambient (no heat sink) temperature rise of only 4°C!

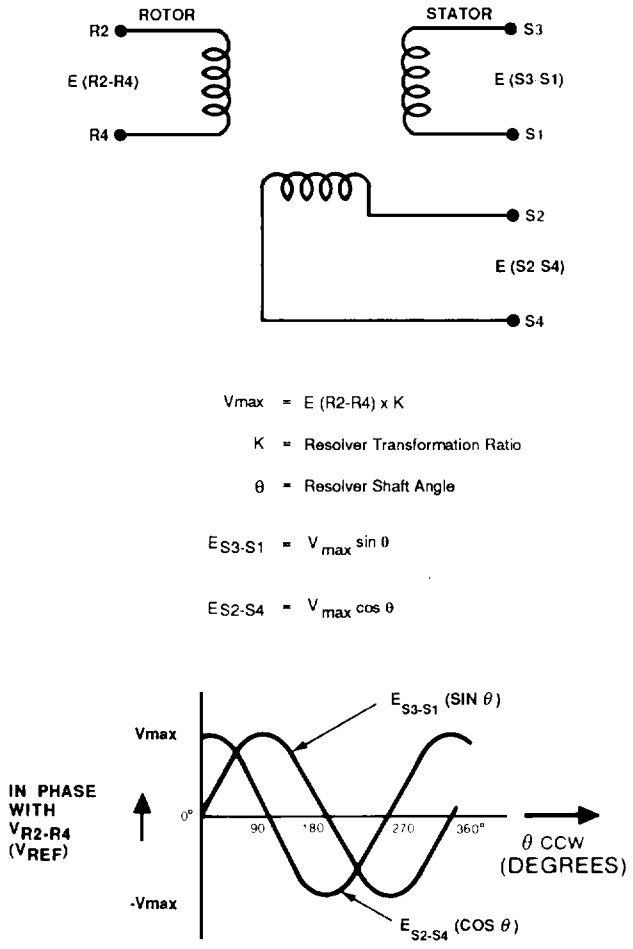


FIGURE 2 Resolver Conventions

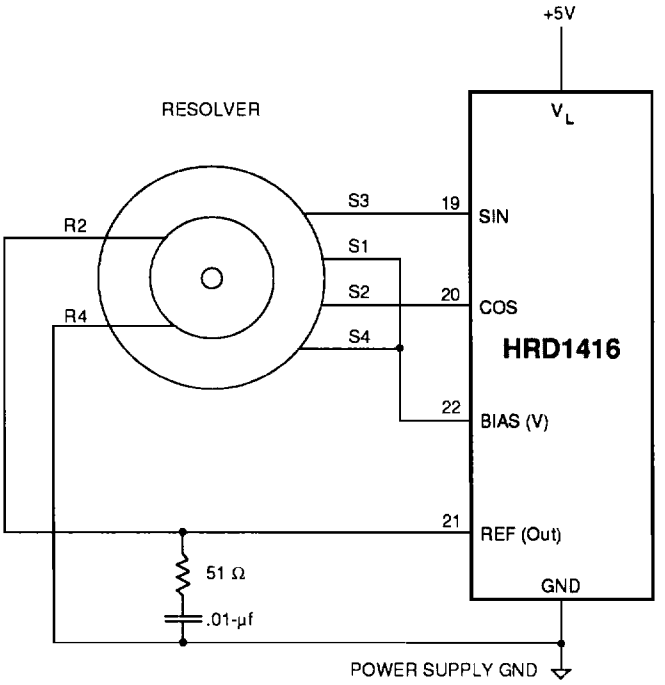


FIGURE 3 Resolver Connections

Connections of resolver to the HRD**1416** is shown in Figure 3. Standard resolver "conventions" as applicable are shown in Figure 2. Resolvers normally contain a "rotor" winding (reference input) and two "signal" windings (sin and cos outputs). The Sin (S3-S1) and Cos (S2-S4) resolver outputs are signals which are proportional to the "product" of the "sin", "cos" (respectively) of shaft angle θ and the reference voltage (R2, R4 or RH, RL), multiplied by the resolver transformation ratio (K). The reference input to the resolver (carrier signal) is essentially modulated by the shaft angle, producing "modulated" sin and cos outputs. The waveforms in Figure 2 represent the "demodulated" sin and cos outputs of the resolver, which essentially shows the amplitude relationship (in phase or out of phase) of the sin and cos outputs with respect to the reference input.

Resolvers are typically connected as shown in Figure 3. The "bias"(V) connection at Pin 22 serves as the "signal low" or "return" for the Sin and Cos resolver signals. Bias (V) is an internally generated "analog gnd" with a nominal output voltage of 2.15 V-dc. The sin and cos inputs are high impedance, voltage follower, DC coupled inputs. The nominal Sin, Cos input voltage level is 0.5 V-rms ±10%. The reference (REF) output is an A.C. coupled output (4.7uf series blocking capacitor) with an output drive of 10 mA-rms. The nominal output voltage level is either 0.5 volt or 1.0 V-rms, depending on the option selected. The suggested return path for the resolver reference LO connection is power supply GND (this return path is not critical).

If the resolver is going to be located away from the converter (more than a few feet), it is suggested to use a shielded conductor for both Sin and Cos signals with the shield terminated to power supply GND. The **1416** Reference output (pin 21) has short circuit limiting (30 mA typical) and can drive a maximum capacitive load of 10,000 pf. As a general practice, decoupling capacitors should be used on the power supply (+5V) near the **1416** converter. As a minimum, a 1-μf tantalum in parallel with a 0.01-μf ceramic capacitor is recommended. To improve the REF (Out) stability when driving reactive loads (any resolver), a series RC (51 ohm in series with .01-μf) should be connected between REF (Out) and GND, as shown in Figure 3.

The **1416** will interface with almost any resolver with a "transformation ratio" of 2:1 or 1:1 (depending on option). As an example, a resolver which is specified with a reference voltage of 26 V-rms and an output voltage of 11.8 V-rms has a "transformation ratio" of (2.2:1), which is close enough to 2:1, and therefore can be used directly with the **1416** converter. Almost all resolvers can be operated at "lower" than specified reference voltage levels with little or no degradation in accuracy.

Pin Designations

V_L	Power Supply Voltage Logic Voltage 5 V-dc ±10%
GND	Power Supply Ground Digital Ground REF (Out) return
B1 - B16	Parallel Output Data Bits – B1 is MSB = 180 degrees B16 is LSB = 0.0055 degree
SIN, COS	Input Analog Signals
REF	Reference Voltage Output
$\dot{\theta}$	Velocity Output – dc analog voltage proportional to rotational speed of the input shaft angle. Output is referenced to bias voltage (V)
V	Bias Voltage – Internally generated reference voltage, serves as reference ground for all analog inputs and outputs.
e	Error Voltage – ac analog voltage proportional to instantaneous tracking error of the converter. Output is referenced to bias-voltage (V)
$\overline{INH}$	Inhibit Function – A logic "low" freezes the digital angular output. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal active pull-up will apply V_L to the pin.
CB	Converter Busy – A 1.3 μs pulse which occurs during updating of the holding register. Output data can be transferred at the trailing edge of the CB pulse. When converter output is not changing CB is at logic "low".
BIT	Built-In Test – A Logic "high" output indicates that output is not tracking the input analog signal within ±1°.

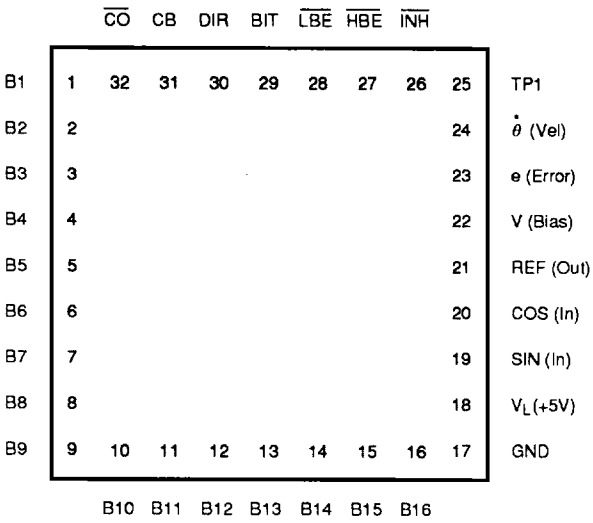


FIGURE 4 HRD1416 Pin Assignments

$\overline{HBE}$	High Byte Enable – Data bits B1 through B8 are enabled (low-impedance state of 3-state output) when HBE is set to a logic "low". When HBE is set to a logic "high", the data bits B1 through B8 are disabled (high-impedance state of 3-state output).
$\overline{LBE}$	Low Byte Enable – Data bits B9 through B16 are enabled when LBE is set to a logic "low". When LBE is set to a logic "high", the data bits B9 through B16 are disabled.
DIR	Direction Output – Digital signal indicating resolver (converter) direction of shaft rotation (CW-increasing or CCW-decreasing angle). Logic "1" = increasing angle, Logic "0" = decreasing angle.
$\overline{CO}$	Carry Output – Digital output pulse (1.3 μs typ.) indicating when the output changes from 359.995 to 0 degrees or vice versa, (from all bits "on" to all bits "off", or vice versa).
TP1	Test Point – For factory use only.

Absolute Maximum Ratings

Signal Inputs ..... GND to V_L
Supply Voltage (V_L) ..... +6.5 V-dc
Digital Inputs ..... -0.3 V-dc to V_L
Storage Temperature ..... -65°C to +135°C

When installing or removing the converter from the printed circuit boards or sockets, it is recommended that the power supply and input signals be turned off. Decoupling capacitors are recommend on the power supply V_L. A 1-µF tantalum capacitor in parallel with 0.01-µF ceramic capacitor should be mounted as close to the supply pin (18) as possible.

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Output Resolution			
	16-bits (0.33 arc-minutes)		Note 2
Accuracy			
	± 5.2 arc-minutes (Option S) ± 2.6 arc-minutes (Option H) ± 1.3 arc-minutes (Option V)	Accuracy applies over the full operating temperature range, ±10% frequency variation and includes hysteresis	Note 1
Reference Output			
Voltage	0.5 V-rms ±10% 1.0 V-rms ±10%	(Option 5) (V_L = 5.0V-dc) (Option 1) (V_L = 5.0V-dc)	Note 1
Frequency	2000 Hz ±10% (Option 2) 800 Hz ±10% (Option 8) 400 Hz ±10% (Option 4) 60 Hz ±10% (Option 6)	(±20% over full temp range) (±20% over full temp range) (±20% over full temp range) (±20% over full temp range)	Note 1
Output Drive (minimum)	±10 mA-rms (Option 5) ±10 mA-rms (Option 1) ± 5 mA-rms (Option 1)	Any load (10,000 pf max) With > 70% inductive load With resistive load	Note 2
Output Impedance (AC coupled)	< 5 ohms in series with 4.7uf (nominal)	Xc = 17 ohms (nominal) @ 2000 Hz = 42 ohms (nominal) @ 800 Hz = 85 ohms (nominal) @ 400 Hz = 565 ohms (nominal) @ 60 Hz	Note 3
Resolver Input		**Sin and Cos inputs**	
Input Voltage	0.5 V-rms±10%	Inputs are with respect to the internal analog gnd "Bias" (V)	Note 1
Input Impedance	> 5 Meg ohms	Voltage follower buffer input	Note 3
Reference Synthesizer			
Phase-shift allowed between Input signals and Input reference	±45° guaranteed ±65° typical	Without any degradation in accuracy specification	Note 2
Digital Inputs		**CMOS transient protected**	
$\overline{HBE}$	Logic "1" Logic "0"	8 MSBs are in the high impedance state of 3-state output 8 MSBs are enabled	Note 1
$\overline{LBE}$	Logic "1" Logic "0"	8 LSBs are in the high impedance state of 3-state output 8 LSBs are enabled	Note 1
$\overline{INH}$	Logic "1" Logic "0"	Digital output follows analog input signals Output data latched in holding register (does not interrupt converter tracking loop)	Note 1
Voltage Levels Logic "0" Logic "1"	 -0.3 V-dc to 0.8 V-dc 2.4 V-dc to 5 V-dc	For V_L = 5 V-dc	Note 2
Input Currents			
$\overline{HBE}$, $\overline{LBE}$	15 μA typical (30 μA max) "active" pull down to ground (GND)	When not used, may be left unconnected	Note 3
$\overline{INH}$	-15 μA typical (-30 μA max) "active" pull up to the power supply (V_L)	When not used, may be left unconnected	Note 3

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Outputs		**CMOS Outputs**	
Data Bits (B1-B16)	Natural Binary Angle	Positive logic	
CB	Logic "0" Logic "1" (Nominal 1.3 μs pulse for every LSB change)	Output angle not changing Output angle changing (leading edge initiates output change - see figure 5)	Note 1
BIT	Logic "0" Logic "1"	Digital output tracking analog input Fault indication (tracking error >±1° typical)	Note 1
Drive Capability B1-B16, CB, BIT, DIR, $\overline{CO}$	1 Standard TTL minimum	For V_L = 4.5 V-dc, over full temp range	Note 3
Logic "0" sink current Logic "1" source current	1.6 mA (min) @ 0.4 V-dc -1.6 mA (min) @ 3.0 V-dc		Note 3
HI-Z Output Leakage Data Bits (B1-B16)	±10 μA maximum	Output capacitance = approx. 5 pF	Note 3
DIR (direction)	Logic "0" Logic "1"	Angle is decreasing (CCW) (Down) Angle is increasing (CW) (Up)	Note 1
$\overline{CO}$ (carry out)	Logic "0" pulse (1.3 μs typical)	All data bits changing from all "on" to all "off" or vice versa	Note 1
Analog Outputs	**Typical, unless specified**		
V (Bias Voltage)	1/2 (V_L – 0.7) ±10%	2.15 V-dc ±10% for 5 V-dc supply	Note 3
e (unfiltered ac error)	750 mV-rms typical for 1° error	ac voltage referenced to V	Note 3
Drive Capability	± 1 mA minimum	All analog outputs	Note 3
$\dot{\theta}$ Velocity Output	**Typical, unless specified**	**dc voltage referenced to V (bias)**	
Polarity	Negative for increasing angle		Note 3
Scale Factor (Gain) @ 25°	0.835 mV/deg/sec typical 1.22 mV/deg/sec typical 6.11 mV/deg/sec typical	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 2
Temperature Coefficient Power Supply Dependence	±500 PPM/°C typical -1% per percent maximum	All Models	Note 3
Full Scale Output @ 25°C	1.5 V-dc @1800°/sec typical 1.1 V-dc @ 900°/sec typical 1.1 V-dc @180°/sec typical	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 2
Linearity @ 25°C	±5% of full scale maximum ±2% of full scale maximum ±1% of full scale maximum	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 2
Temperature Coefficient Power Supply Dependence	±200 PPM/°C typical 0.1% per percent typical	All Models	Note 3
Output Noise Static Input	3 mV-rms typical 3 mV-rms typical 3 mV-rms typical	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 3
Input changing at a constant maximum tracking rate	15 mV-rms typical 15 mV-rms typical 30 mV-rms typical	800 Hz and 2000 Hz Models 400 Hz Models 60 Hz Models	Note 3
Output Offset @ 25°C	± 5 mV-dc typical ±20 mV-dc maximum	All Models	Note 2
Temperature Coefficient Power Supply Dependence	±30 μV/°C typical ±20 μV per percent typical		Note 3
Δ Gain vs Polarity	10% maximum	All Models	Note 2
Temperature Coefficient Power Supply Dependence	±200 PPM/°C typical 0.1% per percent typical		Note 3

PARAMETER	VALUE	REMARKS	TEST LEVEL
Dynamic Characteristics	Typical, unless specified	Specified for power supply = +5 V-dc	
Velocity Constant (K_V)	∞	Type II servo loop	Note 3
Tracking Rate (minimum)	1800° /sec 900° /sec 180° /sec	For 800 and 2000 Hz Models For 400 Hz Models For 60 Hz Models	Note 1
Maximum Acceleration (typical)	400,000° /sec² 100,000° /sec² 4,000° /sec²	For 800 and 2000 Hz Models For 400 Hz Models For 60 Hz Models	Note 3
Acceleration Constant (nominal)	192,000 /sec² 48,000 /sec² 1,920 /sec²	For 800 and 2000 Hz Models For 400 Hz Models For 60 Hz Models	Note 3
Acceleration for 1 LSB error (LSB=0.0055°)	1,055° /sec² typical 264° /sec² typical 11° /sec² typical	For 800 and 2000 Hz Models For 400 Hz Models For 60 Hz Models	Note 3
Settling time to 1 LSB (for 179° step change)	150 ms maximum 300 ms maximum 1350 ms maximum	For 800 and 2000 Hz Models For 400 Hz Models For 60 Hz Models	Note 2
Settling time to 1 LSB (small signal step < 1.4°)	25 ms maximum 50 ms maximum 250 ms maximum	For 800 and 2000 Hz Models For 400 Hz Models For 60 Hz Models	Note 2
Converter Bandwidth	200 Hz typical 100 Hz typical 20 Hz typical	For 800 and 2000 Hz Models For 400 Hz Models For 60 Hz Models	Note 3
Power Supply			
Voltage	5 V-dc ±10%	Without degradation in accuracy specification	Note 3
Current	25 mA typical, 35 mA maximum 15 mA typical, 25 mA maximum	For 800 Hz and 2000 Hz Models For 400 Hz and 60 Hz Models	Note 1
Thermal Characteristics			
Junction Temperature Rise above case	1°C typical, 4°C maximum	For component with highest temperature rise	Note 3
Case Temperature Rise above ambient	3°C typical, 6°C maximum 10°C max. (800, 2000 Hz Models)	Without any heat sink	Note 3
Power Dissipation For V_L= 5 V-dc, No load	75 mW typical, 125 mW max. 175 mW max.	For 60 Hz and 400 Hz Models For 800 Hz and 2000 Hz Models	Note 3
Physical Characteristics			
Type	32-pin Hermetic 1" square		
Size	1.0 x 1.0 x 0.21 inch (25 x 25 x 5.3 mm)		Note 3
Weight	0.6 oz (17 g) maximum		Note 3

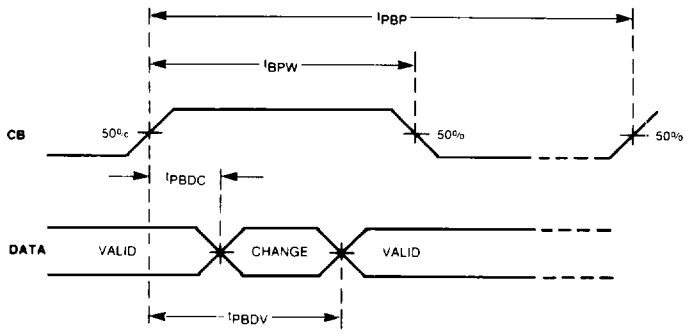
NOTE 1. Compliance of each componenet to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

CHARACTERISTIC	LIMITS			UNITS	FIGURE
	MIN	TYP	MAX		
BUSY PULSE WIDTH (t_{BPW})	0.8	1.3	2.0	µs	5
BUSY PERIOD (t_{PBP})	2.0	NOTE 1	—	µs	5
BUSY TO DATA CHANGE (t_{PBDC})	100	500	—	ns	5
BUSY TO DATA VALID (t_{PBDV})	—	600	800	ns	5
INHIBIT TO DATA STABLE (t_{PIDS})	0	—	1.0	µs	6,7
INHIBIT TO DATA UP-DATE (t_{PIDU})	100	—	—	ns	6,7
INHIBIT UPDATE PULSE WIDTH (t_{IPW})	2.0	—	—	µs	7
HIGH Z TO LOW Z (t_{PHZL})	30	150	250	ns	8
LOW Z TO HIGH Z (t_{PLZH})	30	100	200	ns	8
TRANSITION HIGH TO LOW (t_{THL}) 90%-10%	—	45	75	ns	9
TRANSISTION LOW TO HIGH (t_{LHT}) TTL 10%-50%	—	60	100	ns	9
(t_{TLH}) CMOS 10%-90%	—	120	200	ns	
DIRECTION TO CB (t_{DCB})	0.5	1.0	2.0	µs	10
CARRY PULSE WIDTH (t_{CPW})	0.5	1.3	2.0	µs	10
CARRY "LOW" TO CB (t_{CLCB})	0.5	1.0	2.0	µs	10
CARRY "HIGH" TO CB (t_{CHCB})	0.1	0.2	0.4	µs	10



NOTE 1: **Busy Period (t_{PBP})** = $\frac{K \cdot 10^6}{2^N \cdot R}$ (µs)

Where,

N = Converter Resolution (16)

K = 360 (For Degrees) or = 2π (For Radians)

and

R = Rate (Degrees / Second) or = Rate (Radians / Second)

For Reference:

Busy Frequency = $\frac{2^N \cdot R}{K}$ (Hz)

Rate (R) = $\frac{K \cdot \text{Busy Frequency}}{2^N}$

FIGURE 5 Converter Busy and Data Timing

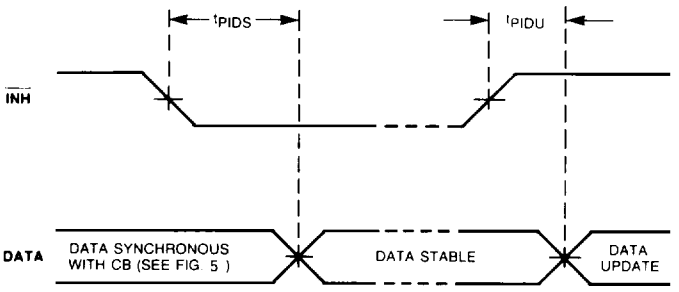


FIGURE 6 Inhibiting Output Data Update

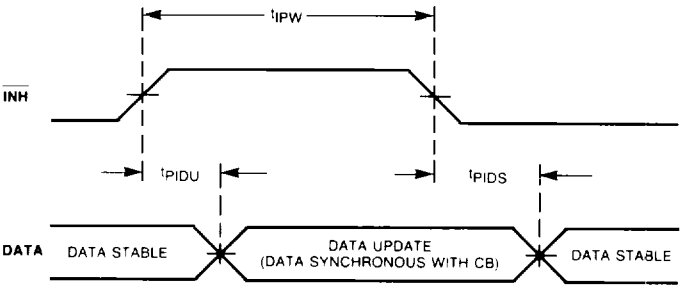


FIGURE 7 Enabling Output Data Update

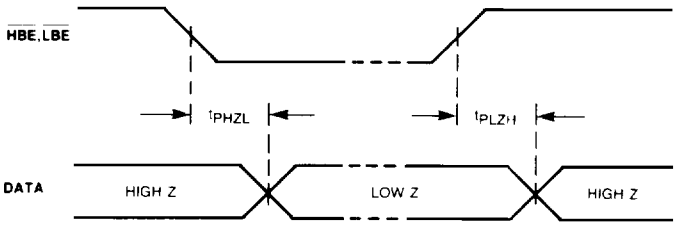


FIGURE 8 3-State Output

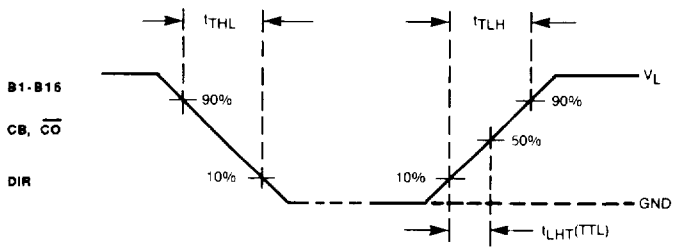


FIGURE 9 Transition Times

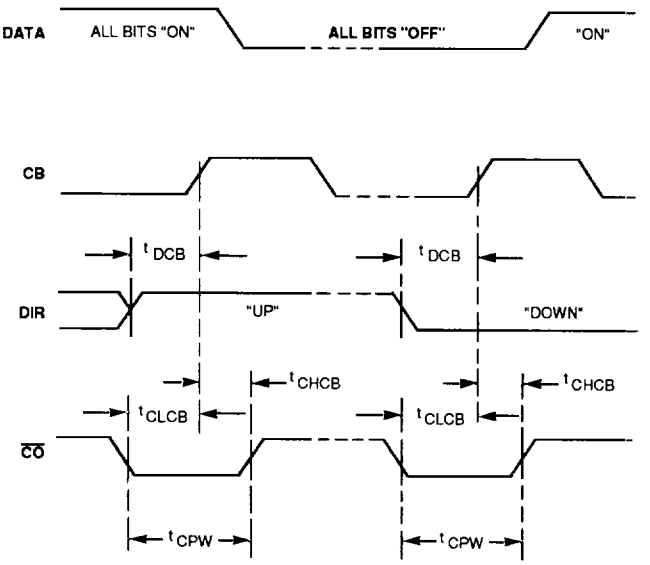


FIGURE 10 Direction and Carry Out Timing

Data Transfer

Due to the nature of the Type II servo conversion mechanism incorporated in the **1416**, the output data angle always tracks the resolver input shaft angle within the converter's rated maximum tracking rate (angular velocity) and bandwidth. Theoretically, for every 0.0055 degree of input angle change, there will be a corresponding data output change of one LSB. To prevent reading data during an output change or transition, the following methods of data transfer can be used:

1) Synchronous transfer with shaft angle change.

   Use CB (Converter Busy) pulse to clock data into an external register. Use the falling edge of CB as an edge-triggered clock. (Rising edge of CB could be used but data would have an additional error of ±1 LSB.) Data changes within 800 ns after the rising edge of the CB pulse.

2) Asynchoronous transfer with shaft angle change (using CB).

   Monitor the CB (Converter Busy) during a data transfer attempt. If CB is at logic "1", (the data will be void) . . . try another data transfer attempt. If CB is at logic "0" the data will be good. Note that the longest CB pulsewidth and therefore the longest wait period is 2μsec. The CB pulse can essentially be used to gate an external data clock enable since the converter updates within the CB logic "1" duration (2μs maximum).

3) Asynchronous transfer with shaft angle change (using $\overline{INH}$).

   The simplest method of data transfer (which is completely independent of input shaft angle change) is to use the inhibit ($\overline{INH}$) function to hold or freeze the current data output angle. Set the $\overline{INH}$ input to logic "0" . . . wait a minimum of 1μs . . . transfer the data . . . return $\overline{INH}$ to logic "1" for a minimum of 2μs. This method of asynchronous data transfer from the 1416 is shown in Figures 12 and 13.

It should be noted that the $\overline{INH}$ control does not affect the conversion process . . . it only affects the transparent output latch. If the resolver angle input changes while an inhibit is applied ($\overline{INH}$ = "0"), the internal data angle (up–down counter output) will still track the input. Fresh output data (B1-B16) will be available within 2μs after the $\overline{INH}$ input returns to logic "1" (un-inhibit), regardless of the previous $\overline{INH}$ logic "0" duration.

Since the **1416** is a "tracking type" converter, no external "start conversion" or "clock" signals are required. The digital angle output "continuously" tracks the resolver angle input. If the $\overline{INH}$ input is tied to logic "1", the data output (B1-B16) will continuously "track" the resolver input. For "non-bus" and/or "no clock" systems, the **1416** converter can be connected as shown in figure 11, for "continuous data transfer".

Note: The CB output (Converter Busy) will always produce a pulse for every LSB of output angle change, regardless the state of the $\overline{INH}$ input.

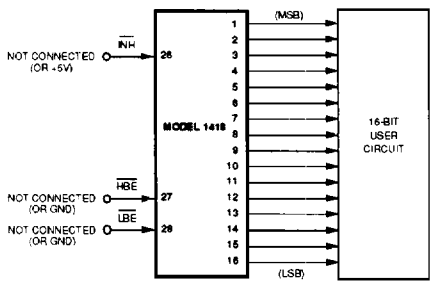
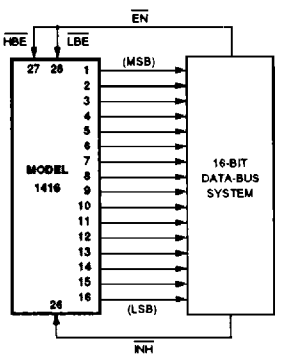


FIGURE 11 Continuous Data Transfer

Single-Byte Data Transfer on 16 - Bit Data Bus



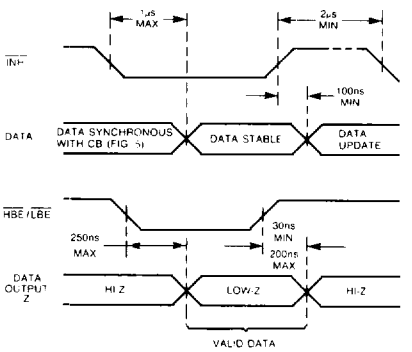


FIGURE 12 Digital Connections and Timing for Single-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from the **Model 1416** to a 16-bit 3-state data-bus system is shown in Figure 12. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 1μs before transferring valid data.

2) Set $\overline{HBE}$ and $\overline{LBE}$ to logic "0" (3-state enables) for a minimum of 250 ns before transferring valid data.

   Note: The last device on the data-bus should be set to high impedance state no later than 30 ns after $\overline{HBE}$ and $\overline{LBE}$ are set to logic "0".

3) Transfer Data

4) Return $\overline{HBE}$ and $\overline{LBE}$ to logic "1" at least 200 ns before the next device is put on the data bus.

   Note: The data output remains in the low-Z state for a minimum of 30 ns after the rising edge of $\overline{HBE}$ and $\overline{LBE}$, therefore data can be transferred at the rising edge of $\overline{HBE}$ and $\overline{LBE}$ . . . provided the data hold requirement of the external device is less than 30 ns.

5) Return $\overline{INH}$ to logic "1" no earlier than 100 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2 μs to allow update of fresh accurate output data.

   Note: $\overline{INH}$ (inhibit) input function is independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state enable) inputs.

Two-Byte Data Transfer on 8-Bit Data Bus

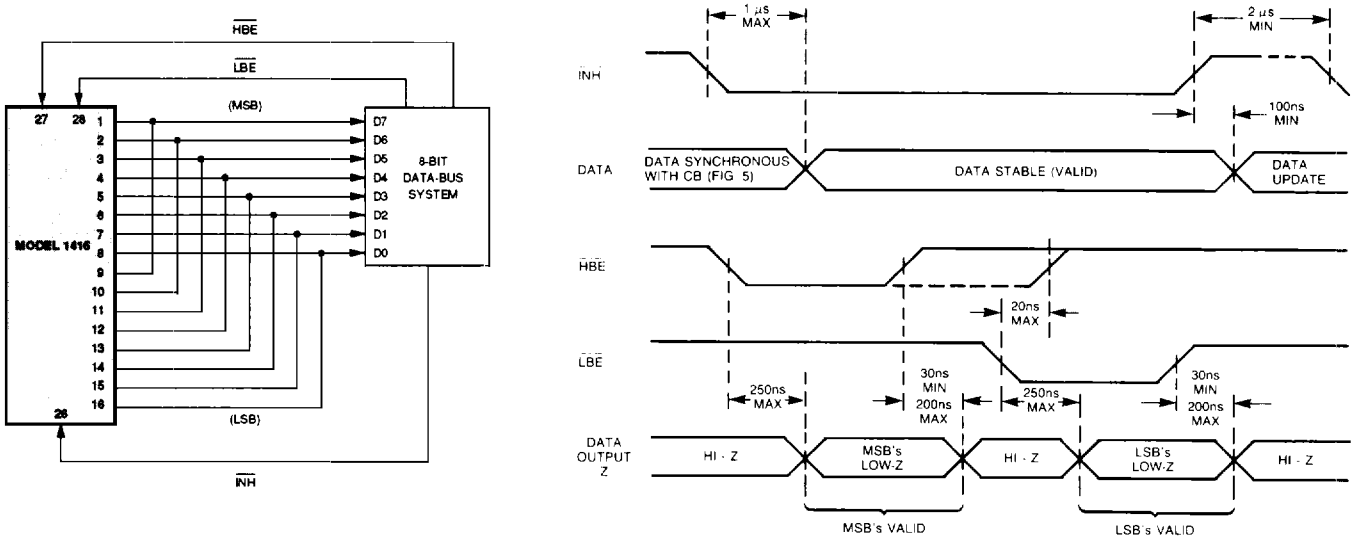


FIGURE 13 Digital Connections and Timing for Two-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from **Model 1416** to an 8-bit 3-state data-bus system is shown in Figure 13. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 1 µs before transferring valid data.

2) Set $\overline{HBE}$ to logic "0" (high-byte-enable) for a minimum of 250 ns before transferring valid data (MSBs).

Note: The last device on the data-bus should be set to high impedance state no later than 30 ns after $\overline{HBE}$ is set to logic "0".

3) Transfer MSBs.

4) Return $\overline{HBE}$ to logic "1" no later than 20 ns after $\overline{LBE}$ is set to logic "0".

5) Set $\overline{LBE}$ to logic "0" (low-byte-enable) for a minimum of 250 ns before transferring valid data (LSBs), but not more than 20 ns before $\overline{HBE}$ has returned to logic "1" (rising edge).

6) Transfer LSBs.

7) Return $\overline{LBE}$ to logic "1" at least 200 ns before the next "device" is put on the data-bus.

8) Return $\overline{INH}$ to logic "1" no earlier than 100 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 2 µs to allow update of fresh accurate output data.

Notes:

— $\overline{HBE}$ and $\overline{LBE}$ data bytes can be transferred in any sequence ($\overline{HBE}$ or $\overline{LBE}$ first). The timing requirements are the same for both $\overline{HBE}$ and $\overline{LBE}$ data byte enables.

— The data output remains in the low-Z state for a minimum of 30 ns after the rising edge of $\overline{HBE}$ and/or $\overline{LBE}$, therefore data can be transferred at the rising edge of $\overline{HBE}$ and/or $\overline{LBE}$ respectively . . . provided the data hold requirement of the external device is less than 30 ns.

— $\overline{INH}$ input function is independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state enable) inputs.

— The CB output (Converter Busy) will always produce a pulse for every LSB of output angle change, regardless of the state of the $\overline{INH}$ (inhibit) input or $\overline{HBE}$/$\overline{LBE}$ (3-state enable) inputs.

Revolution Counting

The model **1416's** "direction" (DIR) and "carry out" (CO) signals can be used to monitor resolver "revolutions" (or turns) in "multi-turn" systems. Figure 14 shows a typical connection to a "4516" type Up/Down counter. In this configuration the counter(s) is synchronously clocked by the CB (converter busy) output from the **1416**. The counter output is incremented or decremented by "one count" on the rising edge of CB, when a "negative" CO pulse is sent from the **1416**, indicating an angle transition from 359.995 to 0.000 degrees (all bits "on" to all bits "off") or vice-versa. Additional Up/Down counters can be "cascaded" to any number of bits, by extending the CB, DIR and "carry" from the previous counter stage. The counter's "reset" and/or "preset" inputs can be used to "initialize" the "revolution" count output.

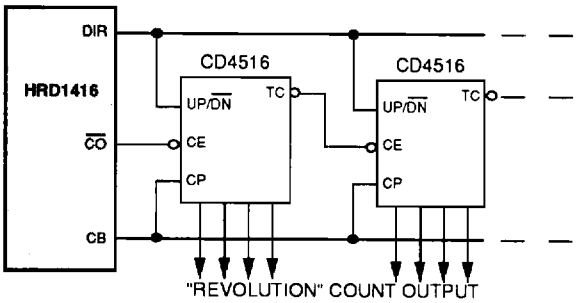


FIGURE 14 Resolver Revolution Counting

8051 Microcontroller Interface

Figure 15 shows a typical interface between the popular 8-bit 8051 microcontroller and the **HRD1416** converter. In this circuit configuration, "memory mapping" is used to address up to four **1416** converter channels, while allowing easy expansion to additional R/D converter channels or other peripheral I/O devices. The **1416** will meet the interface timing requirements for the maximum 8051 clock frequency of 12 MHz.

In this interface mode, Port 0 provides the multiplexed low order address and data bus and Port 2 provides an optional high order address bus (A8-A15), which is used for "external" program memory or 16-bit addressable data memory. In this application shown, Port 2 (bit 0) is used as a "chip select" bit to enable the address decoder and to "inhibit" all **1416** R/D converters on the bus. If "external" program memory is used, another unused "port bit" (Port 1 or 3) should be used instead of Port 2, as the "chip select" bit.

A typical sequence of events for data transfer would be as follows:

1) Set P2.0 to logic "0" (inhibit R/D) using CLR "bit" instruction.
2) Read the "High Byte" from the #1 **HRD1416** using MOVX instruction.
3) Read the "Low Byte" from the #1 **HRD1416** using MOVX instruction.
4) Repeat steps 2 and 3 for any additional **HR1416**s on the bus.
5) Set P2.0 to logic "1" (un-inhibit) using the SETB instruction).

Additionally, the status of the **HRD1416's** BIT (built-in test) output can be read through any unused I/O port at any time in the program.

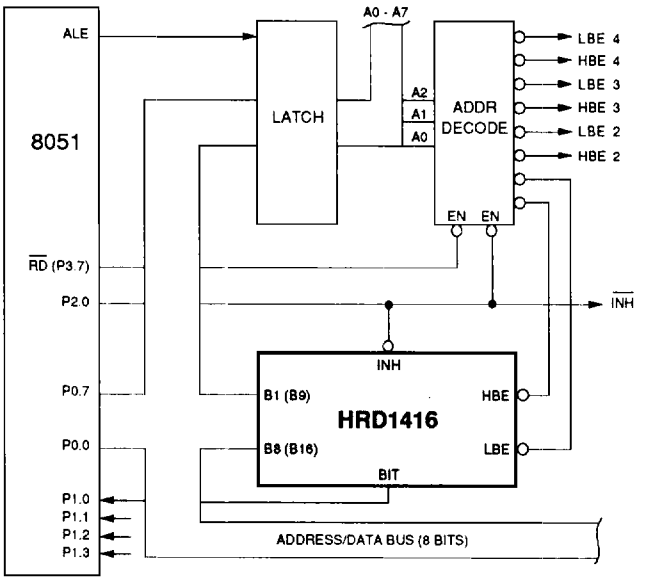


FIGURE 15 HRD1416 to 8051 Interface

Analog Outputs

As a by-product of the conversion process, the **Model 1416** produces various analog signals. Some of these analog signals have proven useful in various applications and are therefore brought out. The absolute value of these analog outputs is not critical to the overall conversion process. Therefore, unless otherwise specified, they are not closely controlled or characterized functions. These outputs are:

- V (pin 22), Internal analog ground (Bias)
- e (pin 23), ac error
- $\dot{\theta}$ (pin 24), Velocity output

"e", the ac error, is an ac voltage (at the output of error amplifier), which is proportional to the instantaneous error of the converter sin $(\theta-\Phi)$ . . . see theory of operation. The output "e" is also proportional to the input angular acceleration . . . the rate of change of angular velocity. This angular error as a function of acceleration is inversely proportional to the acceleration constant (K_A).

$$\text{error (degrees)} = \frac{\text{angular acceleration (degrees/sec}^2)}{K_A\ (\text{sec}^{-2})}$$

For 1 degree error, the nominal magnitude of the error voltage is 750 mV-rms. Polarity of the error is determined by demodulating (phase sensitive) this voltage with the reference voltage (REF).

"$\dot{\theta}$" is a dc voltage proportional to the velocity of the digital output angle (thereby the input shaft angle). The voltage goes negative for increasing digital angle and goes positive for decreasing digital angle. At maximum tracking velocity, the output voltage is 1.1 volts-dc (1.5 volts-dc for 800/2000 Hz models). Detailed specification for velocity functions are provided on page 7. Dynamic characteristics including open loop and closed loop transfer functions are provided on the following pages.

"V", internal analog ground, also referred to as the "bias voltage" provides a reference point for all analog functions. The typical value of the bias voltage, V, is:

$V = 1/2\ (V_L - 0.7\ \text{V-dc})$

$= 2.15\ \text{V-dc} \pm 10\%\ (\text{for } V_L = +5\ \text{V-dc})$

All analog outputs have a minimum output drive of ±1 mA with respect to V (bias). For a power supply of +5 V-dc, the minimum output swing is ±1.1 V peak with respect to V.

If a bipolar signal, with respect to power supply ground, is required for any analog output, a difference circuit, as shown in Figure 16, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

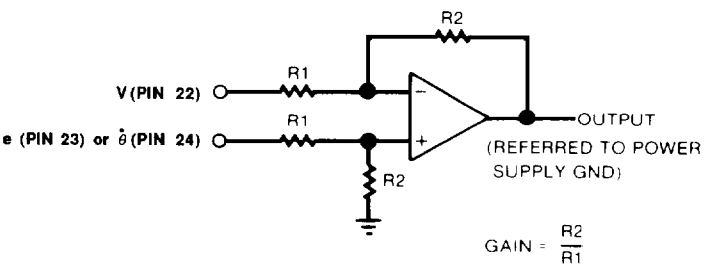


FIGURE 16 Difference Circuit for Bipolar Analog Outputs

HRD1416 incorporates a high gain, Type II, servo loop to provide accurate real-time Resolver-to-Digital conversion. The converter is characterized for the following dynamic input angle conditions:

1) Static Input Angle

2) Constant Rate of Change of Input Angle Position (Constant Velocity)

3) Constant Rate of Change of Input Angular Velocity (Constant Acceleration)

4) Variable Rate of Change of Angular Velocity (Sinusoidal Modulation)

5) Infinite Rate of Change of Angular Velocity (Step Input)

The **1416** accuracy specification applies for **Static (1)** and **Constant Velocity (2)** input conditions, as long as the maximum converter tracking rate is not exceeded.

For **Constant Acceleration (3)** of input angle, the digital output will lag the input by the following amount:

$$\text{Acceleration Lag (error)} = \frac{\text{Input Angle Acceleration}}{K_A}$$

The values of maximum tracking rate and acceleration constant (K_A) for different frequency options are given in the specification table (page 8). Note that the specified K_A is typical and is not a tightly controlled parameter (converter K_A is analogous to the open-loop gain of an operational amplifier).

For Sinusoidal Shaft Angle Modulation (4), the digital angle output will lag the input by the following amount:

$$\text{Sinusoidal lag (error p-p)} = \frac{2 \times \pi^2 \times \text{Amp (p-p)} \times Fo^2}{K_A}$$

Where: Amp (p-p) = peak-peak angle modulation level
Fo = modulation frequency (Hz)
K_A = converter acceleration constant

The Peak Rate (Velocity) for a given sinusoidal modulation is:

Rate (degrees/sec) = π x Amp (degrees p-p) x Fo (Hz)

For **Step Inputs (5),** the digital angle output will respond as a function of the converter's Large Signal and Small Signal transient response.

The **Large Signal** transient response is dependent solely on the maximum velocity (ω max) and the maximum acceleration (α max) of which the converter is capable. The large signal parameters are defined in Figure 17. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals. Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The **Small Signal** settling time (t_S) is specified for step inputs of less than 1.4 degrees. For small signal steps, the settling time is a function of the transient response of the converter.

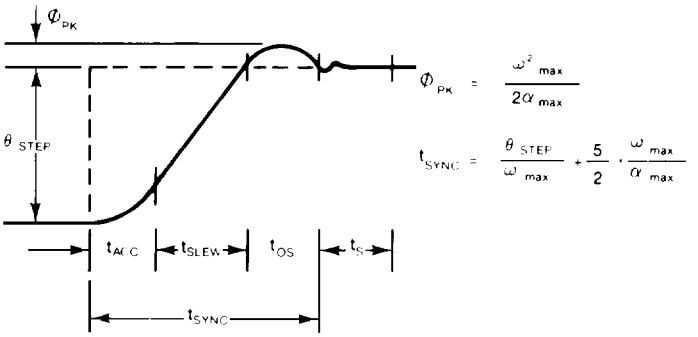


FIGURE 17 Large Signal ($\geq$ 1.4°) Response Parameters

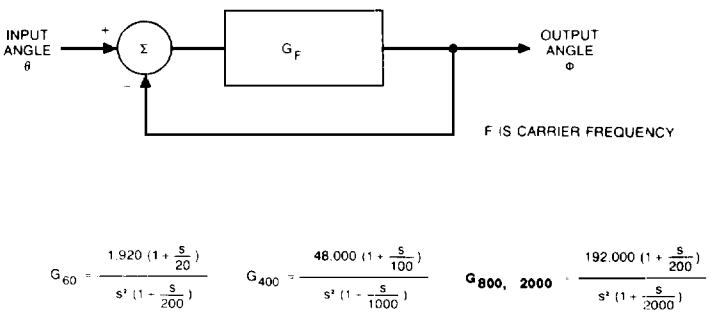


FIGURE 18 Transfer Functions for 1416

Transfer Function

The basic control loop model and transfer functions for 60-Hz, 400-Hz and 800-Hz/2000 Hz models are shown in Figure 18. A more detailed model with corresponding transfer functions for both position and velocity output is shown in Figure 20. Typical values for transfer function parameters for different frequency options are shown in the table of Figure 19.

Transfer function parameters are determined by the specified reference frequency option of the converter (see Figure 19). The 800 Hz and 2000 Hz options share the same transfer function parameters, therefore they have the same converter dynamics such as, tracking rate, settling time and bandwidth. The only difference between the 800 Hz and 2000 Hz "model" is the operating reference frequency.

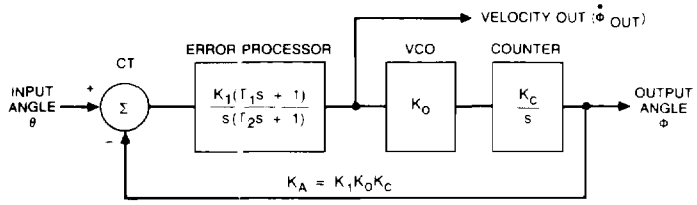
The **HRD1416** can be custom tailored at the factory to meet specific static and dynamic converter characteristics for special applications. R/D converter specifications which are often customized include: converter bandwidth, tracking rate, output resolution and reference frequency. Contact a Natel sales representative for additional information.

For a better understanding of the dynamics of the **1416**, bode plots for converter gain and output phase for 60-Hz, 400-Hz and 800-Hz/2000-Hz options are shown in Figures 21 and 22.

Results of actual performance of step responses for both large and small signal inputs performed on typical converters are shown in Figure 23.

PARAMETER	UNITS	FREQUENCY OPTION		
		60 Hz	400 Hz	800 Hz 2000Hz
K_A	sec^{-2}	1,920	48,000	192,000
K_O	$\frac{Counts}{Volt \cdot Sec}$	29,800	149,000	218,000
K_C	$\frac{Radians}{Count}$	9.587×10^{-5}	9.587×10^{-5}	9.587×10^{-5}
K_1	$\frac{Volts}{Radian}$	672	3360	9187
T_1	ms	50.0	10.0	5.0
T_2	ms	5.0	1.0	0.5
$K_O K_C$	$\frac{Radians}{Volt \cdot Sec}$	2.857	14.28	20.90

FIGURE 19 Transfer Function Parameters (Typical Values)



POSITION GAIN (OPEN LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_A(T_1s + 1)}{s^2(T_2s + 1)}$

VELOCITY GAIN (OPEN LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_1(T_1s + 1)}{s(T_2s + 1)}$

POSITION GAIN (CLOSED LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_1s + 1}{\frac{T_2s^3}{K_A} + \frac{s^2}{K_A} + T_1s + 1}$

VELOCITY GAIN (CLOSED LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_1s^2 + s}{\frac{T_2s^3}{K_1} + \frac{s^2}{K_1} + T_1K_OK_Cs + K_OK_C}$

FIGURE 20 Detailed Transfer Function Model

Bode Plots

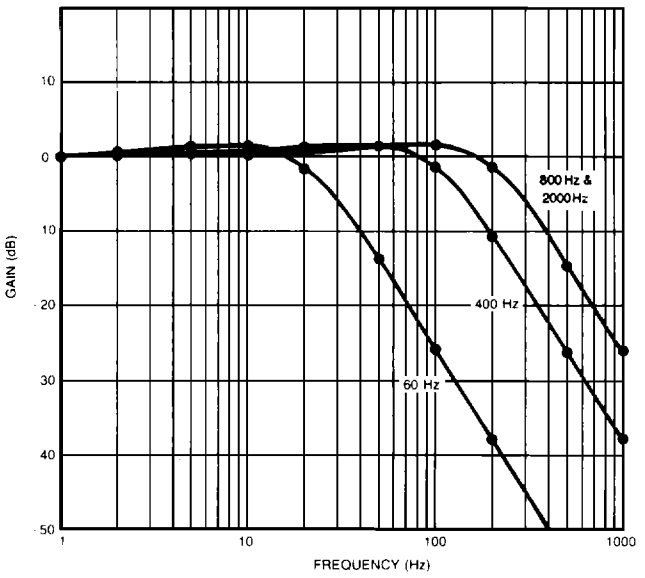


FIGURE 21 Gain Plot

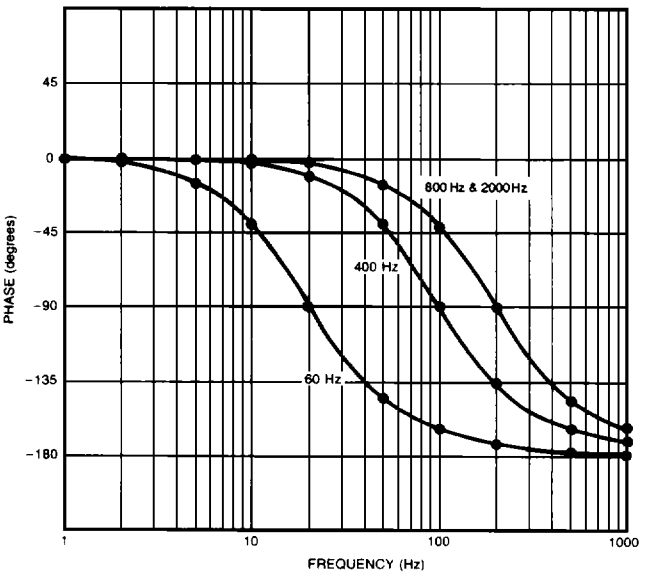
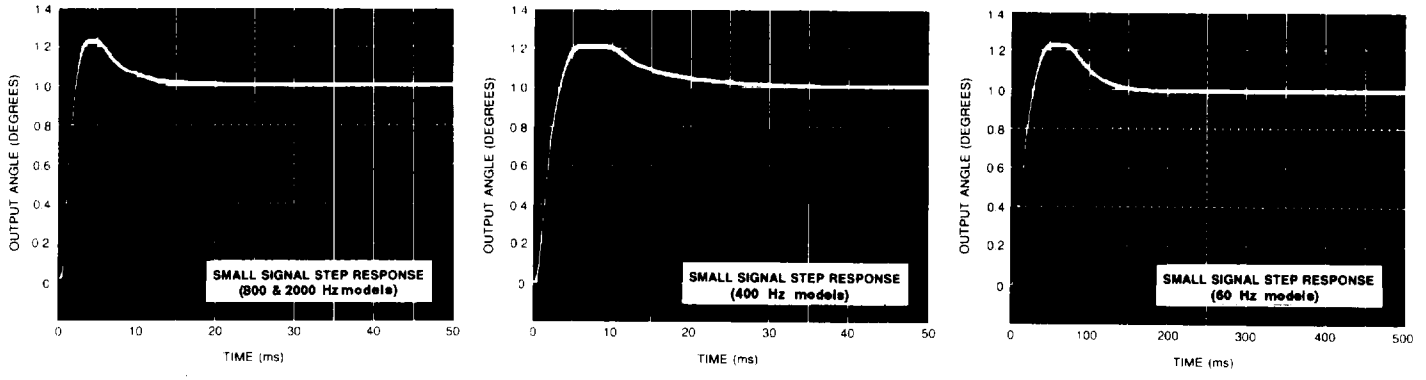


FIGURE 22 Phase Plot

Step Response

V_L = +5 V-dc, T_a = 25°C

Small Signal Input Step = 1.0 Degree



Large Signal Input Step = 179 Degrees

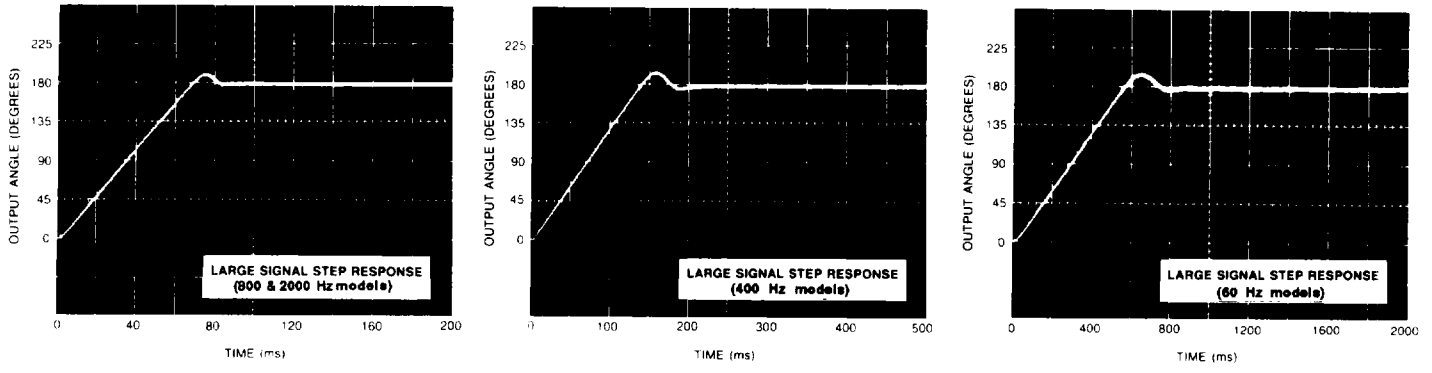
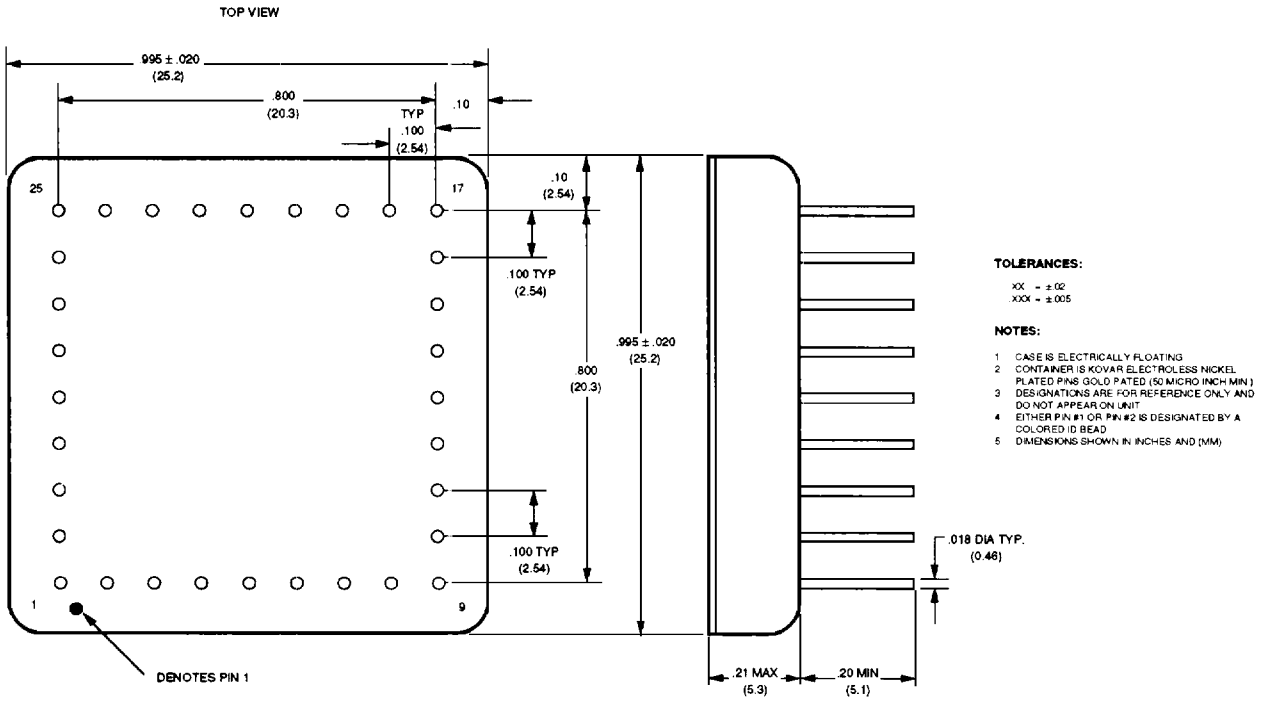


FIGURE 23 Small Signal and Large Signal Step Response



MECHANICAL OUTLINE

Ordering Information

HRD1416 - T F R A

Temperature Range
1 = 0° C to + 70° C
2 = –25° C to + 85° C
3 = –55° C to + 125° C

Frequency
2 = 2000 Hz
4 = 400 Hz
6 = 60 Hz
8 = 800 Hz

Reference Out
1 = 1.0 V-rms
5 = 0.5 V-rms

Accuracy
S = ±5.2 arc-minutes
H = ±2.6 arc-minutes
V = ±1.3 arc-minutes

Other products available from NATEL

- **3 arc-second accurate**, Programmable Dynamic Angle Simulator that includes 4 Related Instruments and is totally A.T.E. Programmable (L200).
- Hybrid (36-pin DDIP size) Synchro(Resolver)-to-Digital converters that operate from a **single +5V power supply** and offer excellent features such as BIT, AGC, low power dissipation and more (Models 1006, 1056, 1046 and 1044).
- 1.3 arc-minute accuracy, high power, Digital-to-Synchro converters that **do not require any DC power supplies** (Models 5031 and 5131).
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2036).
- **2-channel** Digital-to-Sin/Cos Converter in a single 36-pin hybrid (HDSC2036).
- **2-speed**, 22-Bit Synchro(Resolver)-to-Digital Converter, 0.0004° accuracy in a single 40-pin TDIP (HRD/HSD1626).
- **3-channel** Resolver-to-Digital Converter in a single 40-pin TDIP (HRD1346).
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106).

A wide range of applications assistance is available from Natel. Application notes can be requested when available . . . and Natel's applications engineers are at your disposal for solving specific problems.

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