Standard Products

UT54LVDS218 Deserializer

Data Sheet

October 2002

FEATURES

- 15 to 50MHz shift clock support
- 50% duty cycle on receiver output clock
- Low power consumption
- Cold sparing all pins
- ±1V common mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 1.05 Gbps throughput
- Up to 132 Megabytes/sec bandwidth
- 325 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge strobe
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 300 krad(Si) and 1 Mrad(Si)
  - Latchup immune (LET > 100 MeV-cm^2/mg)
- Packaging options:
  - 48-lead flatpack
- Standard Microcircuit Drawing 5962-01535
  - QML Q and V compliant part
- Compatible with TIA/EIA-644 LVDS standard

INTRODUCTION

The UT54LVDS218 Deserializer converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 50MHz, 21 bits of TTL data are transmitted at a rate of 350 Mbps per LVDS data channel. Using a 50 MHz clock, the data throughput is 1.05 Gbit/s (132 Mbytes/sec).

The UT54LVDS218 Deserializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

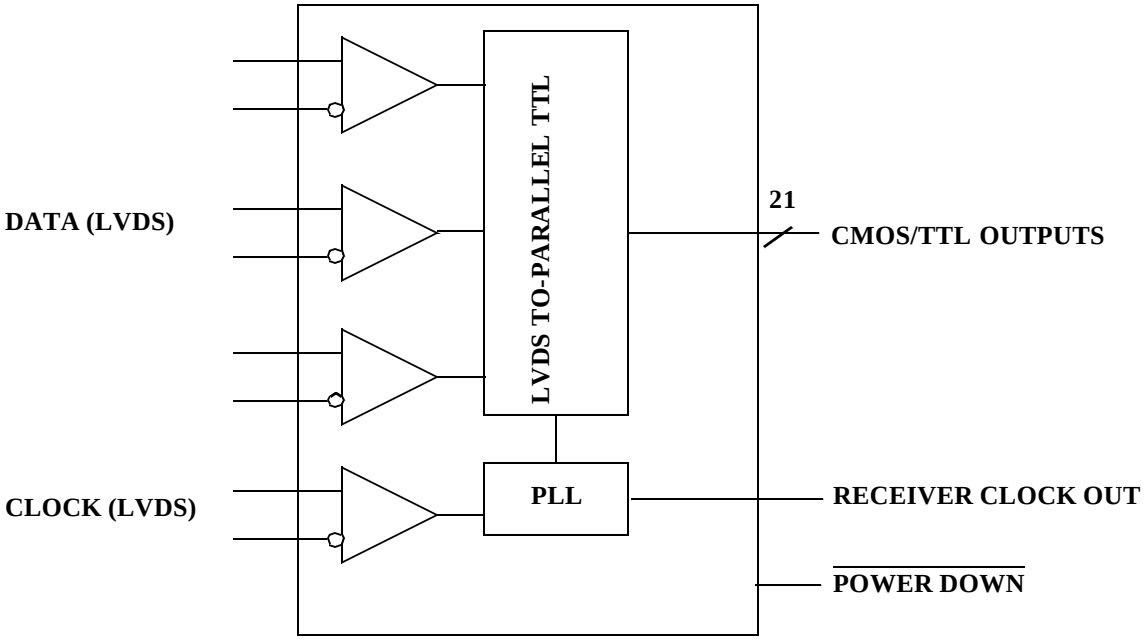


Figure 1. UT54LVDS218 Deserializer Block Diagram

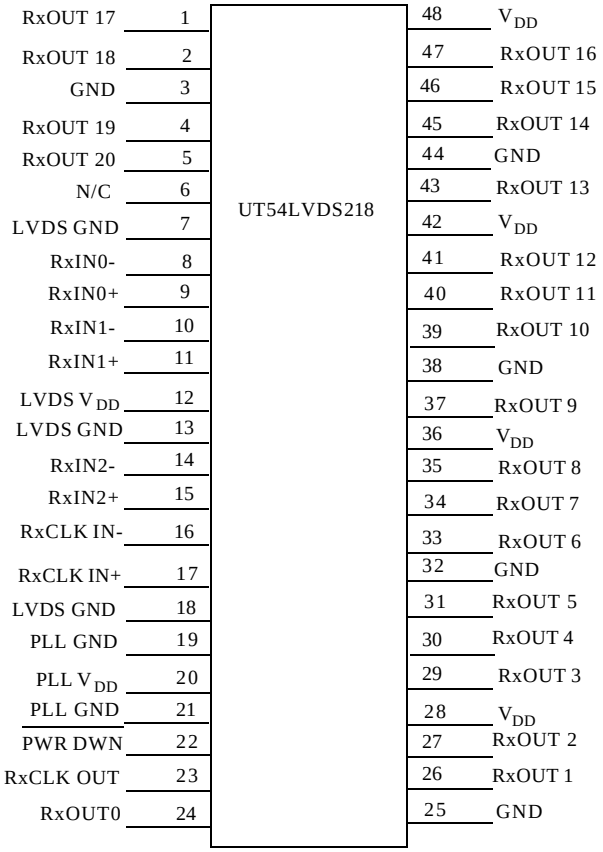


Figure 2. UT54LVDS218 Pinout

PIN DESCRIPTION

Pin Name	I/O	No.	Description
RxIN+	**I**	**3**	Positive LVDS differential data inputs[1]
RxIN-	**I**	**3**	Negative LVDS differential data output[1]
RxOUT	**O**	**21**	TTL level data outputs
RxCLK IN+	**I**	**1**	Positive LVDS differential clock input
RxCLK IN-	**I**	**1**	Negative LVDS differential clock input
RxCLK OUT	**O**	**1**	TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DWN}}$	**I**	**1**	TTL level input. When asserted (low input) the receiver outputs are low
V_{DD}	**I**	**4**	Power supply pins for TTL outputs and logic
GND	**I**	**5**	Ground pins for TTL outputs and logic
PLL V_{DD}	**I**	**1**	Power supply for PLL
PLL GND	**I**	**2**	Ground pin for PLL
LVDS V_{DD}	**I**	**1**	Power supply pin for LVDS pins
LVDS GND	**I**	**3**	Ground pins for LVDS inputs

Notes:

1. These receivers have input fail-safe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, outputs will all be HIGH; if the clock input is also floating/terminated outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

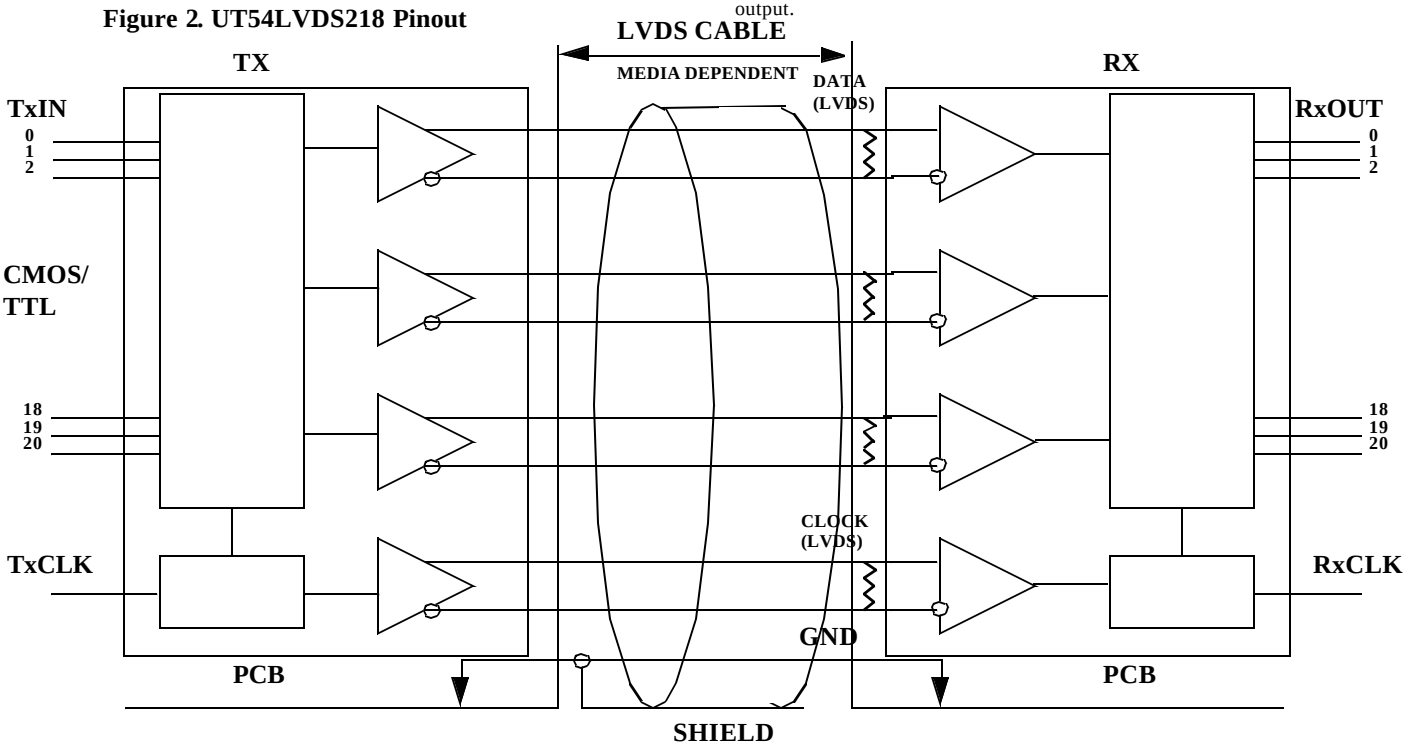


Figure 3. UT54LVDS218 Typical Application

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin	-0.3 to (V_{DD} + 0.3V)
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.25 W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	10°C/W
I_I	DC input current	±10mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.
4. For cold spare mode ($V_{DD} = V_{SS}$), $V_{I/O}$ may be -0.3V to the maximum recommended operating V_{DD} +0.3V.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS[1]

(V_{DD} = 3.0V to 0.3V; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS ($\overline{\text{PWR DWN}}$, RXOUT)					
V_{IH}	High-level input voltage		2.0	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.8	V
V_{OL}	Low-level output voltage	I_{OL} = 2mA		0.3	V
V_{OH}	High-level output voltage	I_{OL} = -0.4mA	2.7		V
I_{IH}	High-level input current	V_{IN}=3.6V; V_{DD} = 3.6V	-10	+10	µA
I_{IL}	Low-level input current	V_{IN}=0V; V_{DD} = 3.6V	-10	+10	µA
V_{CL}	Input clamp voltage	I_{CL} = -18mA		-1.5	V
I_{CS}	Cold spare leakage current	V_{IN}=3.6V; V_{DD} = V_{SS}	-20	+20	µA
I_{OS}[2, 3]	Output short circuit current	V_{OUT} = 0V	-15	-130	mA
LVDS RECEIVER DC SPECIFICATIONS (IN+, IN-)					
V_{TH}[3]	Differential input high threshold	V_{CM} = +1.2V		+100	mV
V_{TL}[3]	Differential input low threshold	V_{CM} = +1.2V	-100		mV
V_{CMR}	Common mode voltage range	V_{ID}=210mV	0.2	2.00	V
I_{IN}	Input current	V_{IN} = +2.4V, V_{DD} = 3.6V	-10	+10	µA
		V_{IN} = 0V, V_{DD} = 3.6V	-10	+10	µA
I_{CSIN}	Cold spare leakage current	V_{IN} = 3.6V, V_{DD} = V_{SS}	-20	+20	µA
Supply Current					
I_{CC}[3]	Active supply current	CL=8pF (see Figure 4)		105	mA
I_{CCPD}	Power down supply current	$\overline{\text{PWR DWN}}$ = Low, LVDS inputs = logic low		2.0	mA

Notes:

1. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
3. Guaranteed by characterization.

RECEIVER SWITCHING CHARACTERISTICS[1]

(V_{DD} = 3.0V to 3.6V; TA = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT
CLHT[3]	CMOS/TTL Low-to-High Transition Time (Figure 5)			3.5	ns
CHLT[3]	CMOS/TTL High-to-Low Transition Time (Figure 5)			3.5	ns
RSPos0[3]	Receiver Input Strobe Position for Bit 0 (Figure 10)	f=50MHz	0.59	1.33	ns
RSPos1[3]	Receiver Input Strobe Position for Bit 1 (Figure 10)	f=50MHz	3.45	4.19	ns
RSPos2[3]	Receiver Input Strobe Position for Bit 2 (Figure 10)	f=50MHz	6.30	7.04	ns
RSPos3[3]	Receiver Input Strobe Position for Bit 3 (Figure 10)	f=50MHz	9.16	9.90	ns
RSPos4[3]	Receiver Input Strobe Position for Bit 4 (Figure 10)	f=50MHz	12.02	12.76	ns
RSPos5[3]	Receiver Input Strobe Position for Bit 5 (Figure 10)	f=50MHz	14.88	15.62	ns
RSPos6[3]	Receiver Input Strobe Position for Bit 6(Figure 10)	f=50MHz	17.73	18.47	ns
RCOP[3]	RxCLK OUT Period (Figure 6)	f=50MHz	20.00	66.7	ns
RCOH[3]	RxCLK OUT High Time (Figure 6)		3.6		ns
RCOL[3]	RxCLK OUT Low Time (Figure 6)	f=50MHz	3.6		ns
RSRC[4]	RxOUT Setup to RxCLK OUT (Figure 6)	f=50MHz	3.5		ns
RHRC[4]	RxOUT Hold to RxCLK OUT (Figure 6)	f=50MHz	3.5		ns
RCCD[2]	RxCLK IN to RxCLK OUT Delay (Figure 7)	f=50MHz	3.4	8.3	ns
RRLLS	Receiver Phase Lock Loop Set (Figure 8)			10	ms
RPDD	Receiver Powerdown Delay (Figure 9)			2	µs

Notes:

1. Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and source clock jitter less than 250 ps (calculated from T_{POS} - R_{POS}) - see Figure 11.
2. Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for LVDS217 Serializer and the LVDS218 Deserializer is (T + TCCD) + 2*T + RCCD), where T = Clock period.
3. Guaranteed by characterization.
4. Guaranteed by design.

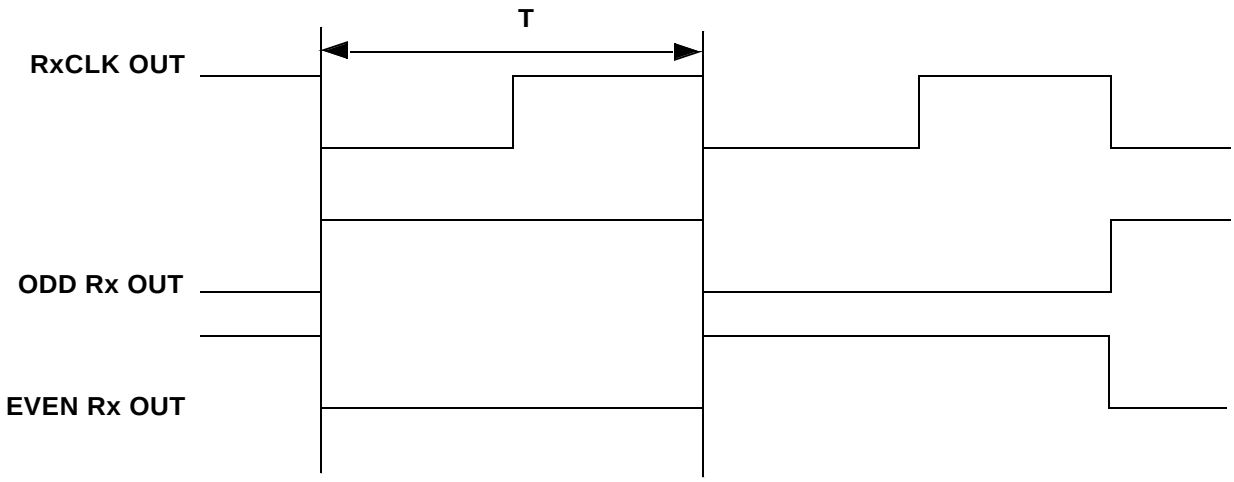


Figure 4. Test Pattern

AC TIMING DIAGRAMS

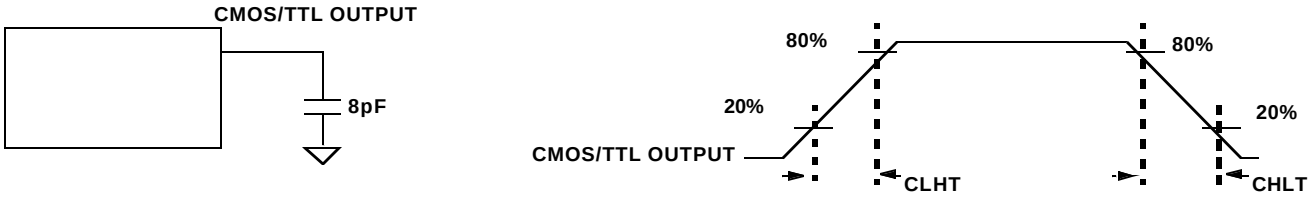


Figure 5. UT54LVDS218 Output Load and Transition Times

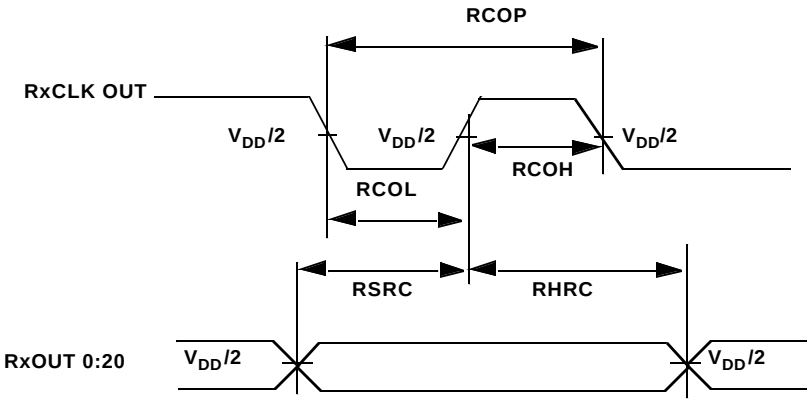


Figure 6. UT54LVDS218 Setup/Hold and High/Low Times

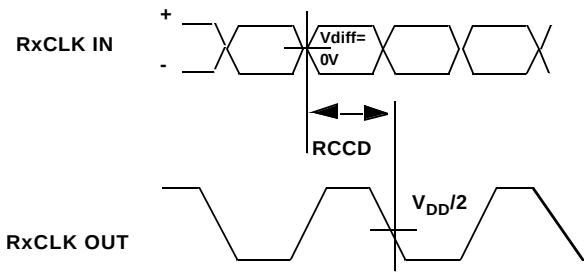


Figure 7. UT54LVDS218 Clock-to-Clock Out Delay

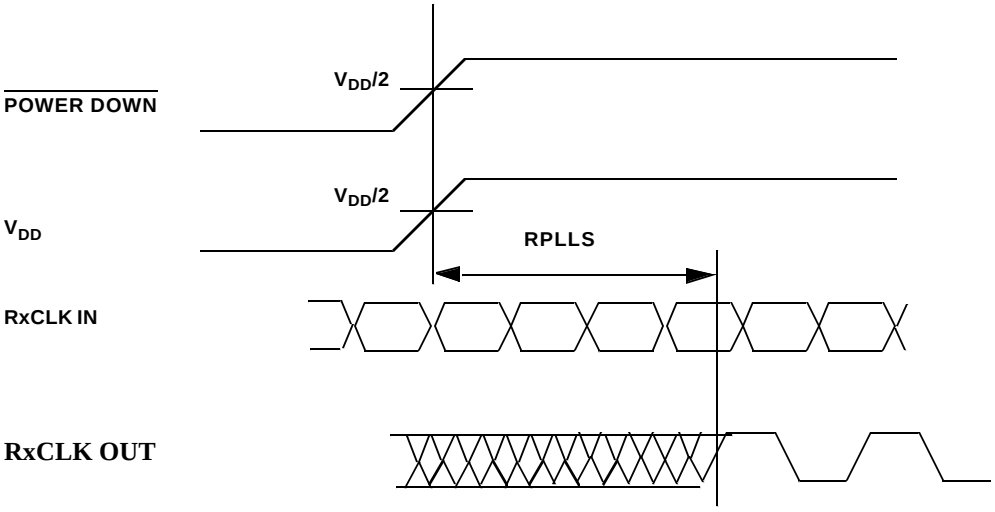


Figure 8. UT54LVDS218 Phase Lock Loop Set Time

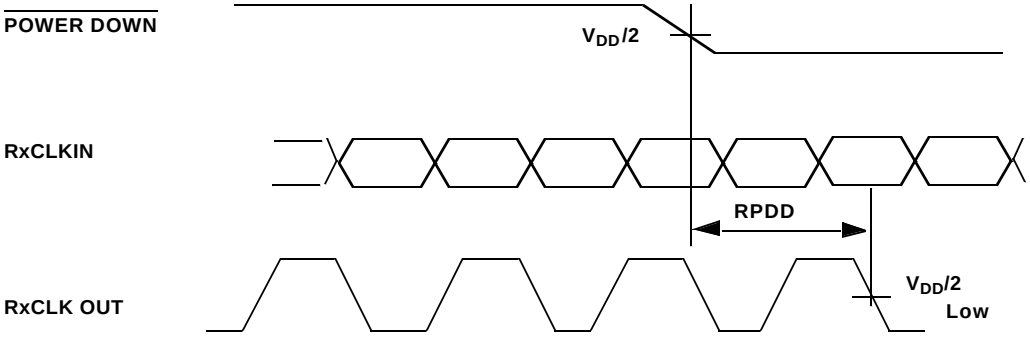


Figure 9. Receiver Powerdown Delay

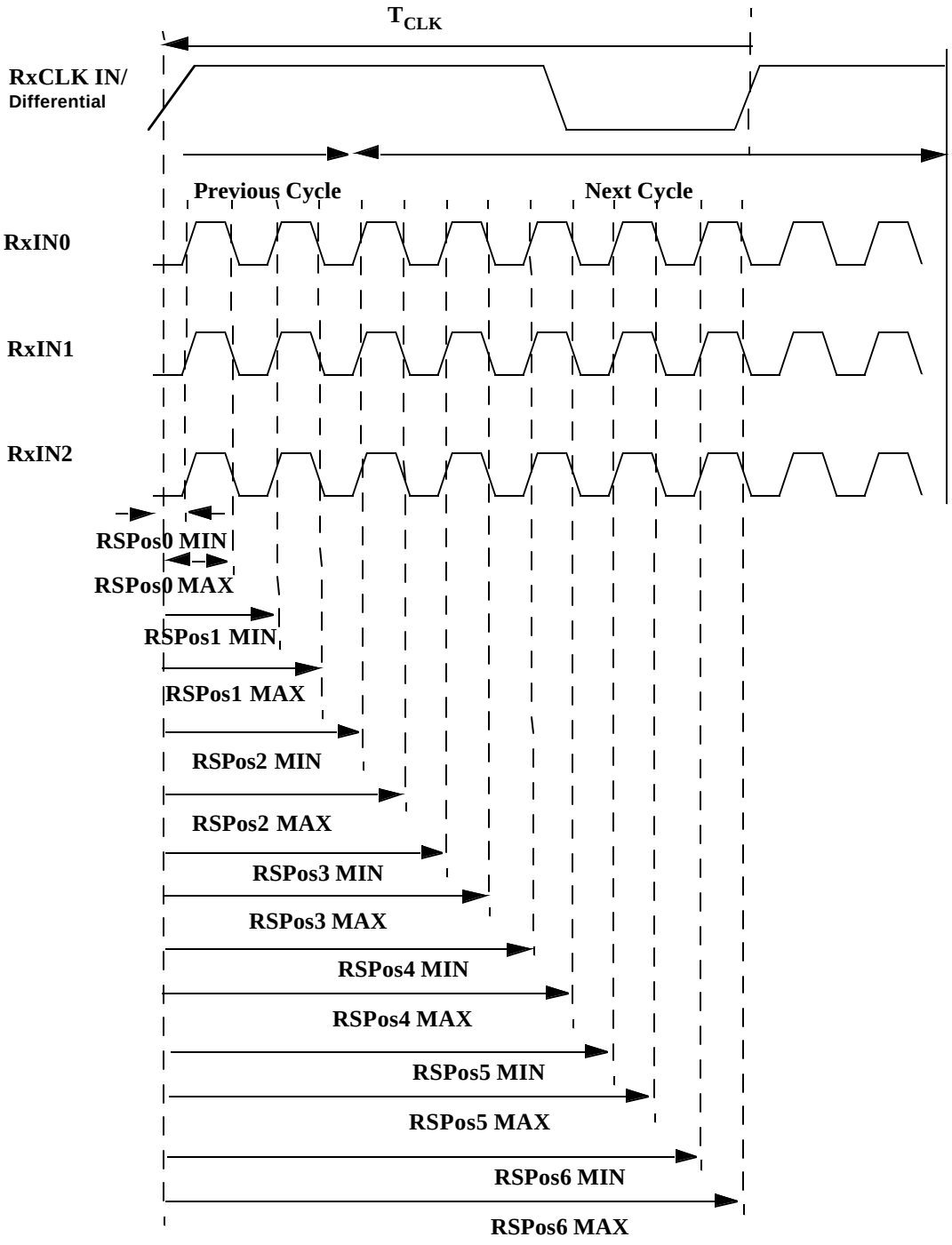
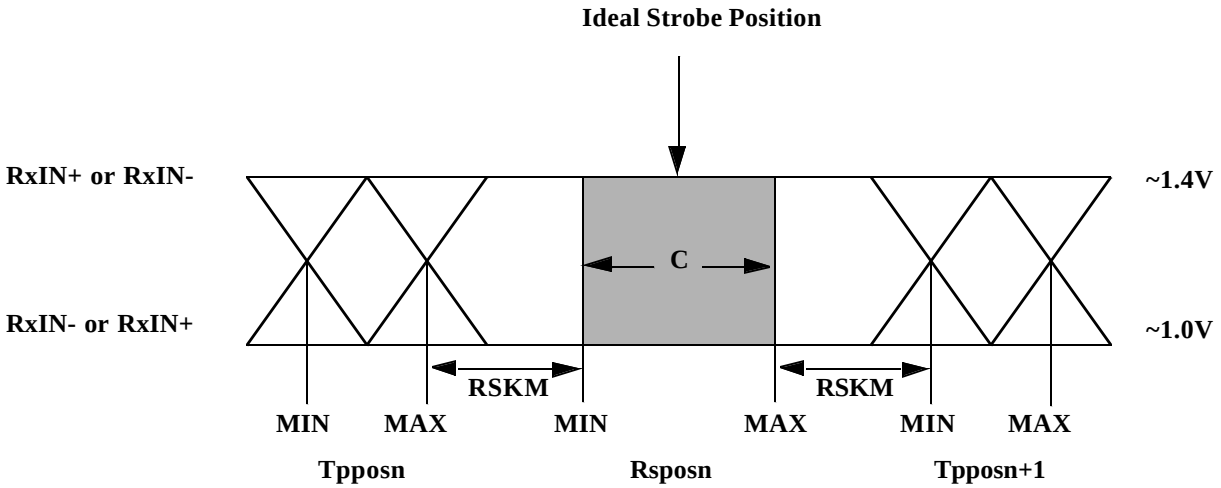


Figure 10. Receiver LVDS Input Strobe Position



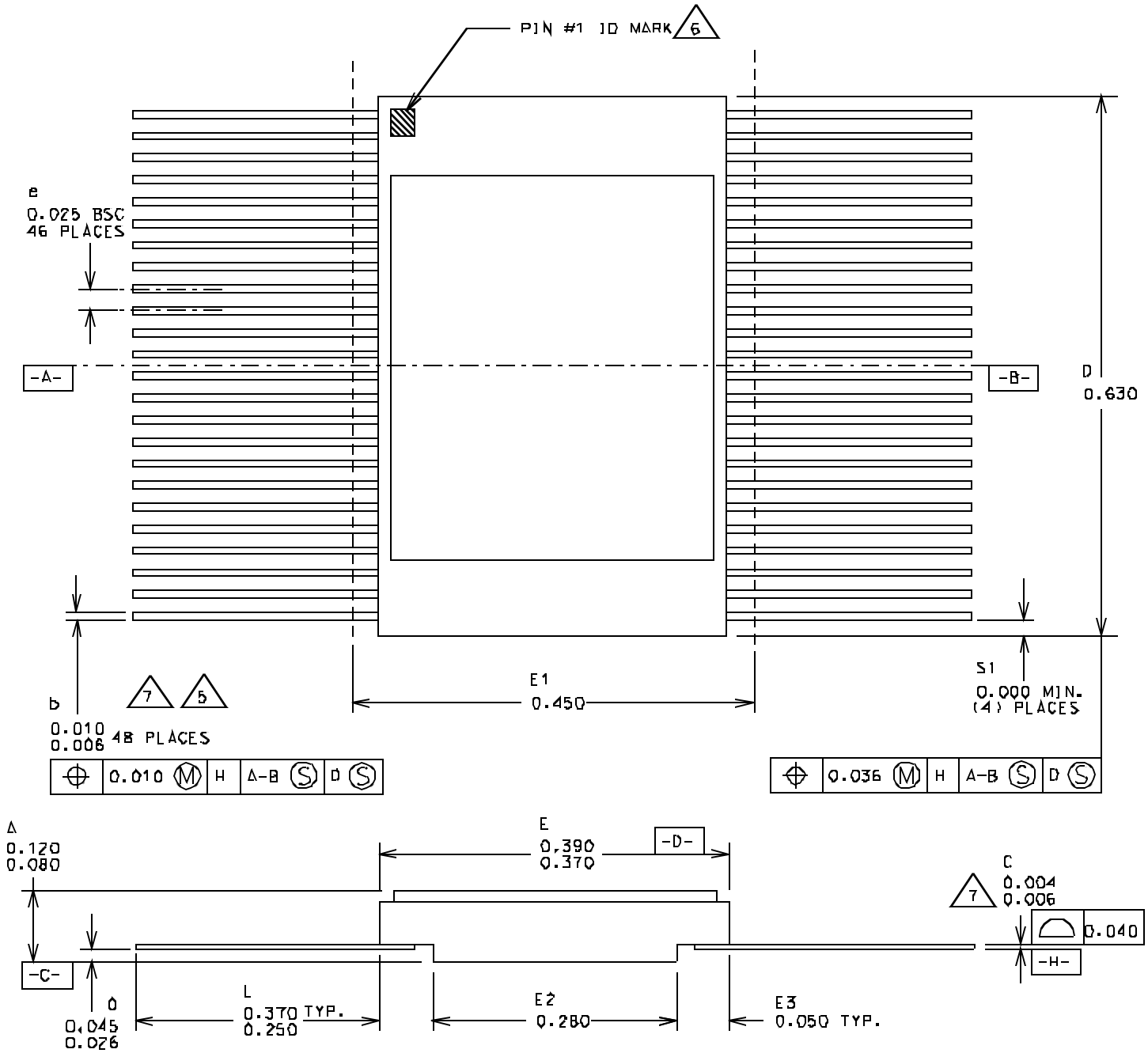
C - Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input stroke position min and max
Tspos - Transmitter output pulse position (min and max)

RSKM ≥ Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)[1] + ISI (Inter-symbol interference)[2]
Cable Skew - typically 10 ps-40 ps per foot, media dependent

Notes:
1. Cycle-to-cycle jitter is less than 250 ps at 50MHz.
2. ISI is dependent on interconnect length, may be zero.

Figure 11. Receiver LVDS Skew Margin

PACKAGING

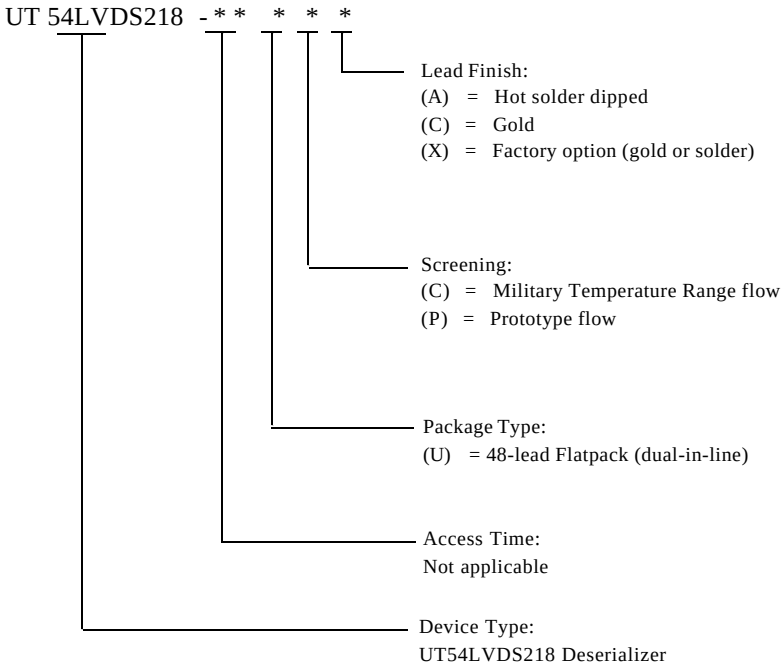


1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to VSS.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Lead position and colanarity are not measured.
5. ID mark symbol is vendor option.
6. With solder, increase maximum by 0.003.
7. Package dimensions and symbols are similar to MIL-STD-1835 variation F-19.

Figure 12. 48-Lead Flatpack

ORDERING INFORMATION

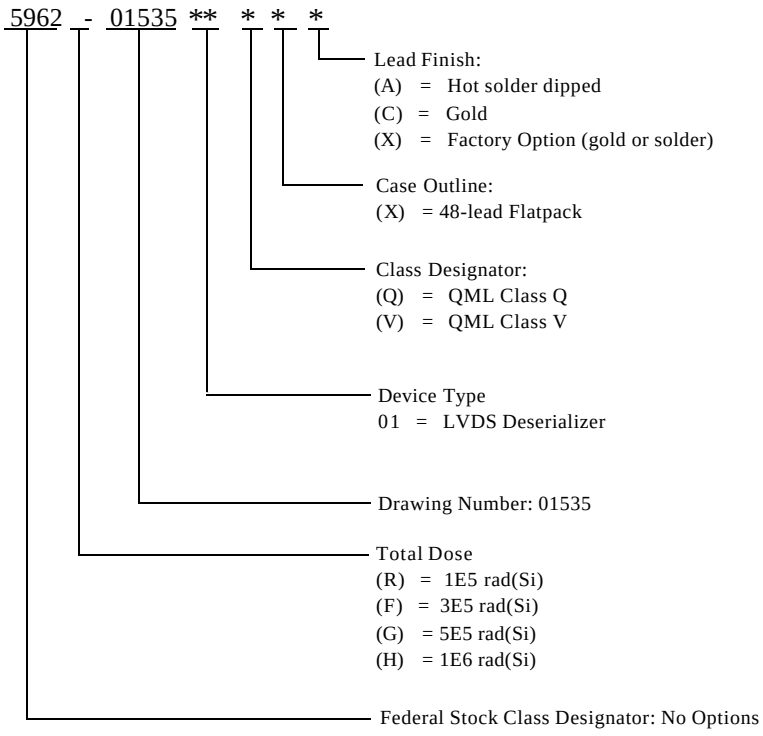
UT54LVDS218 Deserializer:



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125 °C. Radiation neither tested nor guaranteed.

UT54LVDS218 Deserializer: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.