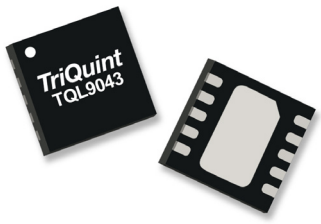
TQL9043

1500 – 2700 MHz Bypass LNA

Applications

- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

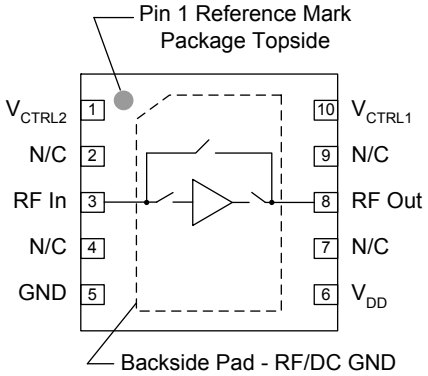


10-pin 3 x 3 mm DFN Package

Product Features

- 1500 – 2700 MHz Operational Bandwidth
- LNA With Integrated Bypass Mode
- Ability to Turn LNA and Bypass Mode OFF
- Ultra Low Noise: 0.6 dB NF
- 17.5 dB Gain
- +33 dBm Output IP3
- +41 dBm Input IP3 in Bypass Mode
- Internally Matched
- Positive Supply Only: +3.3 V to +5 V
- 3 x 3 mm 10-pin DFN Plastic Package

Functional Block Diagram



General Description

The TQL9043 is an ultra low noise, high-linearity gain block amplifier with an integrated bypass mode function. At 1900 MHz, this amplifier typically provides 17.5 dB gain, +33 dBm OIP3 and 0.6 dB noise figure while drawing 80 mA current from a +5 V supply. The TQL9043 also provides high linearity in the bypass mode with +41 dBm input IP3.

The TQL9043 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias circuit to maintain high performance over temperature.

The TQL9043 covers the 1500 – 2700 MHz frequency band and is targeted for wireless infrastructure.

The TQL9043 is available in a 3 x 3 mm DFN package and is pin compatible with the 500 – 2000 MHz TQL9042 and 1700 – 2700 MHz TQL9044.

Pin Configuration

Pin No.	Label
1	V_{CTRL2}
2, 4, 7, 9	N/C
3	RFin
5	GND
6	V_{DD}
8	RFout
10	V_{CTRL1}
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TQL9043	1500 – 2700 MHz Bypass LNA
TQL9043-PCB	Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to +150 °C
Drain Voltage (V_{DD})	+7 V
Input Power (CW)	+24 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_{DD})	+3.3	+5.0	+5.25	V
Operating Temp. Range	−40		+85	°C
T_{ch} (for>10^6 hrs MTTF)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp. = +25 °C. Tested in an unmatched 50 Ω fixture.
Input trace loss up to package pin de-embedded on noise figure data.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1500		2700	MHz
Test Frequency			1900		MHz
Gain	Bypass OFF, LNA ON	16	17.5	19	dB
Input Return Loss	Bypass OFF, LNA ON		7.2		dB
Output Return Loss	Bypass OFF, LNA ON		13		dB
Noise Figure	Bypass OFF, LNA ON		0.6	0.9	dB
Output P1dB	Bypass OFF, LNA ON		+19.4		dBm
Output IP3	Bypass OFF, LNA ON Pout=+5 dBm / tone, Δf=1 MHz	+28.5	+33		dBm
Insertion Loss	Bypass ON, LNA OFF		1.6	3.0	dB
Return Loss	Bypass ON, LNA OFF		10		dB
Input IP3	Bypass ON, LNA OFF Pin = +6.5 dBm / tone, Δf=1 MHz		+41		dBm
Isolation	LNA OFF, Bypass OFF		13.5		dB
Drain Voltage, V_{DD}			+5		V
Control Voltage, V1, V2 (1)	V_{IH}	2.4		V_{DD}	V
	V_{IL}	0		0.4	V
Current, I_D	LNA ON, Bypass OFF	40	80	120	mA
Current, I_D	Bypass ON, LNA OFF		3		mA
Switching Speed	Bypass to LNA Mode		960		ns
	LNA to Bypass Mode		76		ns
Thermal Resistance, θ_{jc}	Channel to case		44		°C/W

Notes:
1. The limits shown are true when using the external resistive divider values as shown on the TriQuint app board.

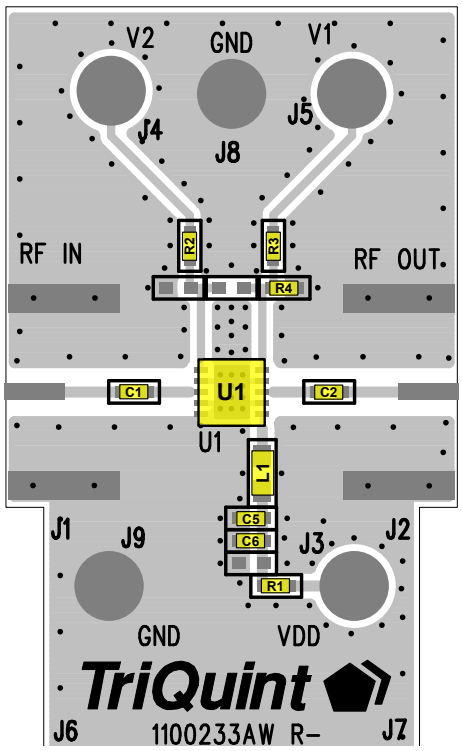
Control Truth Table

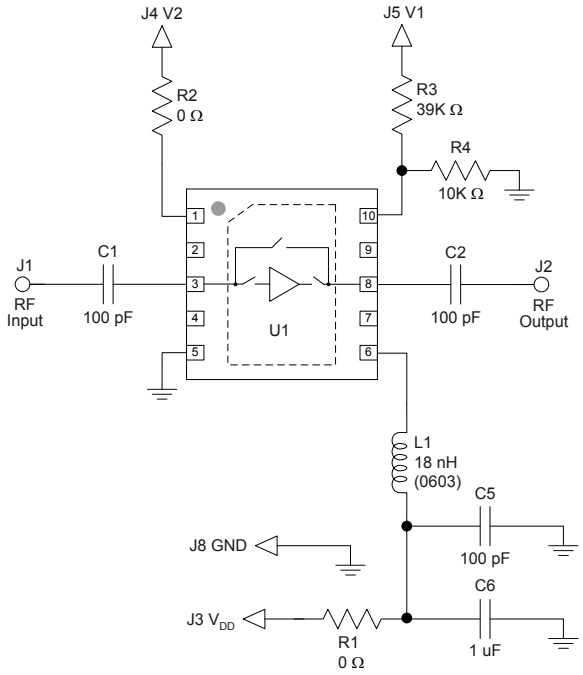
V_{CTRL2}	V_{CTRL1}	State
Low	High	LNA OFF, Bypass OFF
High	High	LNA OFF, Bypass ON
Low	Low	LNA ON, Bypass OFF
High	Low	Reserved (Do not use)

Control Voltage Limits (at device pins)

	State	Bias Condition
V_{CTRL1}	Low	≤ 0.1 V
	High	≥ 0.52 V
V_{CTRL2}	Low	≤ 0.4 V
	High	≥ 1.3 V

TQL9043-PCB Evaluation Board





Bill of Material – TQL9043-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Bypass LNA	TriQuint	TQL9043
C1, C2, C3, C4, C5	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C6	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	
R1, R2	0 Ω	RES, 0402, +/-5%, 1/10W	various	
R3	39K	RES, 0402, +/-5%, 1/10W	various	
R4	10K	RES, 0402, +/-5%, 1/10W	various	
L1	18 nH	IND, 0603, +/-5%	Coilcraft	0603CS-18NXJL

Power-up and Power-down Sequencing

		V_{DD}	V_{CTRL1} & V_{CTRL2}
LNA ON, Bypass OFF	Power-up	1st	2nd
	Power-down	1st	2nd
LNA OFF, Bypass ON	Power-up	1st	2nd
	Power-down	1st	2nd

Typical Performance (LNA Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_D = 80 mA, Temp. = +25 °C.
Input trace loss de-embedded in noise figure data.

Parameter	Typical Value			Units
Frequency	1700	1900	2100	MHz
Gain	18.4	17.5	16.6	dB
Noise Figure	0.55	0.59	0.65	dB
Input Return Loss	6.8	7.1	7.2	dB
Output Return Loss	13.2	13	13	dB
Output P1dB	+19.5	+19.4	+19.6	dBm
OIP3 (Pout / tone = +5 dBm, Δf = 1 MHz)	+33.2	+33	+33	dBm

Typical Performance (Bypass Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_D = 3 mA, Temp. = +25 °C.

Parameter	Typical Value			Units
Frequency	1700	1900	2100	MHz
Insertion Loss	1.6	1.8	1.9	dB
Input Return Loss	9	8.5	8.2	dB
Output Return Loss	10.4	10	9.8	dB
Input IP3 (Pin / tone = +6.5 dBm, Δf = 1 MHz)	+40.7	+40.8	+40.8	dBm

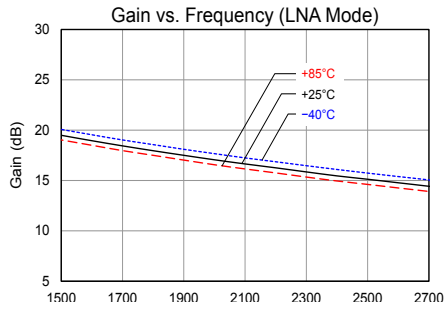
Typical Performance (LNA OFF, Bypass OFF Mode)

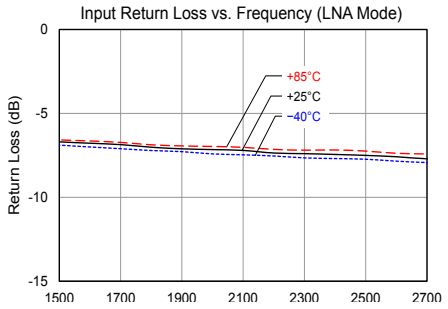
Test conditions unless otherwise noted: V_{DD} = +5 V, Temp. = +25 °C.

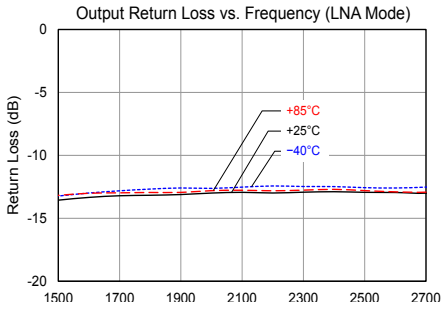
Parameter	Typical Value			Units
Frequency	1700	1900	2100	MHz
Isolation	12.7	13.5	14	dB

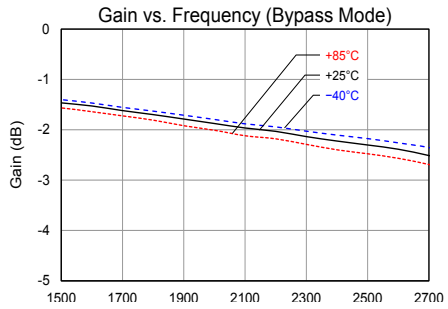
Performance Plots

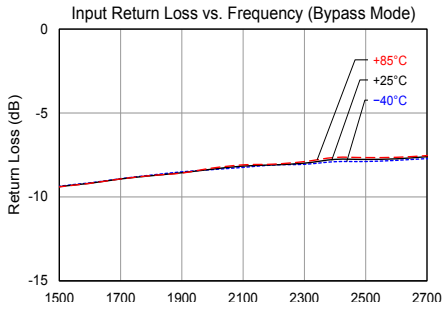
Test conditions unless otherwise noted: V_{DD} = +5 V, I_D = 80 mA

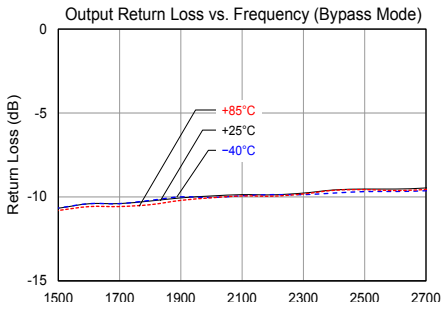


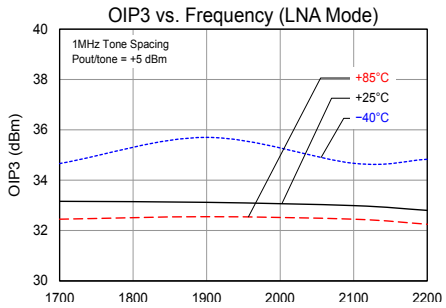


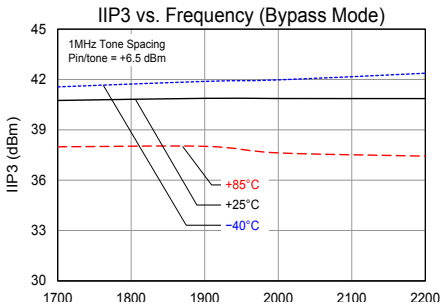


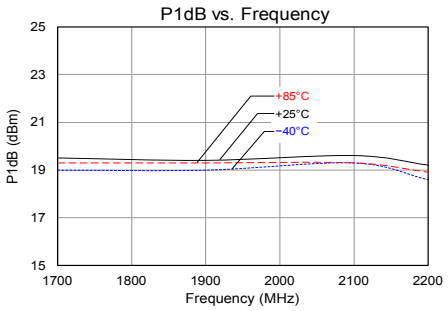


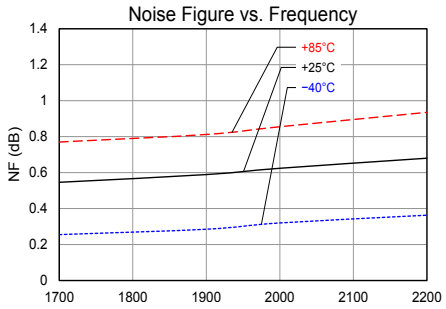


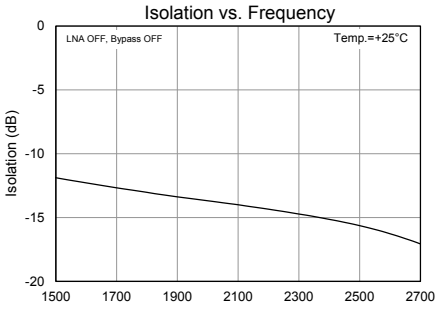




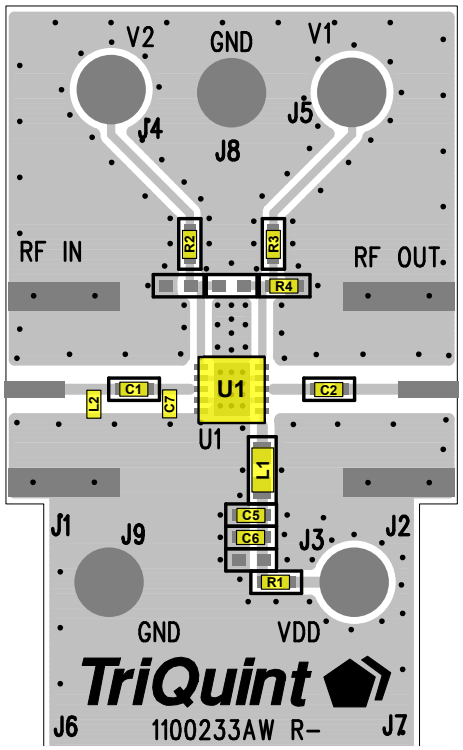


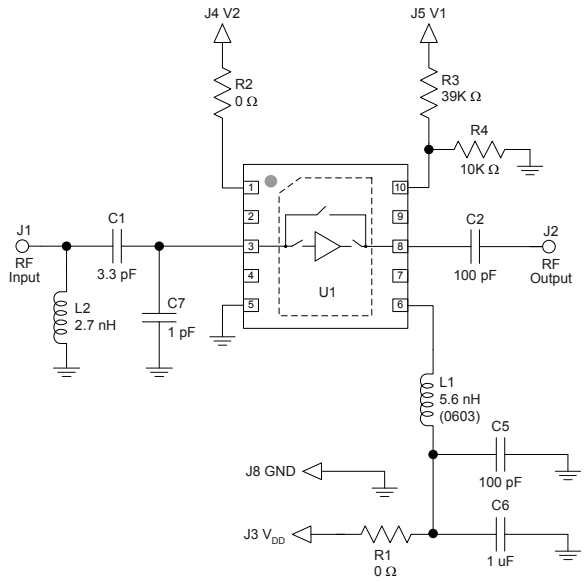






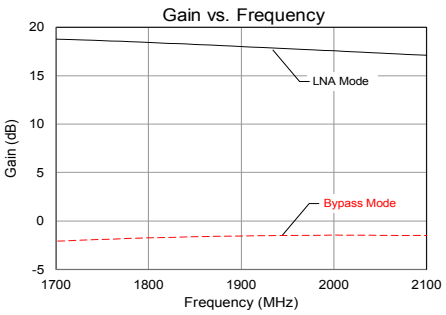
Reference Design – Optimized Return Loss

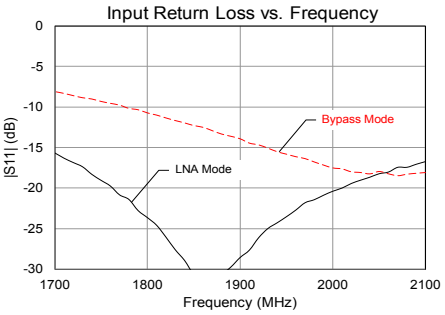


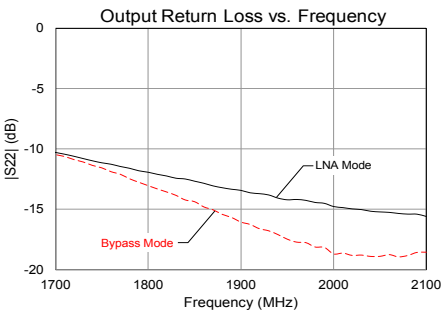


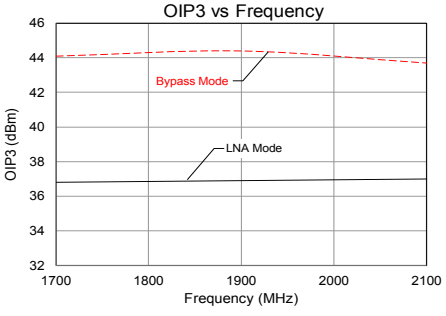
Performance Plots

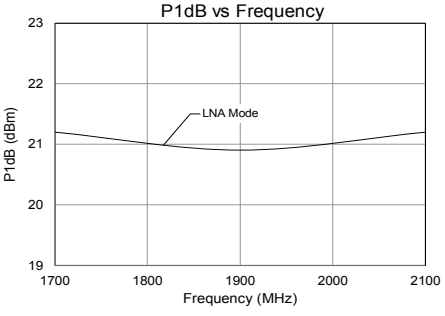
Test conditions unless otherwise noted: V_{DD} = +5 V, I_D = 80 mA

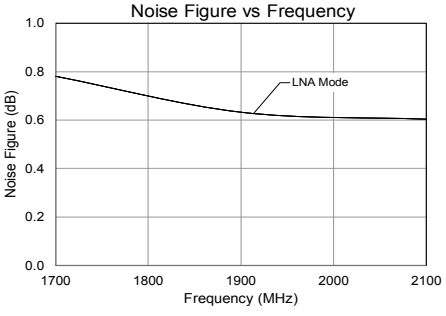










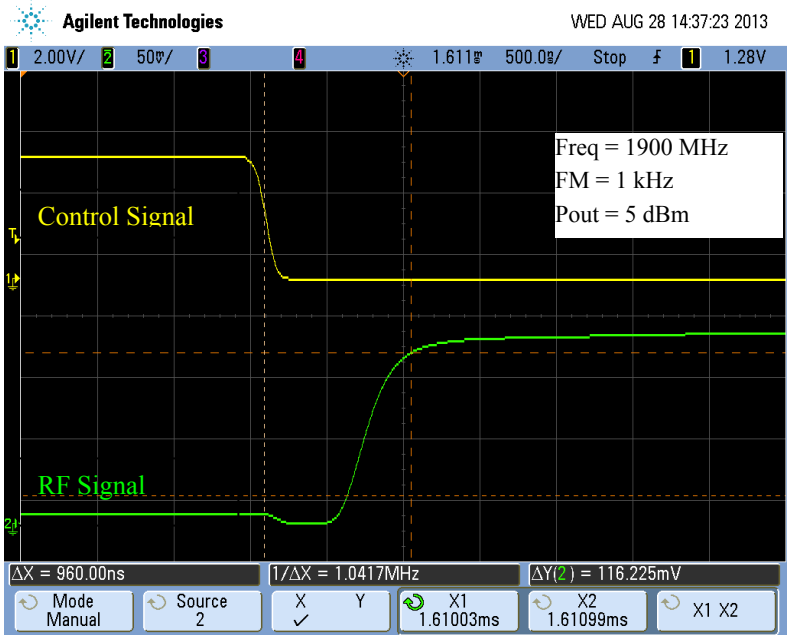


Switching Speed

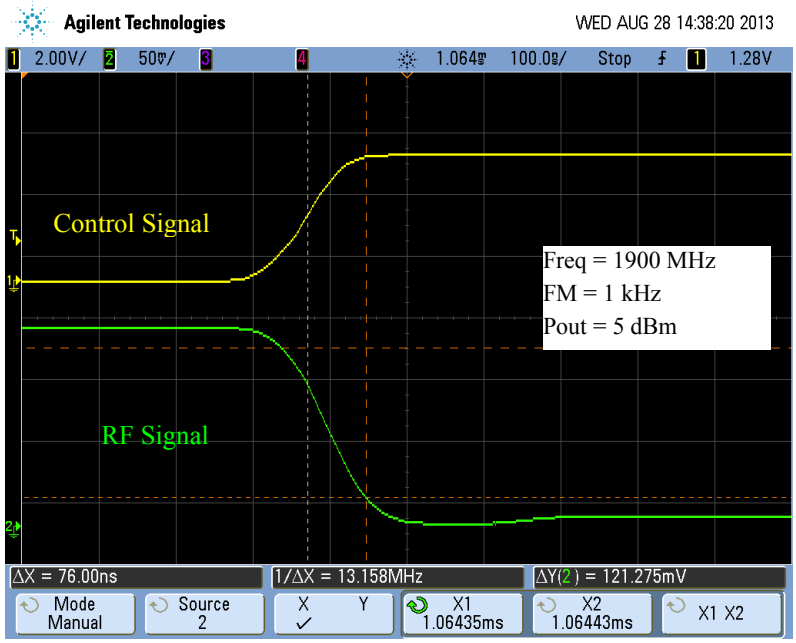
Switching Speed Measurement on TriQuint Application Board

Transition	Measurements	Units
Bypass to LNA mode (50% V1/V2 – 10% RF)	960	ns
LNA to Bypass mode (50% V1/V2 – 90% RF)	76	ns

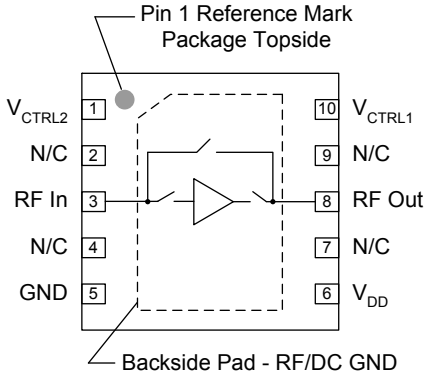
Bypass to LNA mode (50% V1/V2 – 10% RF)



LNA to Bypass mode (50% V1/V2 – 90% RF)



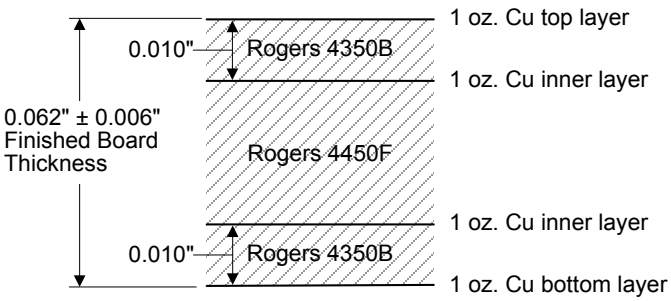
Pin Configuration and Description



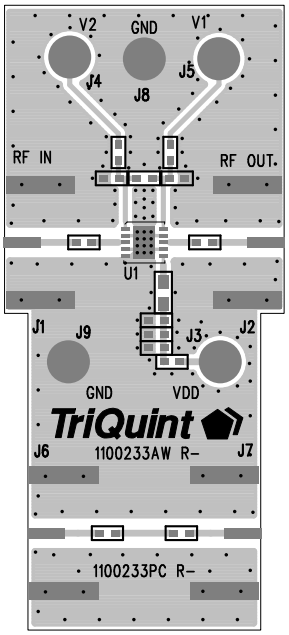
Pin No.	Label	Description
1	V_{CTRL2}	Control pin for bypass mode and LNA mode. Internal resistor divider. Refer to truth table.
2, 4, 7, 9	N/C	No internal connection. These pins can be grounded to provide PCB mounting integrity.
3	RFin	RF input pin. DC block required.
5	GND	RF/DC Ground pin.
6	V_{DD}	Supply voltage pin.
8	RFout	RF output pin. DC block required.
10	V_{CTRL1}	Control pin for bypass mode and LNA mode. Requires external resistor divider. Refer to truth table.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

TriQuint PCB 1100233 Material and Stack-up



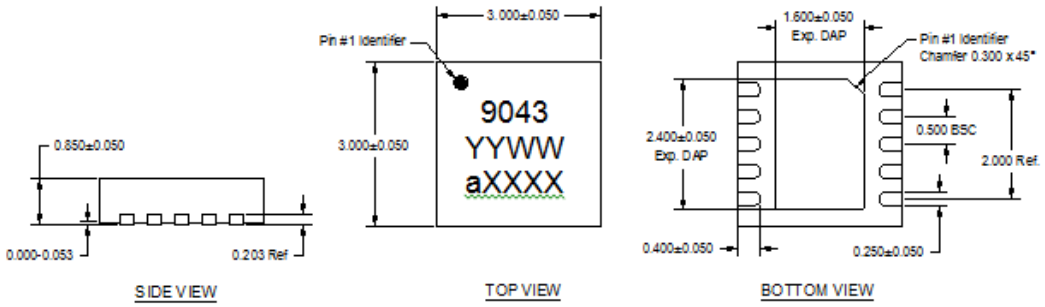
50 ohm line dimensions: width = .020”, spacing = .032”



Mechanical Information

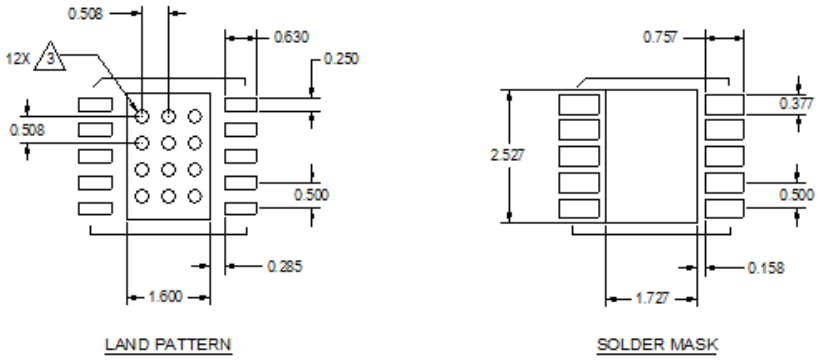
Package Marking and Dimensions

Marking: Part number – 9043
Year/Week – YYWW
Lot Code – aXXXX



1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥250V to 500V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class C3
Value: >1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C maximum reflow temperature) and tin/lead (245 °C maximum reflow temperature) soldering processes.

Package contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@triquint.com **Fax:** +1.503.615.8902

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Email: sjcapplications.engineering@triquint.com

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