

# UTR 0.8 $\mu$ Gate Array Family



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## FEATURES

- ❑ Up to 200,000 usable equivalent gates
- ❑ Clock rates up to 180 MHz
- ❑ Advanced 0.8 $\mu$  radiation-hardened silicon gate CMOS
- ❑ Operating voltage of 5V
- ❑ QML Class Q & V compliant
- ❑ Designed specifically for high reliability applications
- ❑ Radiation-hardened to 1.0E6 rads(Si) total dose (functional) and SEU-immune cells to less than 1.0E-10 errors/bit-day
- ❑ JTAG (IEEE 1149.1) boundary-scan registers built into I/O cells
- ❑ Low noise package technology for high speed circuits
- ❑ Design support using Mentor Graphics®, Synopsys™ and VHDL tools on HP® and Sun® workstations
- ❑ Standard Microcircuit Drawing pending

## PRODUCT DESCRIPTION

The high-performance UTR 0.8 $\mu$  gate array family features densities of up to 200,000 equivalent gates and is available in MIL-PRF-38535 QML Q and V quality levels and radiation-hardened.

For those designs requiring stringent radiation hardness, UTR's 0.8 $\mu$  process employs a special processing module that enhances the total dose radiation hardness of the field and gate oxides while maintaining circuit density and reliability. In addition, for both greater transient radiation-hardness and latchup immunity, the UTR 0.8 $\mu$  process is built on epitaxial substrate wafers.

Developed from UTMC's patented architectures, the UTR 0.8 $\mu$  array family uses a highly efficient continuous transistor architecture for the internal cell construction. Combined with state-of-the-art placement and routing tools, the utilization of available transistors is maximized using three levels of metal interconnect.

The UTR 0.8 $\mu$  family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX equivalent functions, as well as, configurable RAM and other megafunc-tions. UTMC's megacell library includes the following functions:

- Intel 80C31® equivalent
- MIL-STD-1553 functions (BRCTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- RISC microcontroller
- Configurable RAM

**Table 1. Gate Densities**

DEVICE PART NUMBERS <sup>1</sup>	EQUIVALENT USABLE GATES <sup>2</sup>	SIGNAL I/O <sup>3</sup>	POWER & GROUND PADS <sup>4</sup>
UTR25	5,000 - 25,000	175	40
UTR35	35,000	175	40
UTR50	50,000	175	40
UTR75	75,000	256	80
UTR100	125,000	256	80
UTR150	150,000	256	80
UTR200	200,000	256	80

**Notes:**

1. The "R" denotes radiation-hardened.
2. Based on NAND2 equivalents. Actual usable gate count is design-dependent. Estimates reflect a mix of functions including RAM.
3. Includes five pins that may or may not be reserved for JTAG boundary-scan, depending on user requirements.
4. Reserved for dedicated  $V_{DD}/V_{SS}$  and  $V_{DDQ}/V_{SSQ}$ .

**Low-noise Device and Package Solutions**

The UTR 0.8 $\mu$  output drivers feature programmable slew rate control for minimizing noise and switching transients. This feature allows the user to optimize edge characteristics to match system requirements. Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, UTMC offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring built-in isolated power and ground planes. These planes provide lower overall resistance/inductance through power and ground

paths which minimize voltage drops during periods of heavy switching. These isolated planes also help sustain supply voltage during dose rate events, thus preventing rail span collapse.

Flatpacks are available with up to 304 leads; PGAs are available with up to 280 leads. UTMC's flatpacks feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations. In addition to the packages listed in Table 2, UTMC offers custom package development and package tooling modification services for individual requirements.

**Table 2. Packages**

PACKAGE TYPE/LEADCOUNT <sup>1</sup>	UTR25	UTR35	UTR50	UTR75	UTR100	UTR150	UTR200
<b>Flatpack</b>							
84	X	X	X				
132	X	X	X				
172	X	X	X	X	X	X	X
196	X	X	X	X	X	X	X
224				X	X	X	X
256				X	X	X	X
304				X	X	X	X
<b>PGA<sup>2</sup></b>							
84	X	X	X				
120				X	X	X	X
144	X	X	X				
208	X	X	X	X	X	X	X
280				X	X	X	X

**Notes:**

1. The number of device I/O pads available may be restricted by the selected package.
2. PGA packages have one additional non-connected index pin (i.e., 144 + 1 index pin = 145 total package pins for the 144 PGA). Contact UTMC for specific package drawings.

### **Extensive Cell Library**

The UTR 0.8 $\mu$  family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX-equivalent functions, as well as, RAM and other megafunctions. User-selectable options for cell configurations include scan for all register elements, as well as output drive strength. UTMC's megacell library includes the following functions:

- Intel® 80C31 equivalent
- MIL-STD-1553 functions (BCRTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- Standard microprocessor peripheral functions
- Configurable RAM

Refer to UTMC's UTR 0.8 $\mu$  Design Manual for complete cell listing and details.

### **I/O Buffers**

The UTR 0.8 $\mu$  gate array family offers up to 342 device pad locations (note: device pad availability is affected by package selection and pinout.) The I/O cells can be configured by the user to serve as input, output, bidirectional, three-state, or additional power and ground pads. Output drive options range from 2 to 8mA. To drive larger off-chip loads, output drivers can be combined in parallel to provide additional drive up to 12mA.

Other I/O buffer features and options include:

- Slew rate control
- Pull-up and pull-down resistors
- TTL, CMOS, and Schmitt levels
- Built-in boundary-scan

### **JTAG Boundary-Scan**

The UTR 0.8 $\mu$  arrays include a test access port and boundary-scan architecture that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits this capability offers include the following:

- Allows easy test of complex assembled printed circuit boards
- Can be used to gain access to and control internal scan paths
- Can be used to initiate Built-In Self Test

### **Clock Driver Distribution**

UTMC design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

### **Speed and Performance**

UTMC specializes in high-performance circuits designed to operate in harsh military and radiation environments. Table 3 presents a sampling of typical cell delays.

Note that the propagation delay for a CMOS device is a function of its fanout loading, supply voltage, operating temperature, and processing tolerance. In a radiation environment, additional performance variances must be considered. The UTR 0.8 $\mu$  simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

### **Power Dissipation**

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. The radiation-hardened processes exhibit power dissipation that is typical of CMOS processes. For a rigorous power estimating methodology, refer to the UTMC UTR 0.8 $\mu$  Design Manual or consult with a UTMC Applications Engineer.

**Table 3. Typical Cell Delays**

<b>CELL</b>	<b>OUTPUT TRANSITION</b>	<b>PROPAGATION DELAY <sup>1</sup></b>
<b>Internal Gates</b>		
INV1, Inverter	HL	0.26
	LH	0.39
INV4, Inverter 4X	HL	0.14
	LH	0.23
NAND2, 2-Input NAND	HL	0.35
	LH	0.39
NOR2, 2-Input NOR	HL	0.25
	LH	0.61
DFF	CLK to Q	1.53
Latch	Enable to Q	1.45
<b>Output Buffers</b>		
O8N19, CMOS	HL	3.22
	LH	2.33
O4N10, TTL Scan, 4mA	HL	5.92
	LH	4.01
OTN10, TTL Scan, 12mA	HL	3.76
	LH	3.14
<b>Input Buffers</b>		
ICN19, CMOS	HL	.597
	LH	.482
ITN19, TTL	HL	.787
	LH	.735

**Note:**

1. All specifications in ns (typical). Output load capacitance is 50pF. Fanout loading for input buffers and gates is the equivalent of two gate input loads.

**ASIC DESIGN SOFTWARE**

Using a combination of state-of-the-art third-party and proprietary design tools, UTMC delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

**DESIGN CREATION**

UTMC’s flexible design creation methodology supports high level design by providing UTR 0.8µ cell libraries for synthesis. Using Mentor Graphics and Synopsys synthesis tools, a structural design can be created for verification in VITAL-compliant VHDL or the Mentor Graphics environment. UTMC’s cell libraries also support Automatic Test Program Generation (ATPG) to improve design testing.

**DESIGN ANALYSIS**

UTMC’s design analysis tools check the integrity of the design and ensure that it can be manufactured in UTMC processes. Design analysis tools include:

DESIGN ANALYSIS TOOL	FUNCTION
Logic Rules Checker	Makes sure the design meets connectivity rules
Tester Rules Checker	Makes sure the design can be tested on UTMC testers
Design Transfer Tool	Allows accurate transfer of design data to UTMC

**TOOLS SUPPORTED BY UTMC**

MENTOR GRAPHICS	SYNOPSYS	VHDL
AutoLogicII®	Design Compiler™	Synopsys VSS™
QuickSimII®	VHDL Compiler™	Mentor Graphics Quick-HDL®
QuickFault II®	TestSim™	Cadence Leapfrog®
QuickGradeII®	Verilog HDL Compiler™	Viewlogic Vantage™
FastScan ®/ FlexTest® / DFT Advisor®	Test Compiler Plus™	Any VITAL-compliant VHDL tool

**XDT<sup>SM</sup> (EXTERNAL DESIGN TRANSLATION)**

Through UTMC’s XDT services, customers can convert an existing non-UTMC design to UTMC’s processes. The XDT tool is particularly useful for converting an FPGA to a UTMC radiation-hardened gate array. The XDT translation tools convert industry standard netlist formats and vendor libraries to UTMC formats and libraries. Industry standard netlist formats supported by UTMC include:

- VHDL
- Verilog HDL™
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

## PHYSICAL DESIGN

Using three layers of metal interconnect, UTMC achieves optimized layouts that maximize speed of critical nets, overall chip performance, and design density up to 200,000 equivalent gates.

### Test Capability

UTMC supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation, and fault grading. Scan design options are available on all UTR 0.8 $\mu$  storage elements. In addition, all UTR 0.8 $\mu$  arrays feature JTAG boundary-scan (per IEEE Standard 1149.1). Automatic test program development capabilities handle large vector sets for use with UTMC's LTX/Trillium MicroMasters, supporting high-speed testing (up to 80MHz with pin multiplexing).

### Unparalleled Quality and Reliability

UTMC is dedicated to satisfying the demanding quality and reliability requirements of aerospace and defense systems suppliers. Quality assurance and reliability programs are integrated into the entire manufacturing process with Statistical Process Control (SPC) fully implemented for all manufacturing operations. These high quality standards have enabled UTMC to offer product in accordance with:

- MIL-PRF-38535, QML Q and V
- ISO-9001
- Other enhanced reliability flows

Because of numerous product variations permitted with customer specific designs, much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). Thus, UTMC can assure high reliability prior to delivery of product to the customer.

## Radiation Hardened

UTMC incorporates radiation-hardening techniques in process design, design rules, array design, power distribution, and library element design. All key radiation-hardening process parameters are controlled and monitored using statistical methods and in-line testing.

PARAMETER	RADIATION HARD	NOTES
Total dose	1.0E6 rads(Si) functional	1
Dose rate upset	1.0E9 rads(Si)/sec	2
Dose rate survivability	1.0E12 rads(Si)/sec	3
SEU	<1.0E-10 errors per cell-day	3,4
Projected neutron fluence	1.0E14 n/sq cm	
Latchup	Latchup-immune over specified use conditions	

### Notes:

1. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019. Data sheet electrical characteristics guaranteed to 1.0E6 rads(Si). All post-radiation values measured at 25°C;  $I_{DDQ}$  post-rad limit = 4mA.
2. Short pulse 20ns FWHM (full width, half maximum).
3. May be design dependent, SEU limit based on standard evaluation circuit.
4. SEU-hard flip-flop cell. Non-hard flip-flop typical is 5E-8.

## ABSOLUTE MAXIMUM RATINGS <sup>1</sup>

(Referenced to  $V_{SS}$ )

SYMBOL	PARAMETER	LIMITS
$V_{DD}$	DC supply voltage	-0.3 to 7.0V
$V_{IO}$	Voltage on any pin	-0.3V to $V_{DD} + 0.3$
$T_{STG}$	Storage temperature	-65 to +150°C
$T_J$	Maximum junction temperature	+175°C
$I_{LU}$	Latchup immunity	$\pm 150$ mA
$I_I$	DC input current	$\pm 10$ mA
$T_{LS}$	Lead temperature (soldering 5 sec)	+300°C

### Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
$V_{DD}$	Positive supply voltage	4.5 to 5.5V
$T_C$	Case temperature range	-55 to +125C
$V_{IN}$	DC input voltage	0V to $V_{DD}$

## DC ELECTRICAL CHARACTERISTICS

( $V_{DD} = 5.0V \pm 10\%$ ;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$V_{IL}$	Low-level input voltage <sup>1</sup> TTL inputs CMOS, OSC inputs				0.8 .3 $V_{DD}$	V
$V_{IH}$	High-level input voltage <sup>1</sup> TTL inputs CMOS, OSC inputs		2.2 .7 $V_{DD}$			V
$V_{T+}$	Schmitt Trigger, positive going <sup>1</sup> threshold				4.0	V
$V_{T-}$	Schmitt Trigger, negative going <sup>1</sup> threshold		1.0			V
$V_H$	Schmitt Trigger, typical range of hysteresis <sup>2</sup>		1.5		2.0	V
$I_{IN}$	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors, OSC Inputs with pull-up resistors Inputs with pull-up resistors, OSC	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{DD}$	-1 +150 -10 -900 -10		1 +900 +10 -150 +10	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup> TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	$I_{OL} = 2.0mA$ $I_{OL} = 4.0mA$ $I_{OL} = 8.0mA$ $I_{OL} = 12.0mA$ $I_{OL} = 1.0\mu A$ $I_{OL} = 100\mu A$ $I_{OL} = 100\mu A$			0.4 0.4 0.4 0.4 0.05 0.25 1.0	V
$V_{OH}$	High-level output voltage <sup>3</sup> TTL half-drive buffer TTL single-drive buffer TTL double-drive buffer TTL triple-drive buffer * CMOS outputs CMOS outputs (optional) OSC outputs	$I_{OH} = -2.0mA$ $I_{OH} = -4.0mA$ $I_{OH} = -8.0mA$ $I_{OH} = -12.0mA$ $I_{OH} = -1.0\mu A$ $I_{OH} = -100\mu A$ $I_{OH} = -100\mu A$	2.4 2.4 2.4 2.4 $V_{DD}-0.05$ $V_{DD}-0.25$ 3.5			V



SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I <sub>OZ</sub>	Three-state output leakage current TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	V <sub>O</sub> = V <sub>DD</sub> and V <sub>SS</sub>	-5 -10 -20 -30		5 10 20 30	μA
I <sub>OS</sub>	Short-circuit output current <sup>2,4</sup> TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	V <sub>O</sub> = V <sub>DD</sub> and V <sub>SS</sub>	-50 -100 -200 -300		50 100 200 300	mA
I <sub>DDQ</sub>	Quiescent Supply Current	V <sub>DD</sub> = 5.5V			1	mA
C <sub>IN</sub>	Input capacitance <sup>5</sup>	f = 1MHz @ 0V		12		pF
C <sub>OUT</sub>	Output capacitance <sup>5</sup> TTL half-drive buffer TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	f = 1MHz @ 0V		11 12 14 22		pF
C <sub>IO</sub>	Bidirect I/O capacitance <sup>5</sup> TTL single-drive, CMOS, OSC buffers TTL double-drive buffer TTL triple-drive buffer *	f = 1MHz @ 0V		13 15 23		pF

**Notes:**

\* Contact UTMC prior to usage.

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V<sub>IH</sub> = V<sub>IH</sub>(min) + 20%, - 0%; V<sub>IL</sub> = V<sub>IL</sub>(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V<sub>IH</sub>(min) and V<sub>IL</sub>(max).
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF\*MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V<sub>SS</sub> at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

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