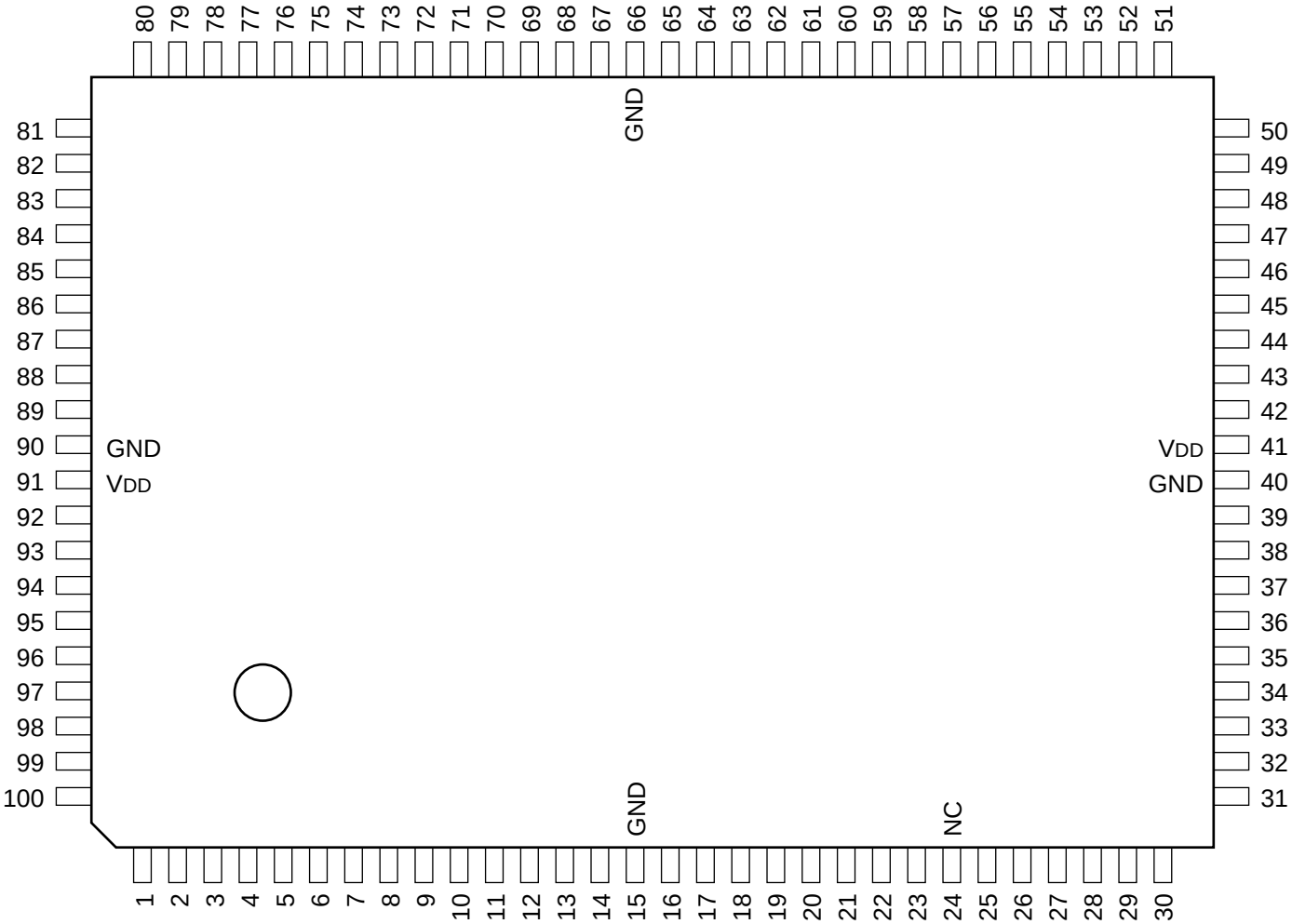
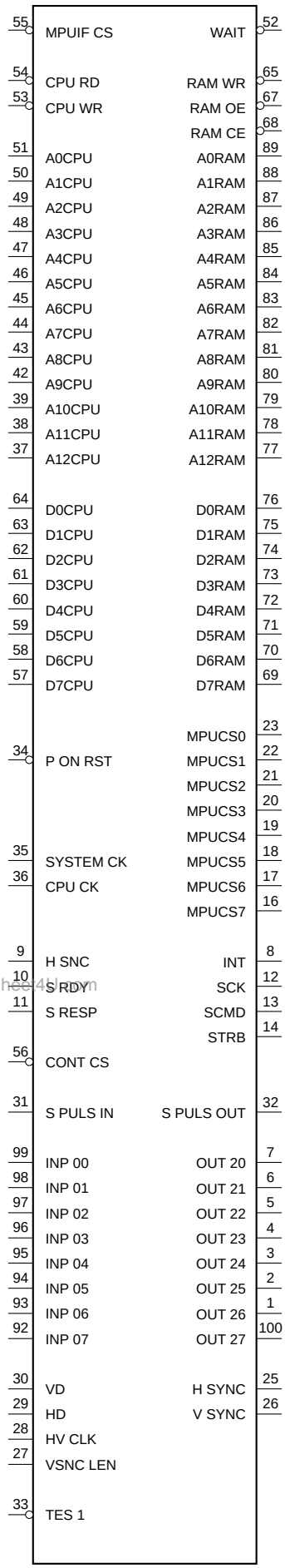
C-MOS 8-MPU COMMUNICATION CONTROLLER WITH PARALLEL PORT

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	O	OUT26	26	O	V SYNC	51	I	A0 CPU	76	I/O	D0 RAM
2	O	OUT25	27	I	VSNC LEN	52	O	$\overline{\text{WAIT}}$	77	O	A12 RAM
3	O	OUT24	28	I	HV CLK	53	I	$\overline{\text{CPU WR}}$	78	O	A11 RAM
4	O	OUT23	29	I	HD	54	I	$\overline{\text{CPU RD}}$	79	O	A10 RAM
5	O	OUT22	30	I	VD	55	I	$\overline{\text{MPUIF CS}}$	80	O	A9 RAM
6	O	OUT21	31	I	S PULS IN	56	I	$\overline{\text{CONT CS}}$	81	O	A8 RAM
7	O	OUT20	32	O	S PULS OUT	57	I/O	D7 CPU	82	O	A7 RAM
8	O	INT	33	I	$\overline{\text{TES 1}}$	58	I/O	D6 CPU	83	O	A6 RAM
9	I	H SNC	34	I	$\overline{\text{P ON RST}}$	59	I/O	D5 CPU	84	O	A5 RAM
10	I	S RDY	35	I	SYSTEM CK	60	I/O	D4 CPU	85	O	A4 RAM
11	I	S RESP	36	I	CPU CK	61	I/O	D3 CPU	86	O	A3 RAM
12	O	SCK	37	I	A12 CPU	62	I/O	D2 CPU	87	O	A2 RAM
13	O	SCMD	38	I	A11 CPU	63	I/O	D1 CPU	88	O	A1 RAM
14	O	STRB	39	I	A10 CPU	64	I/O	D0 CPU	89	O	A0 RAM
15	—	GND	40	—	GND	65	O	$\overline{\text{RAM WR}}$	90	—	GND
16	O	MPUCS7	41	—	V_{DD}	66	—	GND	91	—	V_{DD}
17	O	MPUCS6	42	I	A9 CPU	67	O	$\overline{\text{RAM OE}}$	92	I	INP 07
18	O	MPUCS5	43	I	A8 CPU	68	O	$\overline{\text{RAMCE}}$	93	I	INP 06
19	O	MPUCS4	44	I	A7 CPU	69	I/O	D7 RAM	94	I	INP 05
20	O	MPUCS3	45	I	A6 CPU	70	I/O	D6 RAM	95	I	INP 04
21	O	MPUCS2	46	I	A5 CPU	71	I/O	D5 RAM	96	I	INP 03
22	O	MPUCS1	47	I	A4 CPU	72	I/O	D4 RAM	97	I	INP 02
23	O	MPUCS0	48	I	A3 CPU	73	I/O	D3 RAM	98	I	INP 01
24	—	N.C	49	I	A2 CPU	74	I/O	D2 RAM	99	I	INP 00
25	O	H SYNC	50	I	A1 CPU	75	I/O	D1 RAM	100	O	OUT 27



INPUT

A0CPU - A12CPU	;	CPU ADDRESS BUS
CONT CS	;	INTERNAL/PARALLEL PORT
CPU CK	;	CPU CLOCK
CPU RD	;	CPU READ STROBE
CPU WR	;	CPU WRITE STROBE
HD	;	VIDEO HORIZONTAL SYNCHRONIZING PULSE
H SNC	;	SERIAL RECEIVE WAIT
HV CLK	;	VIDEO VERTICAL SAMPLING PULSE (13.5 MHz)
INP 00 - 07	;	PARALLEL PORT
MPUIF CS	;	EXTERNAL RAM CHIP SELECT
P ON RST	;	POWER IN RESET (L)
S PULS	;	MEDIOCRITY CLOCK PULSE
S RDY	;	SERIAL TRANSMISSION LEADY
S RESP	;	SERIAL RECEIVE DATA
SYSTEM CK	;	SYSTEM CLOCK
TES 1	;	TEST (L)
VD	;	VIDEO VERTICAL SYNCHRONIZING PULSE
VSNC LEN	;	VIDEO VERTICAL SYNCHRONIZING PULSE OUTPUT WIDTH CONTROL

OUTPUT

A0RAM - A12RAM	;	EXTERNAL RAM ADDRESS BUS
H SYNC	;	VIDEO HORIZONTAL SYNCHRONIZING PULSE
INT	;	SERIAL RECEIVE END
MPUCS0 - MPUCS7	;	SERIAL CORRESPONDENCE ENABLE
OUT 20 - 27	;	PARALLEL PORT
RAM CE	;	EXTERNAL RAM CHIP SELECT
RAM OE	;	EXTERNAL RAM OUTPUT ENABLE
RAM WR	;	EXTERNAL RAM WRITE STROBE
SCK	;	SERIAL CORRESPONDENCE CLOCK
SCMD	;	SERIAL TRANSMISSION DATA
S PULS	;	MEDIOCRITY CLOCK PULSE FREQUENCY (1/2-1/27)
STRB	;	SERIAL TRANSMISSION STROBE
V SYNC	;	VIDEO VERTICAL SYNCHRONIZING PULSE
WAIT	;	CPU WAIT

INPUT/OUTPUT

D0CPU - D7CPU	;	CPU DATA BUS
D0RAM - D7RAM	;	EXTERNAL RAM DATA BUS