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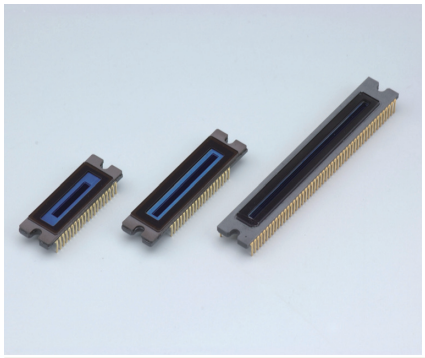
# TDI-CCD image sensors



S10200-02-01 S10201-04-01 S10202-08-01 S10202-16-01

## Operating the back-thinned CCD in TDI mode delivers high sensitivity.

TDI-CCD image sensers capture clear and bright images even under low-light-level conditions. During TDI (time delay integration) mode, the CCD captures an image of a moving object while transferring integrated signal charges synchronously with the object movement. This operation mode dramatically boosts sensitivity to high levels even when capturing fast moving objects. Our new TDI-CCD uses the back-thinned structure to achieve even higher quantum efficiency over a wide spectral range from UV to near IR region (200 to 1100 nm).

### Features

- **TDI mode gives high sensitivity**
- **High-speed, continuous image acquisition**
- **Back-thinned structure ensures high sensitivity from UV to near IR**
- **Multiple ports for high-speed line rate**
- **Low noise**

### Applications

- **Sequential imaging of high-speed moving samples**
- **Inspection tasks on electronic parts production line**
- **Semiconductor inspection**
- **Flow cytometery**

### TDI mode

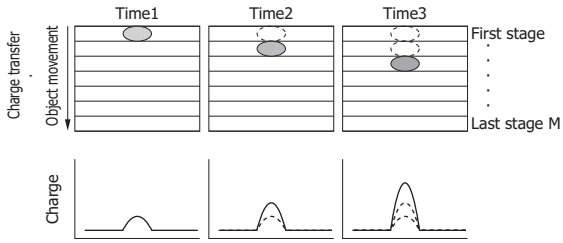
In FFT-CCD, signal charges in each line are vertically transferred during charge readout. TDI mode synchronizes this vertical transfer timing with the movement of the object, so that signal charges are integrated a number of times equal to the number of vertical stages of the CCD pixels. In the TDI mode, the signal charges must be transferred in the same direction at the same speed as those of the object to be imaged. These speeds are expressed by the following equation:

$v = f \times d$

v: object moving speed, charge transfer speed, f: vertical transfer frequency, d: pixel size

In the right figure, when the first stage charges are transferred to the second stage, an additional charges are produced in the second stage by photoelectric conversion and accumulated. When this operation is continuously repeated until reaching the last stage M (the number of vertical stages), signal charges which are M times greater than the initial charges are accumulated. Since the signal charges on each line are output from the CCD horizontal shift register, a two-dimensional image can be continuously acquired. In this way the TDI mode achieves sensitivity which is M times higher than linear image sensors (S/N is improved $\sqrt{M}$ times). The TDI mode also improves sensitivity variations compared to frame mode operation.

#### Schematic diagram showing integrated exposure by TDI mode




KMPDC0139EA

### Selection guide

| Type no. | Number of total pixels (H × V) | Number of effective pixels (H × V) | Number of ports | Pixel rate (MHz/port) | Line rate (kHz) | Vertical transfer | Applicable*1 camera |
|---|---|---|---|---|---|---|---|
| S10200-02-01*2*3 | 1040 × 128 | 1024 × 128 | 2 | 30 | 50 | Bi-directional | - |
| S10201-04-01*2*3 | 2080 × 128 | 2048 × 128 | 4 | | | | C10000-801 |
| S10202-08-01 | 4160 × 128 | 4096 × 128 | 8 | | | | - |
| S10202-16-01 | 4224 × 128 | 4096 × 128 | 16 | | 100 | | - |

*1: The C10000 series cameras are products manufactured by Hamamatsu Photonics, System Division (refer to page 14).
*2: Temporary window type (S10200-02N-01, S10201-04N-01) is also available upon request.
*3: Light-shield mask type (S10200-02M-01, S10201-04M-01) for horizontal register shielding is also available upon request [see device structure (P.7)]. The light-shield mask's aperture size in the vertical direction is 96 pixels. The effect of the light-shield mask may vary depending on the wavelength of the light source in use and the incident angle of light.

## Structure

| Parameter | Specification |
|---|---|
| Pixel size (H × V) | 12 × 12 µm |
| TDI stage | 128 |
| Anti-blooming | FW × 100 (min.) |
| Vertical clock | 3 phases |
| Horizontal clock | 2 phases |
| Output circuit | Three-stage MOSFET source follower |
| Package | Ceramic DIP (refer to dimensional outlines) |
| Window | Quartz glass*4 |

*4: Resin sealing

## Absolute maximum ratings (Ta=25 °C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operating temperature*5 *6 *7 | Topr | -50 | - | 60 | °C |
| Storage temperature*7 | Tstg | -50 | - | 70 | °C |
| Output transistor drain voltage | $V_{OD}$ | -0.5 | - | 25 | V |
| Reset drain voltage | $V_{RD}$ | -0.5 | - | 18 | V |
| Overflow drain voltage | $V_{OFD}$ | -0.5 | - | 18 | V |
| Overflow gate voltage | $V_{OFG}$ | -10 | - | 15 | V |
| Summing gate voltage | $V_{SG}$ | -10 | - | 15 | V |
| Output gate voltage | $V_{OG}$ | -10 | - | 15 | V |
| Reset gate voltage | $V_{RG}$ | -10 | - | 15 | V |
| Transfer gate voltage | $V_{TG}$ | -10 | - | 15 | V |
| Vertical clock voltage | $V_{P1V}$, $V_{P2V}$, $V_{P3V}$ | -8 | - | +8 | V |
| Horizontal clock voltage | $V_{P1H}$, $V_{P2H}$ | -10 | - | 15 | V |

*5: Package temperature
*6: The chip temperature may increase due to heating in high-speed operation. We recommend taking measures to dissipate heat as needed.
*7: No condensation
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

## Operating conditions (TDI mode, Ta=25 °C)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Output transistor drain voltage | | $V_{OD}$ | 12 | 15 | 18 | V |
| Reset drain voltage | | $V_{RD}$ | 12 | 14 | 16 | V |
| Output gate voltage | | $V_{OG}$ | 4 | 6 | 8 | V |
| Substrate voltage | | $V_{DGND}$, $V_{AGND}$ | - | 0 | - | V |
| Overflow drain voltage | | $V_{OFD}$ | 7 | 9 | 11 | V |
| Overflow gate voltage | | $V_{OFG}$ | 3 | 5 | 7 | V |
| Vertical shift register clock voltage | High | $V_{P1VH}$, $V_{P2VH}$, $V_{P3VH}$ | 4 | 6 | 8 | V |
| | Low | $V_{P1VL}$, $V_{P2VL}$, $V_{P3VL}$ | -6 | -5 | -4 | |
| Horizontal shift register clock voltage | High | $V_{P1HH}$, $V_{P2HH}$ | 4 | 6 | 8 | V |
| | Low | $V_{P1HL}$, $V_{P2HL}$ | -6 | -5 | -4 | |
| Summing gate voltage | High | $V_{SGH}$ | 4 | 6 | 8 | V |
| | Low | $V_{SHL}$ | -6 | -5 | -4 | |
| Reset gate voltage | High | $V_{RGH}$ | 7 | 8 | 9 | V |
| | Low | $V_{RGL}$ | -6 | 0 | - | |
| Transfer gate voltage | High | $V_{TGH}$ | 4 | 6 | 8 | V |
| | Low | $V_{TGL}$ | -6 | -5 | -4 | |
| External load resistance | | $R_L$ | 2.0 | 2.2 | 2.4 | kΩ |

## Electrical characteristics [Ta=25 °C, fc=30 MHz, Typ. value in operating conditions table (P.2), unless otherwise noted]

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Signal output frequency | | fc | - | 30 | 40 | MHz |
| Vertical shift register capacitance | S10200-02-01 | $C_{P1V}$, $C_{P2V}$, $C_{P3V}$ | - | 250 | - | pF |
| | S10201-04-01 | | - | 400 | - | |
| | S10202-08-01/-16-01 | | - | 650 | - | |
| Line rate | S10200-02-01 | LR | - | 50 | - | kHz |
| | S10201-04-01 | | - | 50 | - | |
| | S10202-08-01 | | - | 50 | - | |
| | S10202-16-01 | | - | 100 | - | |
| Horizontal shift register capacitance | S10200-02-01 | $C_{P1H}$, $C_{P2H}$ | - | 50 | - | pF |
| | S10201-04-01 | | - | 90 | - | |
| | S10202-08-01/-16-01 | | - | 90 | - | |
| Transfer gate capacitance | S10200-02-01 | $C_{TG}$ | - | 40 | - | pF |
| | S10201-04-01 | | - | 60 | - | |
| | S10202-08-01/-16-01 | | - | 100 | - | |
| Summing gate capacitance | S10200-02-01 | $C_{SG}$ | - | 20 | - | pF |
| | S10201-04-01 | | - | 40 | - | |
| | S10202-08-01/-16-01 | | - | 40 | - | |
| Reset gate capacitance | S10200-02-01 | $C_{RG}$ | - | 20 | - | pF |
| | S10201-04-01 | | - | 40 | - | |
| | S10202-08-01/-16-01 | | - | 40 | - | |
| Charge transfer efficiency*8 | | CTE | 0.99995 | 0.99999 | - | - |
| DC output level*9 | | Vout | - | 11 | - | V |
| Output impedance*10 | | Zo | - | 150 | - | Ω |
| Output MOSFET supply current/node | | Ido | - | 8 | 12 | mA |
| Power consumption*9 *10 | | P | - | 120 | - | mW/port |

*8: Charge transfer efficiency per pixel, measured at half of the full well capacity
*9: The values depend on the load resistance. ($V_{OD}$=15 V, Load resistance=2.2 kΩ)
*10: Power consumption of the on-chip amplifier plus load resistance

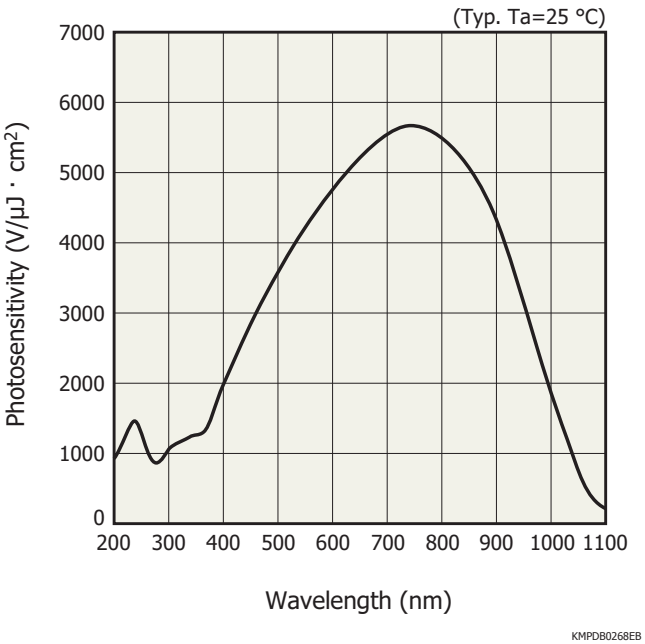
## Electrical and optical characteristics [Ta=25 °C, fc=30 MHz, Typ. value in operating conditions table (P.2), unless otherwise noted]

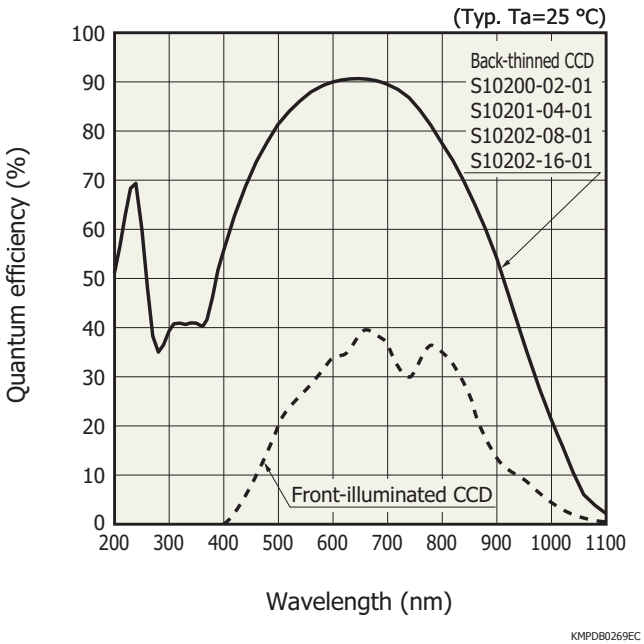
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Saturation output voltage | Vsat | - | FW × Sv | - | V |
| Full well capacity*11 | FW | 80 | 100 | 120 | $ke^-$ |
| CCD node sensitivity | Sv | 8.5 | 9.5 | 10.5 | $\mu V/e^-$ |
| Dark current*11 *12 | DS | - | 30 | 100 | $e^-$/pixel |
| Readout noise | Nr | - | 35 | 45 | $e^-$ rms |
| Dynamic range | DR | 1777 | 2857 | - | - |
| Photoresponse nonuniformity*13 | PRNU | - | ±3 | ±10 | % |
| Spectral response range | λ | - | 200 to 1100 | - | nm |

*11: TDI mode
*12: Line rate 50 kHz, accumulated dark signal after 128-stage transfer
*13: Measured at half of the full well capacity, using LED light (peak emission wavelength: 660 nm), in TDI mode

$$\text{Photoresponse nonuniformity (PRNU)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

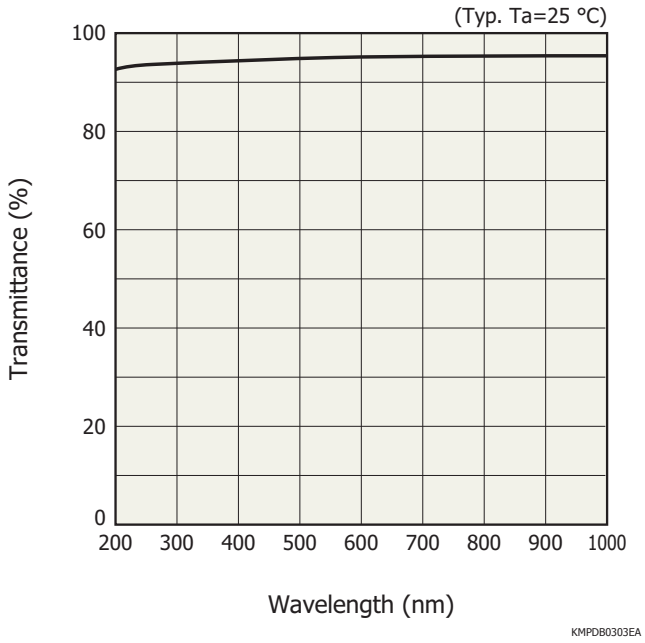
## Spectral response (without window)*14



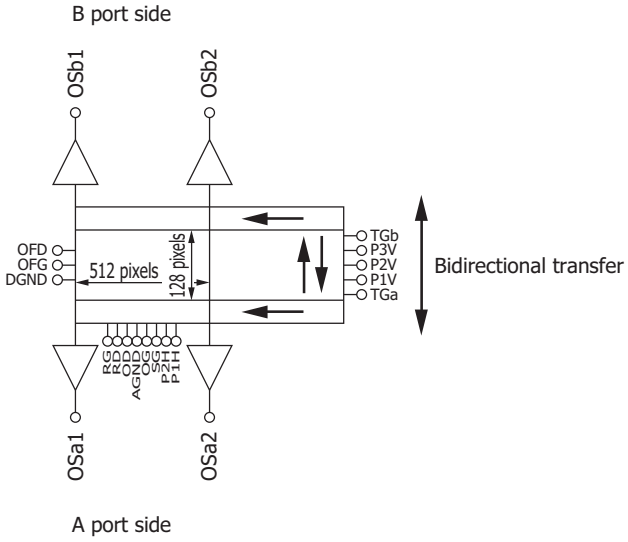

*14: Spectral response with quartz window is decreased according to the spectral transmittance characteristics of window material.

## Spectral transmittance characteristics of window material



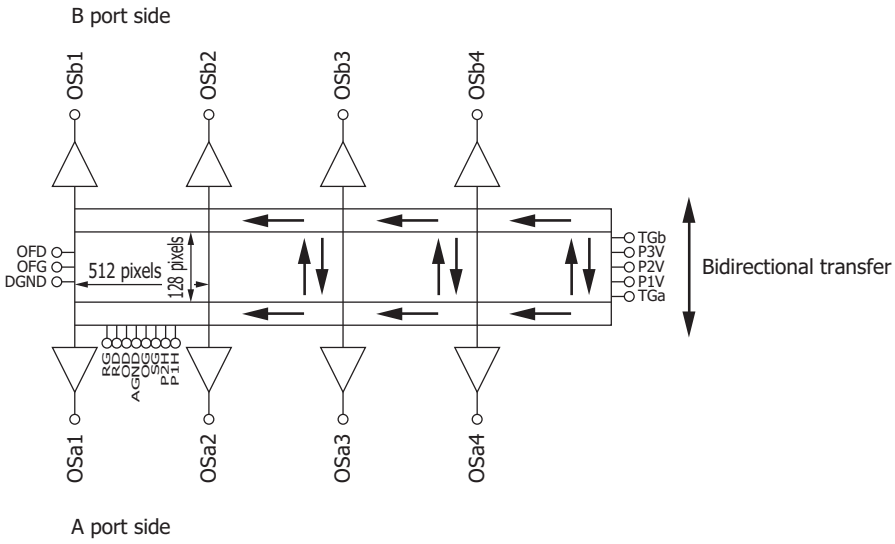
## Sensor structure

S10200-02-01



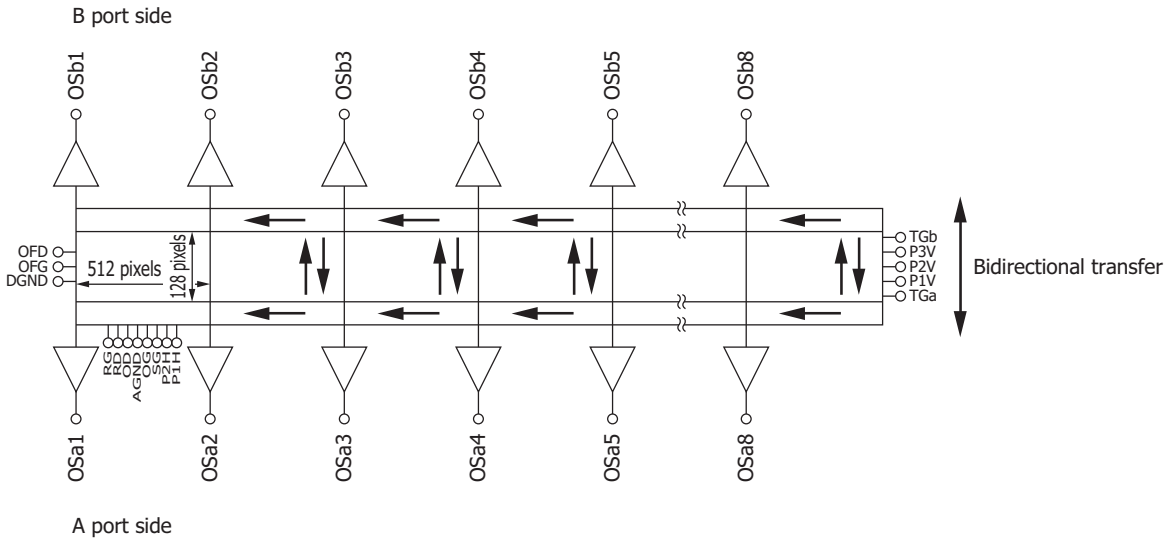

KAPDC0251EA

S10201-04-01



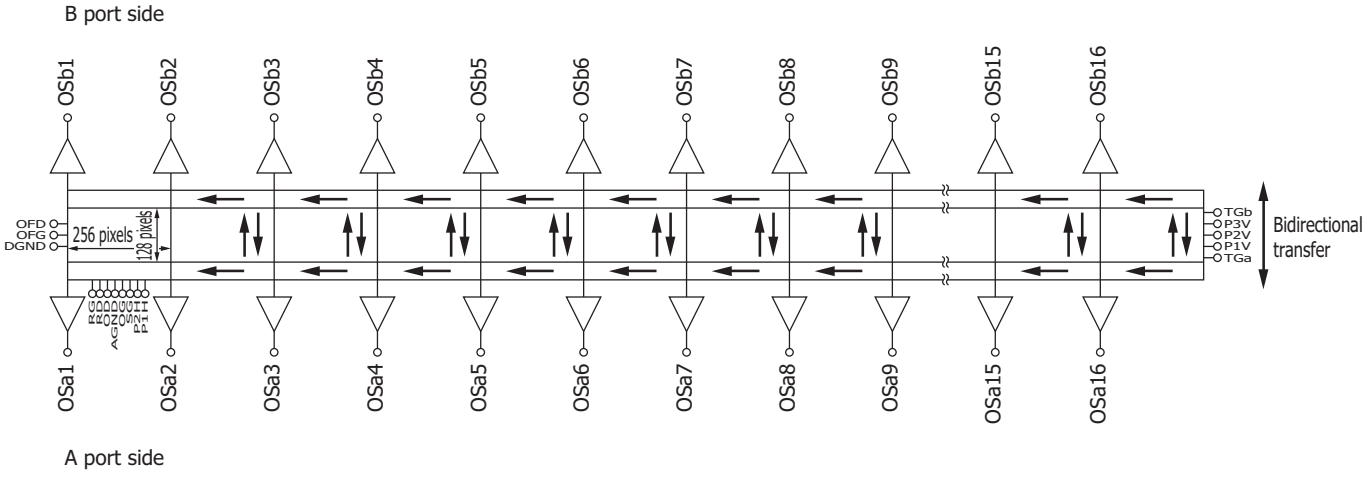

KMPDC0260EA

## S10202-08-01



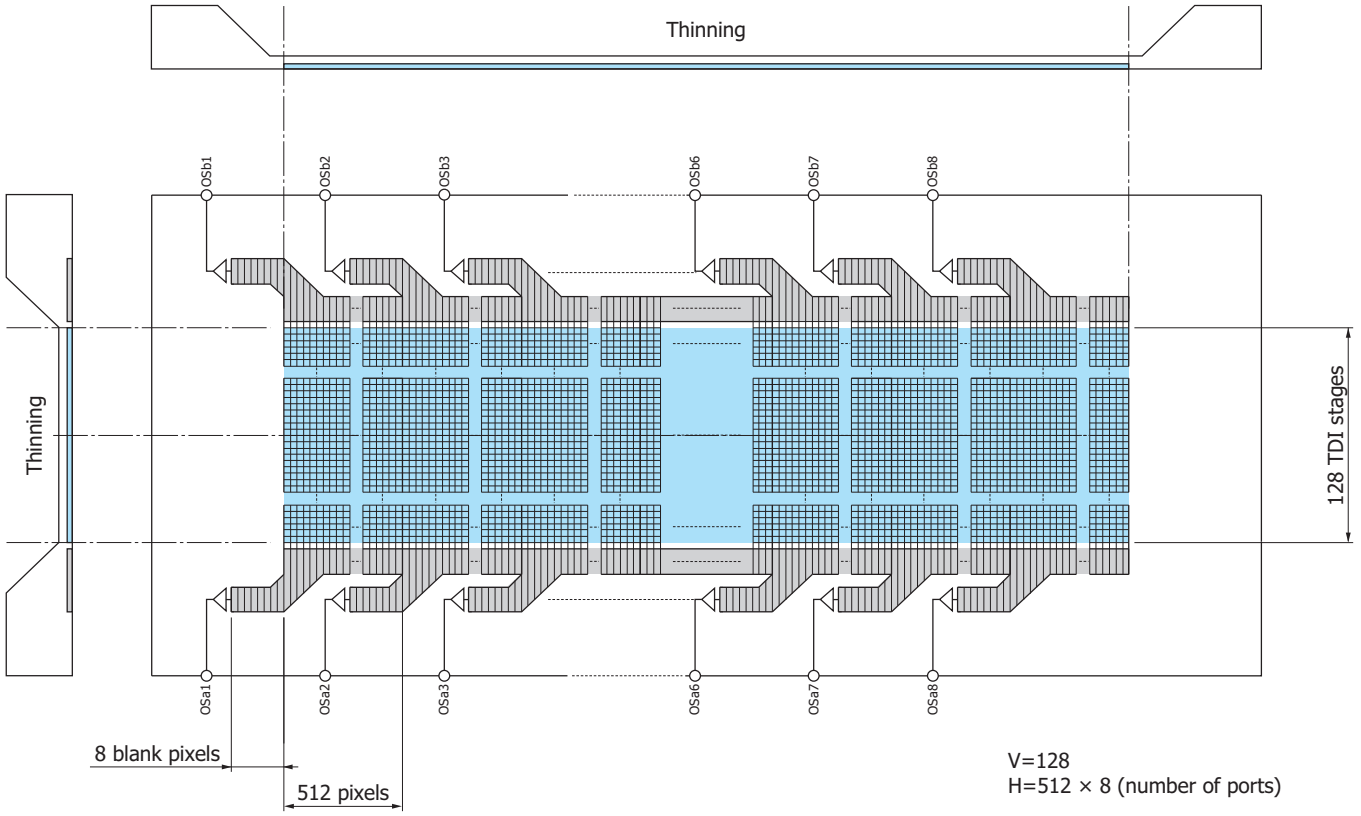

KMPDC0261EA

## S10202-16-01




KMPDC0262EA

## Device structure (typical example: S10202-08-01, conceptual drawing of top view)

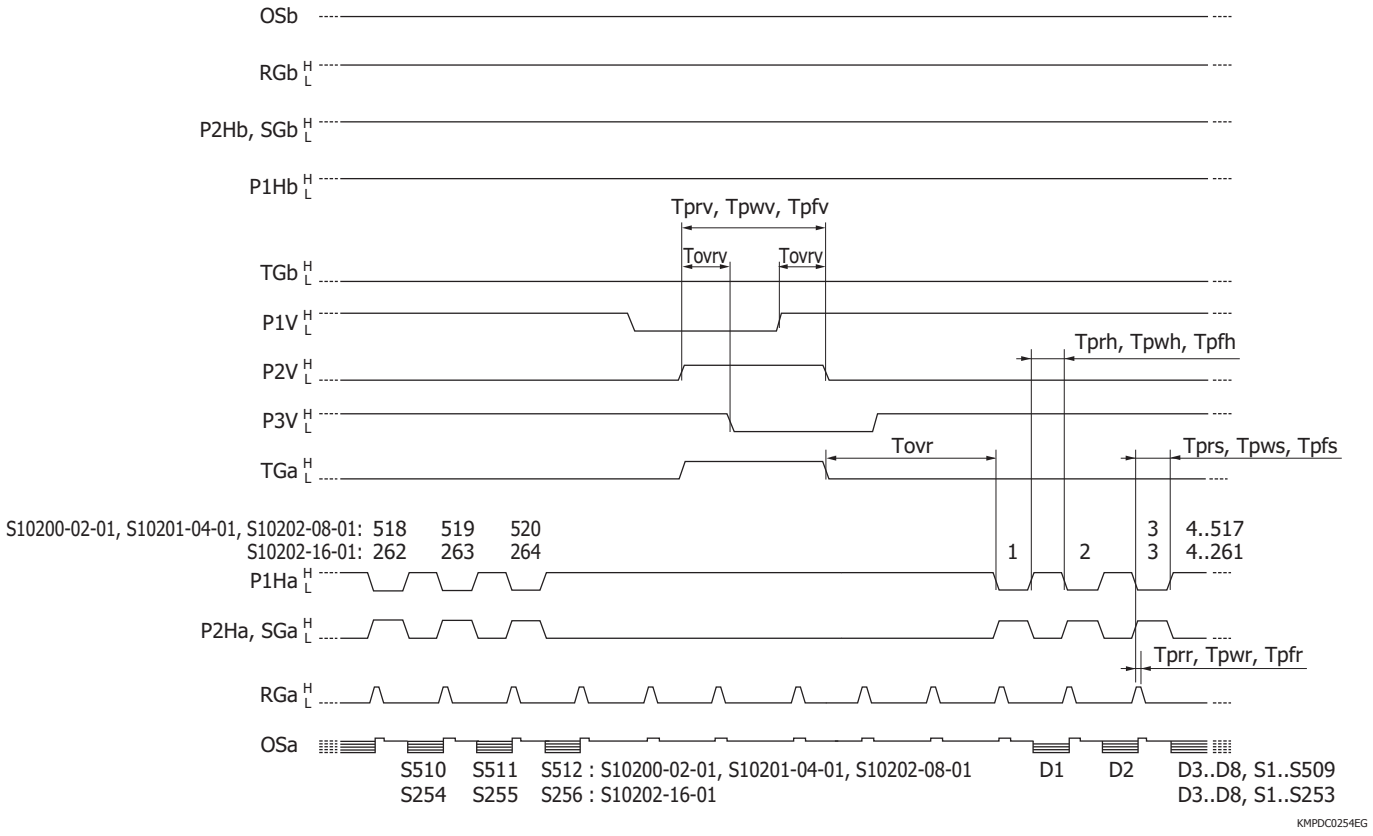



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

KMPDC0252EB

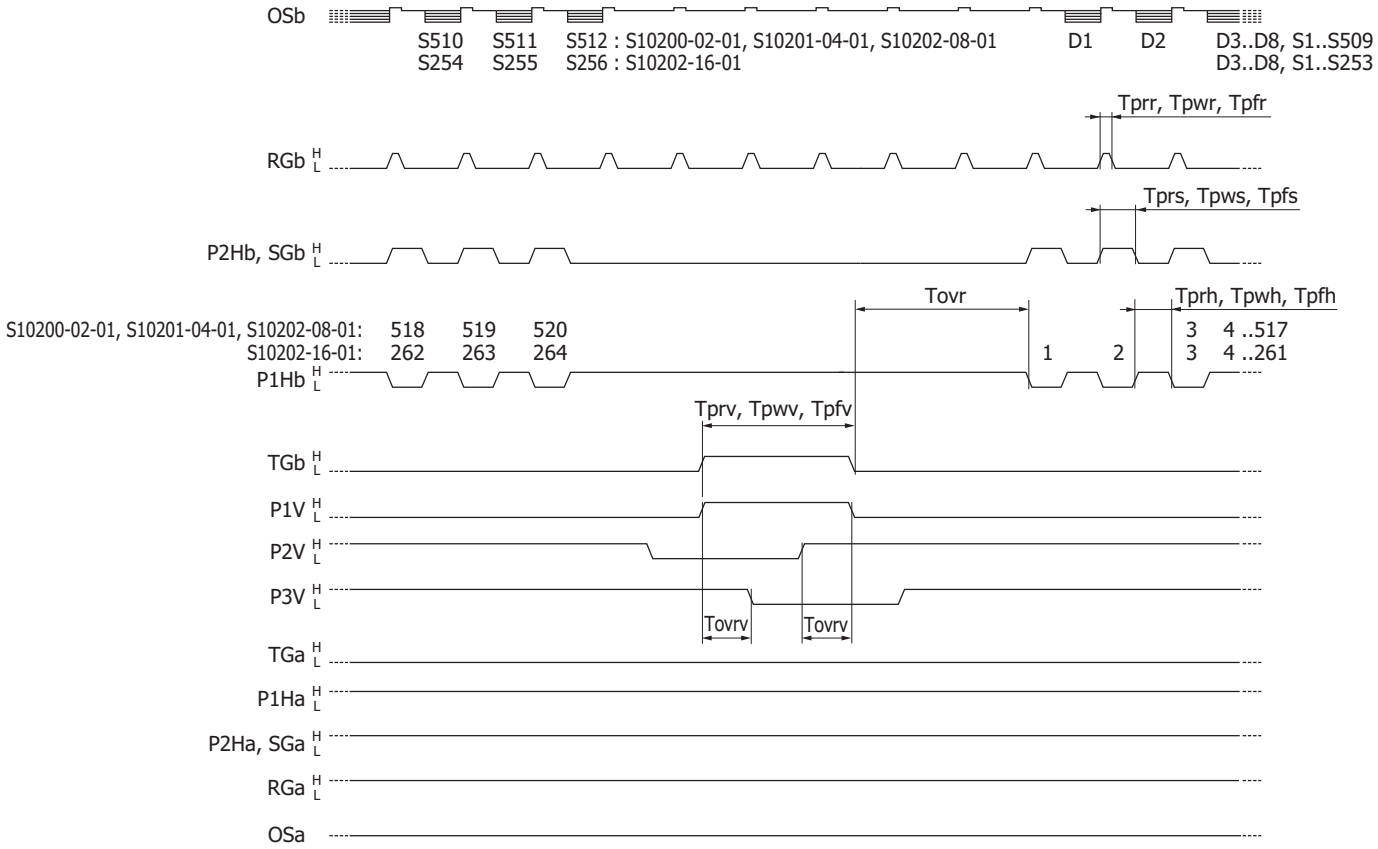
## Timing chart

A port side readout




KMPDC0254EG

B port side readout



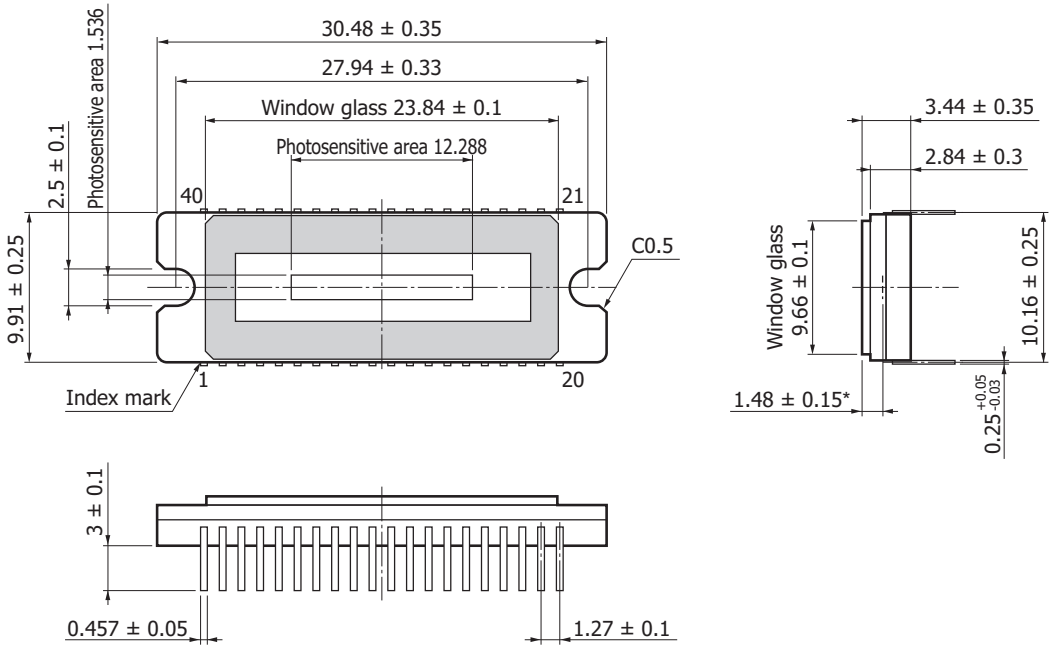

KMPDC0253EH

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| P1V, 2V, 3V, TG | Pulse width | Tpwv | 120 | 770 | - | ns |
| | Rise and fall times | Tprv, Tpfv | 2 | 10 | - | ns |
| | Overlap time | Tovrv | 30 | 300 | - | ns |
| P1H, P2H | Pulse width*15 | Tpwh | 12.5 | 16.5 | - | ns |
| | Rise and fall times*15 | Tprh, Tpfh | 3 | 6 | - | ns |
| | Duty ratio*15 | - | - | 50 | - | % |
| SG | Pulse width | Tpws | 12.5 | 16.5 | - | ns |
| | Rise and fall times | Tprs, Tpfs | 2 | 4 | - | ns |
| | Duty ratio | - | - | 50 | - | % |
| RG | Pulse width | Tpwr | 5 | 6 | - | ns |
| | Rise and fall times | Tprr, Tpfr | 1 | 2 | - | ns |
| TG - P1H | Overlap time | Tovr | 30 | 1000 | - | ns |

*15: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

## Dimensional outlines (unit: mm)

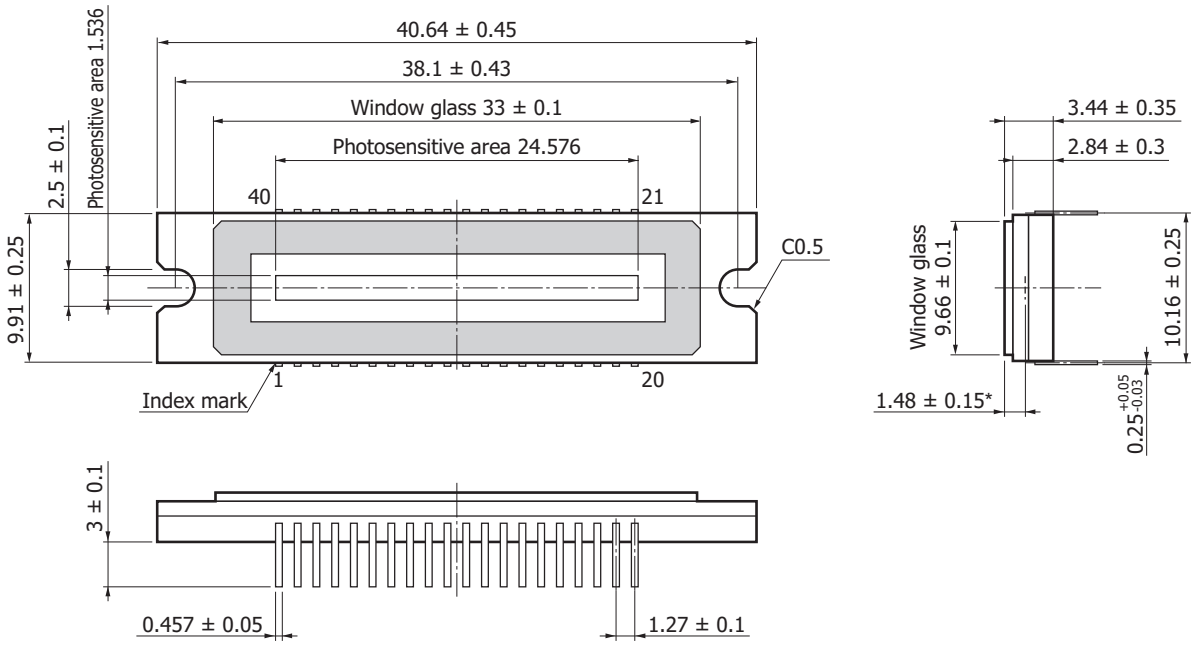
S10200-02-01




* Distance from upper surface of window to photosensitive surface

KMPDA0218EC

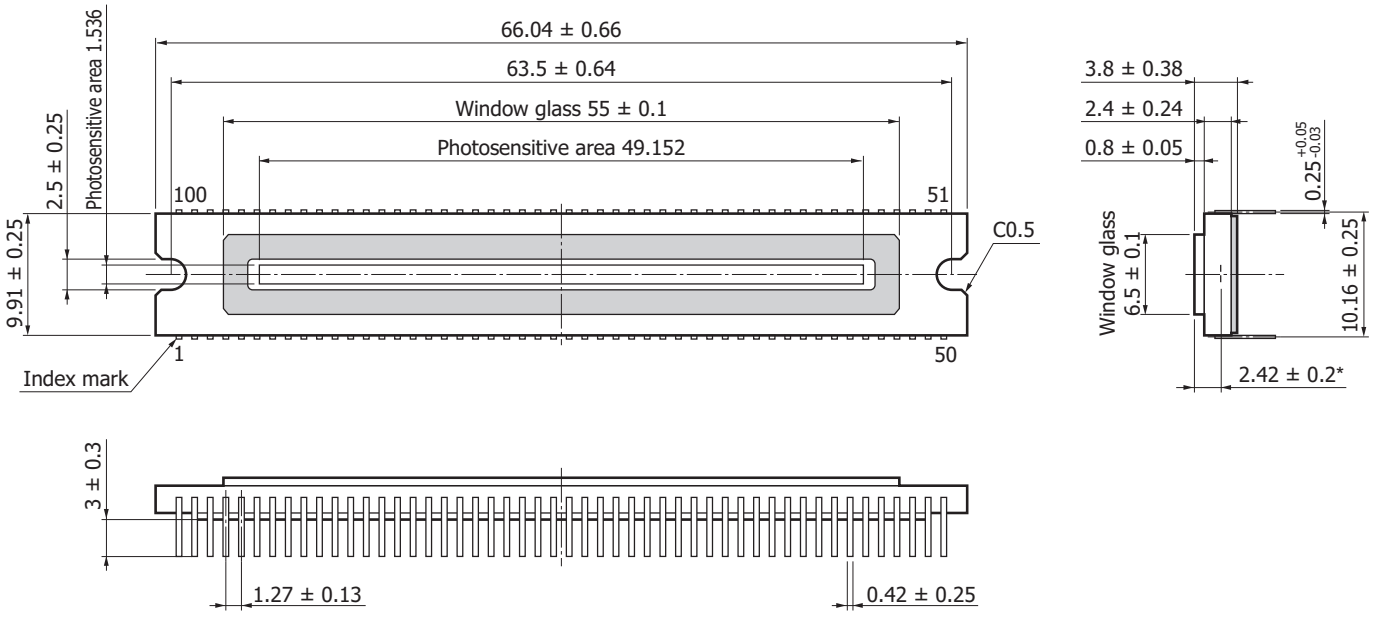
## S10201-04-01




* Distance from upper surface of window to photosensitive surface

KMPDA0219EC

## S10202-08-01, S10202-16-01




* Distance from upper surface of window to photosensitive surface

KMPDA0220EC

## Pin connections

| S10200-02-01 | | | | S10201-04-01 | | | |
|---|---|---|---|---|---|---|---|
| Pin no. | Symbol | Function | Remark | Pin no. | Symbol | Function | Remark |
| 1 | P2V | CCD vertical register clock-2 | | 1 | P2V | CCD vertical register clock-2 | |
| 2 | P3V | CCD vertical register clock-3 | | 2 | P3V | CCD vertical register clock-3 | |
| 3 | P1V | CCD vertical register clock-1 | | 3 | P1V | CCD vertical register clock-1 | |
| 4 | TGa | Transfer gate-a | | 4 | TGa | Transfer gate-a | |
| 5 | SSD | Digital GND | GND | 5 | SSD | Digital GND | GND |
| 6 | NC | No connection | | 6 | OSa1 | Output transistor source-a1 | RL=2.2 kΩ |
| 7 | SSA | Analog GND | GND | 7 | SSA | Analog GND | GND |
| 8 | OSa1 | Output transistor source-a 1 | RL=2.2 kΩ | 8 | OSa2 | Output transistor source-a2 | RL=2.2 kΩ |
| 9 | OD1 | Output drain-1 | +15 V | 9 | OD1 | Output drain-1 | +15 V |
| 10 | OSa2 | Output transistor source-a 2 | RL=2.2 kΩ | 10 | OSa3 | Output transistor source-a3 | RL=2.2 kΩ |
| 11 | NC | No connection | | 11 | OD3 | Output drain-3 | +15 V |
| 12 | NC | No connection | | 12 | OSa4 | Output transistor source-a4 | RL=2.2 kΩ |
| 13 | OG | Output gate | +6 V | 13 | OG | Output gate | +6 V |
| 14 | RD | Reset drain | +14 V | 14 | RD | Reset drain | +14 V |
| 15 | OFD | Overflow drain | +9 V | 15 | OFD | Overflow drain | +9 V |
| 16 | SSD | Digital GND | GND | 16 | SSD | Digital GND | GND |
| 17 | RGa | Reset gate-a | | 17 | RGa | Reset gate-a | |
| 18 | SGa | Summing gate-a | | 18 | SGa | Summing gate-a | |
| 19 | P1Ha | CCD horizontal register-a clock-1 | | 19 | P1Ha | CCD horizontal register-a clock-1 | |
| 20 | P2Ha | CCD horizontal register-a clock-2 | | 20 | P2Ha | CCD horizontal register-a clock-2 | |
| 21 | P2Hb | CCD horizontal register-b clock-2 | | 21 | P2Hb | CCD horizontal register-b clock-2 | |
| 22 | P1Hb | CCD horizontal register-b clock-1 | | 22 | P1Hb | CCD horizontal register-b clock-1 | |
| 23 | SGb | Summing gate-b | | 23 | SGb | Summing gate-b | |
| 24 | RGb | Reset gate-b | | 24 | RGb | Reset gate-b | |
| 25 | SSD | Digital GND | GND | 25 | SSD | Digital GND | GND |
| 26 | OFG | Overflow gate | +5 V | 26 | OFG | Overflow gate | +5 V |
| 27 | RD | Reset drain | +14 V | 27 | RD | Reset drain | +14 V |
| 28 | OG | Output gate | +6 V | 28 | OG | Output gate | +6 V |
| 29 | NC | No connection | | 29 | OSb4 | Output transistor source-b4 | RL=2.2 kΩ |
| 30 | NC | No connection | | 30 | OD4 | Output drain-4 | +15 V |
| 31 | OSb2 | Output transistor source-b2 | RL=2.2 kΩ | 31 | OSb3 | Output transistor source-b3 | RL=2.2 kΩ |
| 32 | OD2 | Output drain-2 | +15 V | 32 | OD2 | Output drain-2 | +15 V |
| 33 | OSb1 | Output transistor source-b1 | RL=2.2 kΩ | 33 | OSb2 | Output transistor source-b2 | RL=2.2 kΩ |
| 34 | SSA | Analog GND | GND | 34 | SSA | Analog GND | GND |
| 35 | NC | No connection | | 35 | OSb1 | Output transistor source-b1 | RL=2.2 kΩ |
| 36 | SSD | Digital GND | GND | 36 | SSD | Digital GND | GND |
| 37 | TGb | Transfer gate-b | | 37 | TGb | Transfer gate-b | |
| 38 | P1V | CCD vertical register clock-1 | | 38 | P1V | CCD vertical register clock-1 | |
| 39 | P3V | CCD vertical register clock-3 | | 39 | P3V | CCD vertical register clock-3 | |
| 40 | P2V | CCD vertical register clock-2 | | 40 | P2V | CCD vertical register clock-2 | |

| S10202-08-01 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin no. | Symbol | Function | Remark | Pin no. | Symbol | Function | Remark |
| 1 | P1Ha1 | CCD horizontal register-a1 clock-1 | | 51 | P1Hb2 | CCD horizontal register-b2 clock-1 | |
| 2 | P2Ha1 | CCD horizontal register-a1 clock-2 | | 52 | P2Hb2 | CCD horizontal register-b2 clock-2 | |
| 3 | SGa1 | Summing gate-a1 | | 53 | SGb2 | Summing gate-b2 | |
| 4 | RGa1 | Reset gate-a1 | | 54 | RGb2 | Reset gate-b2 | |
| 5 | SSD | Digital GND | GND | 55 | SSD | Digital GND | GND |
| 6 | SSA | Analog GND | GND | 56 | SSA | Analog GND | GND |
| 7 | OFG | Overflow gate | +6 V | 57 | OFG | Overflow gate | +5 V |
| 8 | OSa1 | Output transistor source-a1 | RL=2.2 kΩ | 58 | NC | No connection | |
| 9 | OFD | Overflow drain | +9 V | 59 | OFD | Overflow drain | +9 V |
| 10 | NC | No connection | | 60 | OSb8 | Output transistor source-b8 | RL=2.2 kΩ |
| 11 | RD | Reset drain | +14 V | 61 | RD | Reset drain | +14 V |
| 12 | OSa2 | Output transistor source-a2 | RL=2.2 kΩ | 62 | NC | No connection | |
| 13 | OG | Output gate | +6 V | 63 | OG | Output gate | +6 V |
| 14 | NC | No connection | | 64 | OSb7 | Output transistor source-b7 | RL=2.2 kΩ |
| 15 | OD1 | Output drain-1 | +15 V | 65 | NC | No connection | |
| 16 | OSa3 | Output transistor source-a3 | RL=2.2 kΩ | 66 | NC | No connection | |
| 17 | NC | No connection | | 67 | OD8 | Output drain-8 | +15 V |
| 18 | NC | No connection | | 68 | OSb6 | Output transistor source-b6 | RL=2.2 kΩ |
| 19 | OD3 | Output drain-3 | +15 V | 69 | NC | No connection | |
| 20 | OSa4 | Output transistor source-a4 | RL=2.2 kΩ | 70 | NC | No connection | |
| 21 | NC | No connection | | 71 | OD6 | Output drain-6 | +15 V |
| 22 | NC | No connection | | 72 | OSb5 | Output transistor source-b5 | RL=2.2 kΩ |
| 23 | SSD | Digital GND | GND | 73 | SSD | Digital GND | GND |
| 24 | TGa | Transfer gate-a | | 74 | P1V | CCD vertical register clock-1 | |
| 25 | P2V | CCD vertical register clock-2 | | 75 | P3V | CCD vertical register clock-3 | |
| 26 | P3V | CCD vertical register clock-3 | | 76 | P2V | CCD vertical register clock-2 | |
| 27 | P1V | CCD vertical register clock-1 | | 77 | TGb | Transfer gate-b | |
| 28 | SSD | Digital GND | GND | 78 | SSD | Digital GND | GND |
| 29 | OSa5 | Output transistor source-a5 | RL=2.2 kΩ | 79 | NC | No connection | |
| 30 | OD5 | Output drain-5 | +15 V | 80 | NC | No connection | |
| 31 | NC | No connection | | 81 | OSb4 | Output transistor source-b4 | RL=2.2 kΩ |
| 32 | NC | No connection | | 82 | OD4 | Output drain-4 | +15 V |
| 33 | OSa6 | Output transistor source-a6 | RL=2.2 kΩ | 83 | NC | No connection | |
| 34 | OD7 | Output drain-7 | +15 V | 84 | NC | No connection | |
| 35 | NC | No connection | | 85 | OSb3 | Output transistor source-b3 | RL=2.2 kΩ |
| 36 | NC | No connection | | 86 | OD2 | Output drain-2 | +15 V |
| 37 | OSa7 | Output transistor source-a7 | RL=2.2 kΩ | 87 | NC | No connection | |
| 38 | OG | Output gate | +6 V | 88 | OG | Output gate | +6 V |
| 39 | NC | No connection | | 89 | OSb2 | Output transistor source-b2 | RL=2.2 kΩ |
| 40 | RD | Reset drain | +14 V | 90 | RD | Reset drain | +14 V |
| 41 | OSa8 | Output transistor source-a8 | RL=2.2 kΩ | 91 | NC | No connection | |
| 42 | OFD | Overflow drain | +9 V | 92 | OFD | Overflow drain | +9 V |
| 43 | NC | No connection | | 93 | OSb1 | Output transistor source-b1 | RL=2.2 kΩ |
| 44 | OFG | Overflow gate | +5 V | 94 | OFG | Overflow gate | +5 V |
| 45 | SSA | Analog GND | GND | 95 | SSA | Analog GND | GND |
| 46 | SSD | Digital GND | GND | 96 | SSD | Digital GND | GND |
| 47 | RGa2 | Reset gate-a2 | | 97 | RGb1 | Reset gate-b1 | |
| 48 | SGa2 | Summing gate-a2 | | 98 | SGb1 | Summing gate-b1 | |
| 49 | P2Ha2 | CCD horizontal register-a2 clock-2 | | 99 | P2Hb1 | CCD horizontal register-b1 clock-2 | |
| 50 | P1Ha2 | CCD horizontal register-a2 clock-1 | | 100 | P1Hb1 | CCD horizontal register-b1 clock-1 | |

| S10202-16-01 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin no. | Symbol | Function | Remark | Pin no. | Symbol | Function | Remark |
| 1 | P1Ha1 | CCD horizontal register-a1 clock-1 | | 51 | P1Hb2 | CCD horizontal register-b2 clock-1 | |
| 2 | P2Ha1 | CCD horizontal register-a1 clock-2 | | 52 | P2Hb2 | CCD horizontal register-b2 clock-2 | |
| 3 | SGa1 | Summing gate-a1 | | 53 | SGb2 | Summing gate-b2 | |
| 4 | RGa1 | Reset gate-a1 | | 54 | RGb2 | Reset gate-b2 | |
| 5 | SSD | Digital GND | GND | 55 | SSD | Digital GND | GND |
| 6 | SSA | Analog GND | GND | 56 | SSA | Analog GND | GND |
| 7 | OFG | Overflow gate | +5 V | 57 | OFG | Overflow gate | +5 V |
| 8 | OSa1 | Output transistor source-a1 | RL=2.2 kΩ | 58 | OSb16 | Output transistor source-b16 | RL=2.2 kΩ |
| 9 | OFD | Overflow drain | +9 V | 59 | OFD | Overflow drain | +9 V |
| 10 | OSa2 | Output transistor source-a2 | RL=2.2 kΩ | 60 | OSb15 | Output transistor source-b15 | RL=2.2 kΩ |
| 11 | RD | Reset drain | +14 V | 61 | RD | Reset drain | +14 V |
| 12 | OSa3 | Output transistor source-a3 | RL=2.2 kΩ | 62 | OSb14 | Output transistor source-b14 | RL=2.2 kΩ |
| 13 | OG | Output gate | +6 V | 63 | OG | Output gate | +6 V |
| 14 | OSa4 | Output transistor source-a4 | RL=2.2 kΩ | 64 | OSb13 | Output transistor source-b13 | RL=2.2 kΩ |
| 15 | OD1 | Output drain-1 | +15 V | 65 | OD16 | Output drain-16 | +15 V |
| 16 | OSa5 | Output transistor source-a5 | RL=2.2 kΩ | 66 | OSb12 | Output transistor source-b12 | RL=2.2 kΩ |
| 17 | OD2 | Output drain-2 | +15 V | 67 | OD15 | Output drain-15 | +15 V |
| 18 | OSa6 | Output transistor source-a6 | RL=2.2 kΩ | 68 | OSb11 | Output transistor source-b11 | RL=2.2 kΩ |
| 19 | OD5 | Output drain-5 | +15 V | 69 | OD12 | Output drain-12 | +15 V |
| 20 | OSa7 | Output transistor source-a7 | RL=2.2 kΩ | 70 | OSb10 | Output transistor source-b10 | RL=2.2 kΩ |
| 21 | OD6 | Output drain-6 | +15 V | 71 | OD11 | Output drain-11 | +15 V |
| 22 | OSa8 | Output transistor source-a8 | RL=2.2 kΩ | 72 | OSb9 | Output transistor source-b9 | RL=2.2 kΩ |
| 23 | SSD | Digital GND | GND | 73 | SSD | Digital GND | GND |
| 24 | TGa | Transfer gate-a | | 74 | P1V | CCD vertical register clock-1 | |
| 25 | P2V | CCD vertical register clock-2 | | 75 | P3V | CCD vertical register clock-3 | |
| 26 | P3V | CCD vertical register clock-3 | | 76 | P2V | CCD vertical register clock-2 | |
| 27 | P1V | CCD vertical register clock-1 | | 77 | TGb | Transfer gate-b | |
| 28 | SSD | Digital GND | GND | 78 | SSD | Digital GND | GND |
| 29 | OSa9 | Output transistor source-a9 | RL=2.2 kΩ | 79 | OSb8 | Output transistor source-b8 | RL=2.2 kΩ |
| 30 | OD9 | Output drain-9 | +15 V | 80 | OD8 | Output drain-8 | +15 V |
| 31 | OSa10 | Output transistor source-a10 | RL=2.2 kΩ | 81 | OSb7 | Output transistor source-b7 | RL=2.2 kΩ |
| 32 | OD10 | Output drain-10 | +15 V | 82 | OD7 | Output drain-7 | +15 V |
| 33 | OSa11 | Output transistor source-a11 | RL=2.2 kΩ | 83 | OSb6 | Output transistor source-b6 | RL=2.2 kΩ |
| 34 | OD13 | Output drain-13 | +15 V | 84 | OD4 | Output drain-4 | +15 V |
| 35 | OSa12 | Output transistor source-a12 | RL=2.2 kΩ | 85 | OSb5 | Output transistor source-b5 | RL=2.2 kΩ |
| 36 | OD14 | Output drain-14 | +15 V | 86 | OD3 | Output drain-3 | +15 V |
| 37 | OSa13 | Output transistor source-a13 | RL=2.2 kΩ | 87 | OSb4 | Output transistor source-b4 | RL=2.2 kΩ |
| 38 | OG | Output gate | +6 V | 88 | OG | Output gate | +6 V |
| 39 | OSa14 | Output transistor source-a14 | RL=2.2 kΩ | 89 | OSb3 | Output transistor source-b3 | RL=2.2 kΩ |
| 40 | RD | Reset drain | +14 V | 90 | RD | Reset drain | +14 V |
| 41 | OSa15 | Output transistor source-a15 | RL=2.2 kΩ | 91 | OSb2 | Output transistor source-b2 | RL=2.2 kΩ |
| 42 | OFD | Overflow drain | +9 V | 92 | OFD | Overflow drain | +9 V |
| 43 | OSa16 | Output transistor source-a16 | RL=2.2 kΩ | 93 | OSb1 | Output transistor source-b1 | RL=2.2 kΩ |
| 44 | OFG | Overflow gate | +5 V | 94 | OFG | Overflow gate | +5 V |
| 45 | SSA | Analog GND | GND | 95 | SSA | Analog GND | GND |
| 46 | SSD | Digital GND | GND | 96 | SSD | Digital GND | GND |
| 47 | RGa2 | Reset gate-a2 | | 97 | RGb1 | Reset gate-b1 | |
| 48 | SGa2 | Summing gate-a2 | | 98 | SGb1 | Summing gate-b1 | |
| 49 | P2Ha2 | CCD horizontal register-a2 clock-2 | | 99 | P2Hb1 | CCD horizontal register-b1 clock-2 | |
| 50 | P1Ha2 | CCD horizontal register-a2 clock-1 | | 100 | P1Hb1 | CCD horizontal register-b1 clock-1 | |

## Precautions (Electrostatic countermeasures)

· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Avoid directly placing these sensors on a work-desk, etc. that may carry an electrostatic charge.
· Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
· Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

## Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclamer
· Image sensors/Precautions

### TDI camera C10000 series

The TDI camera C10000 series is useful in a wide range of imaging applications that require both high speed and high sensitivity, including in-line monitoring and inspection.

■ Product information
www.hamamatsu.com/all/en/C10000-801.html

C10000-801 (With S10201-04-01)

Electrical and optical characteristics listed in the datasheet are the values when used under typical operating conditions. We recommend using the product under typical operating conditions. Product characteristics vary with operating conditions. Operating conditions specified in the datasheet show the adjustment range. They must be adjusted within the specified range.



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