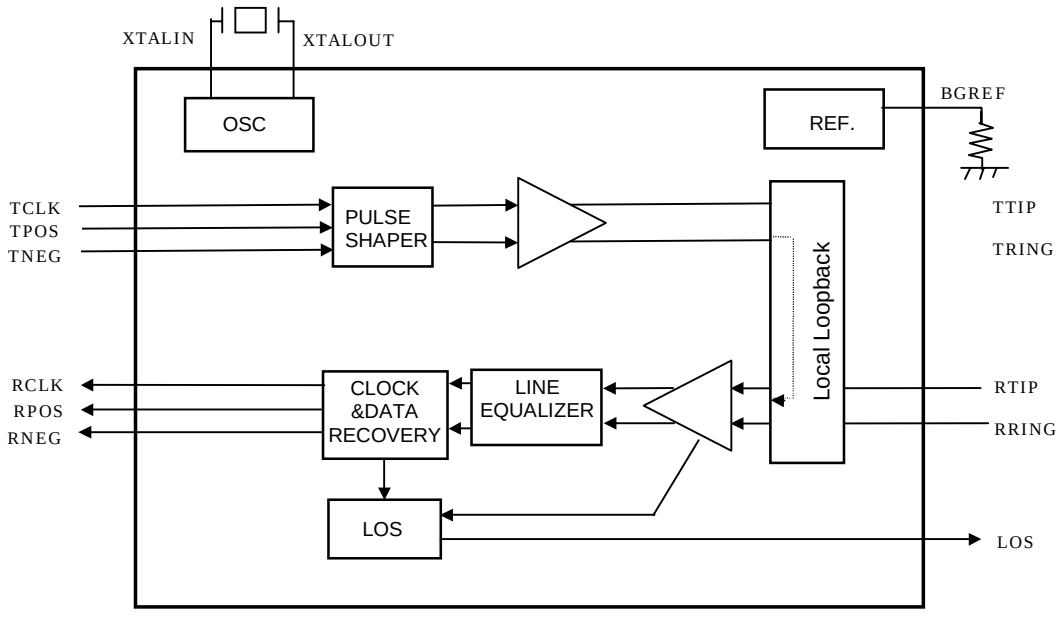
AK2531

J1 (1.5M) / J2 (6.3M) AMI Transceiver

FEATURE

- J1(1.544Mbps) / J2(6.312Mbps) AMI cording transceiver(LIU)
- Jitter Tolerance: Compliant with ITU-T G.824
- Transmitter Pulse Shape: Compliant with JT-G.703
- Loss of Signal Detection
- Line equalizer
- Local loopback function
- Crystal oscillator: 24.704MHz(1.5M), 25.248MHz(6.3M)
- Single 3.3V±5% or 5.0V±5% Supply
- Low Power Consumption:170mW(typ:1.544Mbps), 160mW(typ:6.322Mbps)
- Package: 48pin LQFP

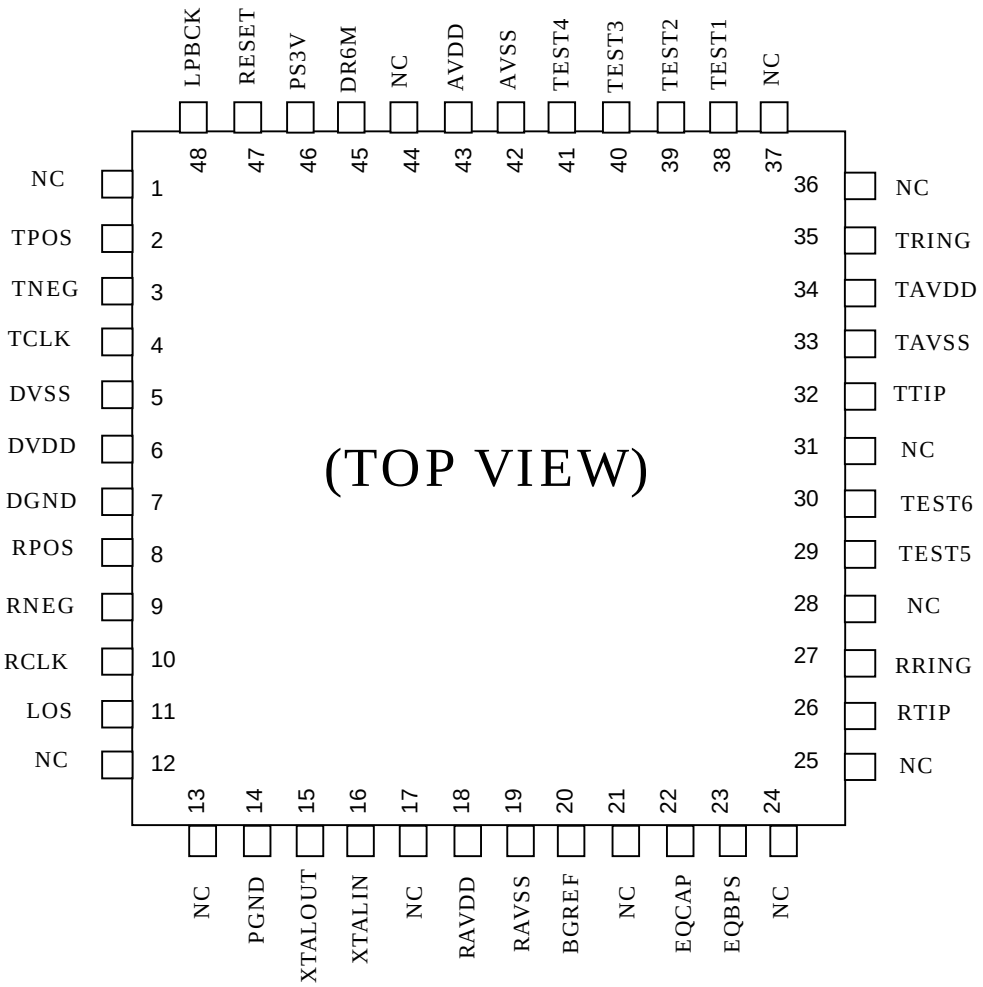
BLOCK DIAGRAM



GENERAL DESCRIPTION

The AK2531 is the J1/J2(JT-G.703) transceiver for Leased line, MUX, Base station for mobile communications etc. It includes Pulse shaper, Line Driver, Clock and Data Recovery, LOS Detector, Crystal oscillator, etc. in one package. Internal equalizer automatically equalizes the receive pulse attenuated by the cable loss.

PIN ASSIGNMENTS



PIN CONDITION

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
1	NC	-				Note 1)
2	TPOS	I	TTL/CMOS			TTL for 5V, CMOS for 3.3V
3	TNEG	I	TTL/CMOS			TTL for 5V, CMOS for 3.3V
4	TCLK	I	TTL/CMOS			TTL for 5V, CMOS for 3.3V
5	DVSS	I	POWER			
6	DVDD	I	POWER			
7	DGND	I	POWER			
8	RPOS	O	CMOS	≤50pF		
9	RNEG	O	CMOS	≤50pF		
10	RCLK	O	CMOS	≤50pF		
11	LOS	O	CMOS	≤50pF		
12	NC	-				Note 1)
13	NC	-				Note 1)
14	PGND	I	POWER			
15	XTALOUT	O	ANALOG			
16	XTALIN	I	ANALOG			
17	NC	-				Note 1)
18	RAVDD	I	POWER			
19	RAVSS	I	POWER			
20	BGREF	O	ANALOG		12kohm.	Connect to +/-1% accuracy resister
21	NC	-				Note 1)
22	EQCAP	I/O	ANALOG	100nF		Connect to +/-10% accuracy capacitance
23	EQBPS	I	TTL/CMOS			TTL/5V,CMOS/3.3V
24	NC	-				Note 1)
25	NC	-				Note 1)
26	RTIP	I	ANALOG			Input impedance between the both pins is over 2kohm.
27	RRING	I	ANALOG			
28	NC	-				Note 1)
29	TEST5	O				
30	TEST6	O				
31	NC	-				Note 1)
32	TTIP	O	ANALOG	≤15pF		
33	TAVSS	I	POWER			

Pin No.	Pin Name	I/O	Pin Type	AC Load	DC Load	Comments
34	TAVDD	I	POWER			
35	TRING	O	ANALOG	≤15pF		
36	NC	-				Note 1)
37	NC	-				Note 1)
38	TEST1	I	TTL/CMOS			TTL for 5V, CMOS for 3.3V
39	TEST2					
40	TEST3					
41	TEST4					
42	AVSS	I	POWER			
43	AVDD	I	POWER			
44	NC	-				Note 1)
45	DR6M	I	TTL/CMOS			TTL for 5V, CMOS for 3.3V
46	PS3V	I	CMOS			Note 2)
47	RESET	I	TTL/CMOS			TTL for 5V, CMOS for 3.3V
48	LPBCK	I	TTL/CMOS			TTL for 5V, CMOS for 3.3V

Note 1) Should be connected to VSS.

Note 2) Should be connected VDD for 3.3V operation or VSS for 5.0V operation.

PIN DESCRIPTIONS

Pin Name	I/O	Function	Comments
Signal Interface			
TTIP	O	**Transmit Positive Data Output**	
TRING	O	**Transmit Negative Data Output**	
TPOS	I	**Transmit Positive Data Input** Incoming data is sampled at the falling edge of TCLK	
TNEG	I	**Transmit Negative Data Input** Incoming data is sampled at the falling edge of TCLK	
TCLK	I	**Transmit clock**	
RTIP	I	**Receive Positive Data Input**	
RRING	I	**Receive Negative Data Input**	
RPOS	O	**Receive Positive Data Output** Fixed to low level during LOS status.	
RNEG	O	**Receive Negative Data Output** Fixed to low level during LOS status.	
RCLK	O	**Receive Clock Output** Fixed to low level during LOS status.	
Control Interface			
DR6M	I	**Data Rate Select** H : 6.322Mbps L : 1.544Mbps	
PS3V	I	**Power supply voltage select** H : 3.3V Supply L : 5.0V Supply	
EQBPS	I	**Equalizer bypass** H : Disable Equalizer L : Enable Equalizer	
RESET	I	**Reset** Active High input. Fixed to VSS for normal use.	
LPBCK	I	**Loop back** When LPBCK=High, TTIP and TRING are loop back to RTIP and RRING.	
LOS	O	**Loss of signal** If the incoming signal is lower than the Loss of signal threshold for more than 25 ms, LOS pin is set to High. During the loss status, if the incoming signal becomes higher than the threshold, LOS pin is set to Low within 125 us.	
TEST1-4	I	**Test pin** These pins are used only for tests. Should be fixed to low for normal use.	
TEST5,6	O	**Test pin** These pins are used only for tests. Should be float for normal use.	

Pin Name	I/O	Function	Comments
Power Supply			
DVSS	I	**Negative Power Supply for Digital circuit**	
DVDD	I	**Positive Power Supply for Digital circuit**	
DGND	I	**Negative Power Supply for Digital circuit**	
PGND	I	**Negative Power Supply for Pad**	
RAVDD	I	**Positive Power Supply for the analog circuit**	
RAVSS	I	**Negative Power Supply for the analog circuit**	
TAVSS	I	**Negative Power Supply for analog circuit.**	
TAVDD	I	**Positive Power Supply for analog circuit.**	
AVSS	I	**Negative Power Supply for analog circuit**	
AVDD	I	**Positive Power Supply for analog circuit**	
BGREF	O	**Current reference** 12 kΩ resister should be connected between this pin and RAVSS.	
Others			
XTALOUT	O	**X-tal Input / X-tal Output** X-tal should be connected between these pins. - 1.544Mbps : 24.704MHz - 6.322Mbps : 25.248MHz 20pF is the recommended value for the external capacitance connected between each of these pins and VSS.	
XTALIN	I		
EQCAP	I/O	**Equalizer Stability Capatitor** External capacitance (100nF±10%) should be connected to stabilize equalizer.	
NC	-	**Not connected.** Must be connected to VSS except 29 and 30 pins. 29 and 30 pins must be left floating.	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units	Conditions
DC Supply	VDD	-0.3	6.5	V	Apply to TAVDD, RAVDD, AVDD, DVDD
Ground Level	VSS	0	0	V	Apply to PGND, TAVSS, RAVSS, DVSS, DGND, AVSS Note 1)
Digital Input Voltage	VDIN	PGND-0.3V	DVDD+0.3V	V	
Analog Input Voltage	VAIN	PGND-0.3V	RAVDD+0.3V	V	
Input Current	IIN	-10	10	mA	
Storage Temperature	Tstg	-55	130	°C	

Note 1) PGND ≤ TAVSS, RAVSS, DVSS, DGND, AVSS
DGND ≤ DVSS

RECOMMENDED OPERATING COMDITIONS

Parameter	Symbol	min	typ	max	Units	Conditions
DC Supply (3.3V mode)	RAVDD,TAVD	3.135	3.3	3.465	V	3.3V+/-5%
DC Supply (5.0V mode)	DDVDD,AVDD	4.75	5.0	5.25	V	5.0V+/-5%
Ambient Operating Temperature	Ta	-10	25	+70	°C	

ELECTRICAL CHARACTERISTICS

Parameter			Symbol	Min	typ	max	Units	Conditions
Power Consumption	VDD=5.0V	1.5M	PDH1		170	237	mW	Note1
		6.3M	PDH2		160	231	mW	Note1
	VDD=3.3V	1.5M	PDL1		122	174	mW	Note2
		6.3M	PDL2		99	146	mW	Note2

Note 1: 100% mark, Load 110ohm

Note 2: 100% mark, Load 75ohm

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

Parameter	Symbol	Min	typ	max	Units	Conditions
5.0V Supply (PS3V=Low)						
Digital High-Level Output Voltage	VOH	0.9DVDD			V	IOH=-40uA
Digital Low-Level Output Voltage	VOL			0.4	V	IOL=1.6mA
Digital High-Level Input Voltage	VIH	2.4			V	
Digital Low-Level Input Voltage	VIL			0.8	V	
3.3V Supply (PS3V=High)						
Digital High-Level Output Voltage	VOH	0.9DVDD			V	IOH=-40uA
Digital Low-Level Output Voltage	VOL			0.4	V	IOL=1.6mA
Digital High-Level Input Voltage	VIH	0.7DVDD			V	
Digital Low-Level Input Voltage 1	VIL			0.3DVDD	V	Except EQBPS and PS3V pin (Note3)
Digital Low-Level Input Voltage 2	VILE			0.6	V	EQBPS pin

Note 3: PS3V pin should be connected to DVDD for 3.3V Supply and to DVSS for 5.0V Supply.

RECEIVER

Parameter			Symbol	Min	Typ	Max	Units	Conditions
Input Impedance				2			kohm	
Sensitivity	1.544Mbps	Equalizer OFF		-6		0	dB	Note 1, EQBPS="H"
		Equalizer ON		-18		-6	dB	Note 1, EQBPS="L"
	6.312Mbps			-4.5		0	dB	Note 2
Loss of Signal Threshold				0.15		0.25	V_{0p}	Note 3
Allowable Consecutive Zeros				60			Bit	Note 4
S/X tolerance						16	dB	Note 5
Generated Jitter					0.02		UIpp	
Jitter Tolerance			ITU-T G.824					

Note 1: Relative value to the reference level with 110ohm cable. ($3.15V_{0p}$±0.38)

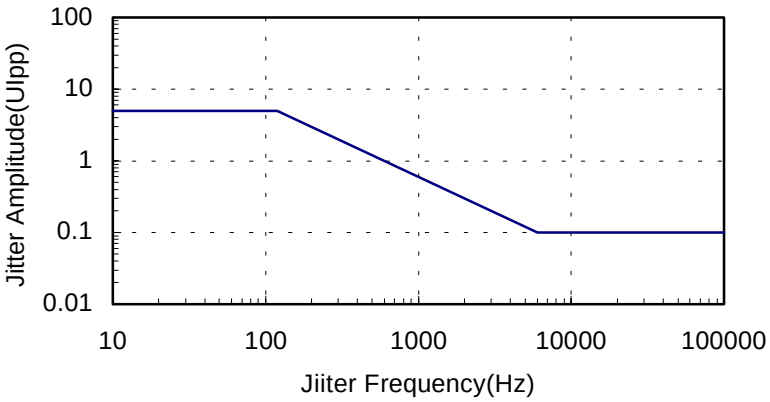
Note 2: Relative value to the reference level with 75ohm cable. ($2.0V_{0p}$±0.3%)

Note 3: Level at the line side of transformer.

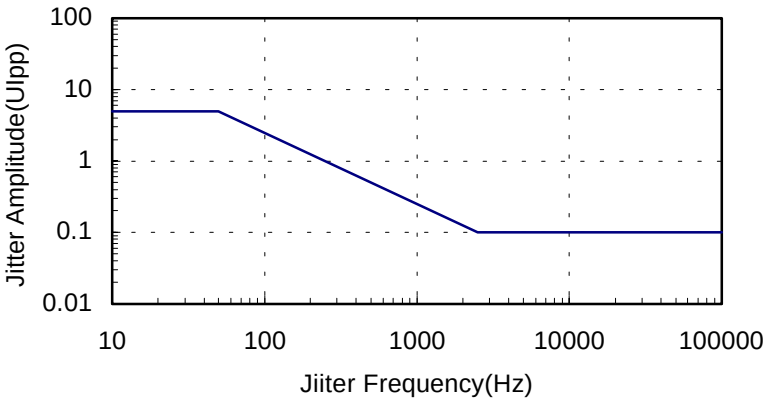
Note 4: The device will tolerate consecutive zeros with PN20 pattern.

Note 5: The frequency of interference signal is 700kHz(1.544Mbps) or 3MHz(6.312Mbps).

JITTER TOLERANCE (1.544Mbps)



JITTER TOLERANCE (6.312Mbps)



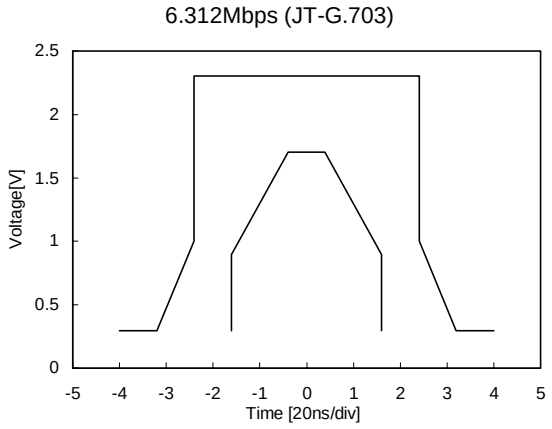
TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Units	Conditions
1.544Mbps (DR6M=Low)						
Transmit Pulse Amplitude	Va	2.77	3.15	3.53	V_{0p}	JT-G703 Note1
Transmit Pulse Width		285	324	363	Ns	
Transmit Pulse Under-Shoot		-0.25Va		-0.75Va	V_{0p}	
Transmit Data Latency from TPOS/TNEG to TTIP/TRING			0.75	1	Bit	
6.312Mbps (DR6M=High)						
Transmit Pulse Shape		JT-G703				Note2
Transmit Pulse Amplitude At Normalized point		1.7	2.0	2.3	V_{0p}	Note2
Transmit Data Latency from TPOS/TNEG to TTIP/TRING			1	1.5	bit	

Note 1: Measured at the line side of transformer terminated with 110ohm. (isolated pulse: ”1000”)

Note 2: Measured at the line side of transformer terminated with 75ohm. (isolated pulse: ”1000”)

ISOLATED PULSE MASK



AC CHARACTERISTICS (Clock/Data)

Parameter			Symbol	Min	Typ	Max	Units	Condi-tions	Notes
Clock Frequency	1.544Mbps	TCLK	fci1		1.544000		MHz	±50ppm	
	6.312Mbps		fci2		6.312000			±30ppm	
Duty Cycle		TCLK		40		60	%		Note 1
		RCLK		46		54	%		Note 1
Delay Time from RCLK to RPOS/RNEG		RCLK RPOS	t_{pd}	-20		20	ns	15pF load	Fig.1
		RNEG		-25		25	ns	50pF load	Fig.1
Setup/Hold Time from TCLK to TPOS/TNEG		TCLK TPOS TNEG	t_{su}	-15		15	ns		Fig.1
Rise Time/Fall Time		RCLK, RPOS, RNEG, LOS	t_r			10	ns	15pF load	Fig.2
			t_f			20	ns	50pF load	Fig.2

Note 1: Duty Cycle: $(t_{pwh} / (t_{pwh} + t_{pwl})) \times 100\%$

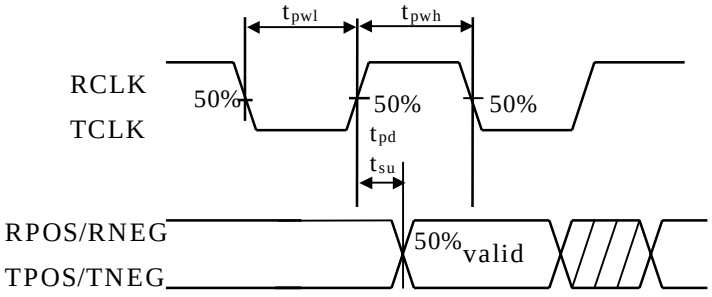


Fig. 1 Transmit/Receive Data Timing

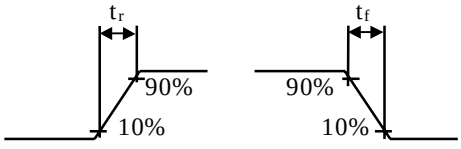


Fig. 2 Rise and Fall Time
(RCLK,RPOS,RNEG,TCLK,TPOS,TNEG)

FUNCTIONAL DESCRIPTION

POWER SUPPLY

AK2531 operates at 3.3V or 5.0V. PS3V should be set to High for 3.3V or Low for 5.0V.

PS3V pin	Power Supply
H	3.3V
L	5.0V

DATA TRANSFER RATE

AK2531 operates at the data rate of 1.544 Mbps or 6.312 Mbps. If you set DR6M pin to High, AK2531 goes into the mode for 6.312 Mbps, or if you set DR6M pin to Low, AK2531 goes into the mode for 1.544 Mbps. Depending on the data rate, MCLK pin requires 24.704 MHz for 1.544Mbps or 25.248 MHz for 6.312 Mbps.

DR6M pin	Data Transfer Rate	MCLK
H	6.312Mbps	25.248MHz
L	1.544Mbps	24.704MHz

EXTERNAL COMPONENTS

The external components shown in the table below should be connected to the appropriate pins depending on the operation voltage or data rate.

	5.0V Supply		3.3V Supply	
	1.544Mbps	6.312Mbps	1.544Mbps	6.312Mbps
Turns Ratio	1:1	1:1	1:1.4	1:1
Load Impedance	110ohm	75ohm	110ohm	75ohm
Receive side Termination	55 ohm	37.5 ohm	28 ohm	37.5 ohm
Crystal Frequency	24.704MHz	25.248MHz	24.704MHz	25.248MHz
Characteristics	Described in “Electrical Characteristics”			

PULSE SHAPER

AK2531 samples the transmit data at TPOS and TNEG pins on the falling edge of TCLK. The sampled incoming data are converted to AMI signal and output at TTIP and TRING pins. If TCLK is in loss, AMI data is set to the Space “0” and is synchronized to the Xtal.

LINE EQUALIZER

AK2531 equalizes the line loss of √f characteristics. EQBPS pin should be set as shown below.

EQBPS pin	Equalizer	Conditions of Cable
H	Bypassed	110 Ω twisted pair up to 6dB cable loss (1.544Mbps mode)
L	Enable	110 Ω twisted pair from 6dB to 18dB cable loss (1.544Mbps mode) 75 Ω coax cable up to 4.5dB cable loss (6.312Mbps mode)

LOCAL LOOPBACK

If you set LPBCK pin to High, AK2531 makes the transmit clock and the line driver output loopback to the receive clock and data input. In this mode, LOS pin is fixed to "Low".

LPBCK pin	Mode	Operation
H	Loopback	TCLK → RCLK TTIP → RTIP TRING → RRING
L	Normal Operation	

LOSS OF SIGNAL

If the received signal level is lower than the LOS threshold during 25ms(typ), AK2531 recognizes that status as Loss of signal and LOS pin goes to "high". LOS pin returns to "low" within 125us after the received signal level is beyond the LOS threshold.

The states of each pin are shown below.

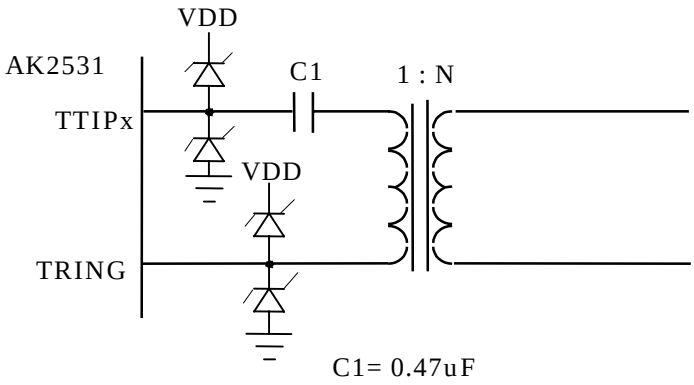
Pin name	STATE	
	Normal operation	Loss of signal
LOS	L	H
RCLK	Recovered clock	L
RPOS	Recovered positive data	L
RNEG	Recovered negative data	L

POWER ON RESET

When the power supply for AK2531 rises within 10ms, AK2531 will be in the reset state for 15ms (max : guaranteed by design).

RECOMMENDED EXTERNAL CIRCUIT

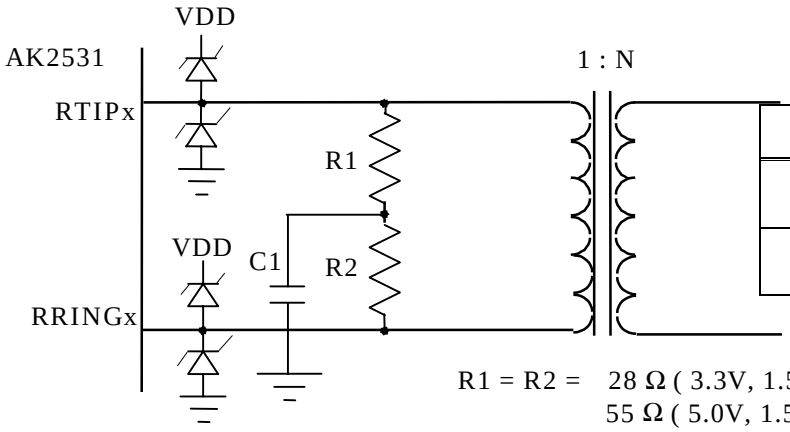
TRANSMITTER



C1= 0.47uF

1 : N	Condition
1 : 1.4	1.544Mbps, 3.3V
1 : 1	Except above

RECEIVER



1 : N	Condition
1 : 1.4	1.544Mbps, 3.3V
1 : 1	Except above

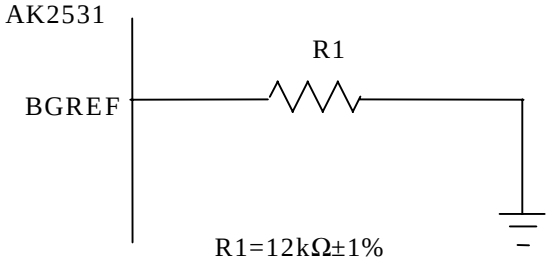
R1 = R2 = 28 Ω (3.3V, 1.544Mbps)
55 Ω (5.0V, 1.544Mbps)
37.5 Ω (6.312Mbps)

C1 = 0.47uF

REFERENCE

12 kΩ±1% resistor should be connected to determine the internal reference current.

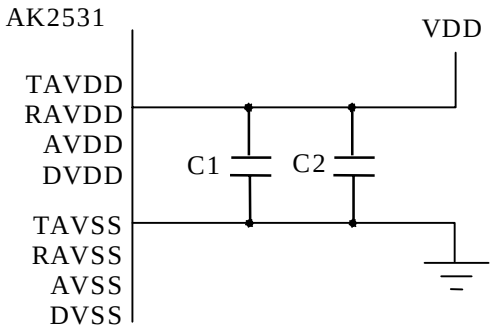
R1 is recommended to connect to AK2531 as short as possible to avoid noise.



R1=12kΩ±1%

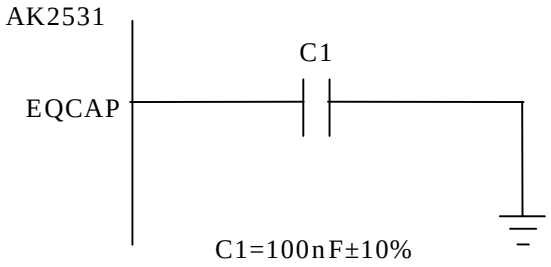
POWER SUPPLY

AK2531 has 4 paths for the power supply such as RAVDD-RAVSS,TAVDD-TAVSS,AVDD-AVSS and DVDD-DVSS. To decouple the power supplies, as shown below, C1, C2 capacitors should be connected between those power supplies respectively. These should be connected to AK2531 as short as possible. The table below shows a typical recommended value. These values depend on the condition of the power supply line on user's board. Please decide the value of the capacitors based on your evaluation.

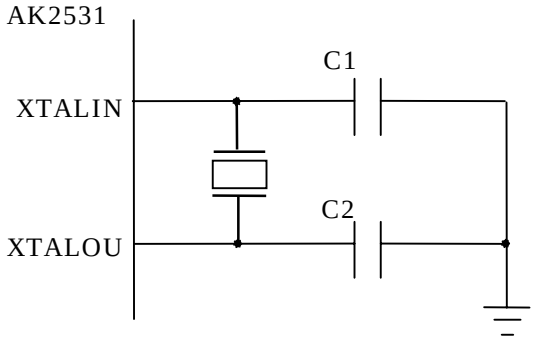


Pin name	C1	C2
RAVDD-RAVSS, AVDD-AVSS	1uF	0.1uF
DVDD-DVSS, TAVDD-TAVSS	1uF	0.01uF

EQUALIZER STABILITY CAPACITOR



X-TAL OSC



Xtal:

1.544Mbps : 24.704 MHz ± 50 ppm

6.312Mbps : 25.248 MHz ± 50 ppm

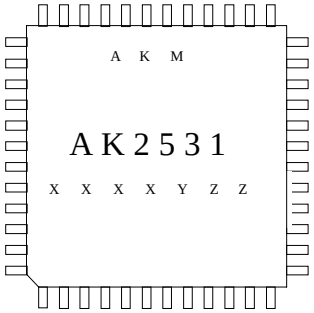
C1 = C2 = 20 pF (Max 25pF)

PACKAGE

48pin LQFP

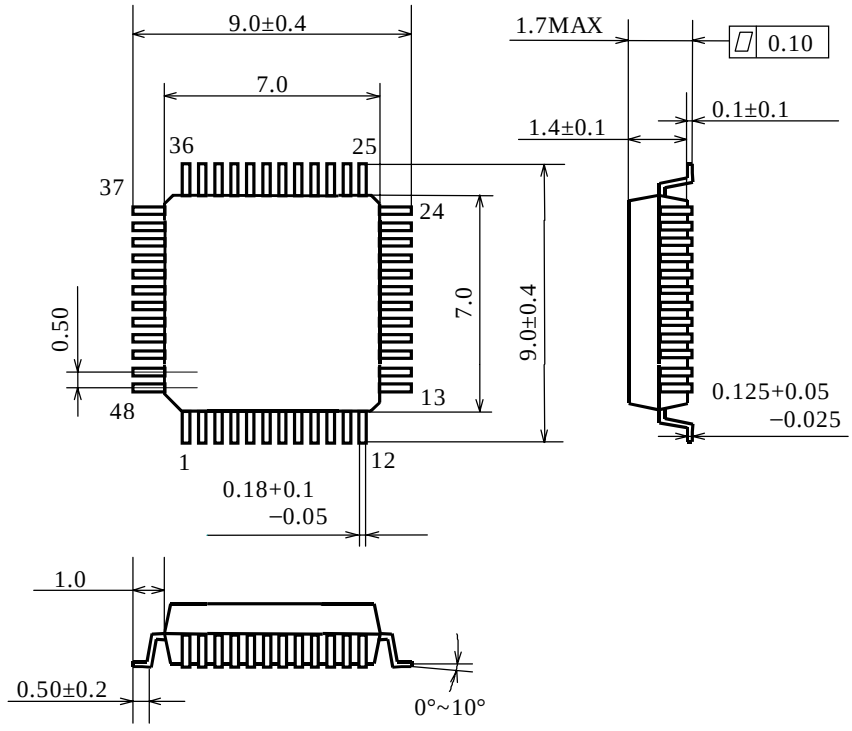
MARKING

(1)Pin #1 indication
(2)Date Code: 7digits XXXXYZZ
(3)Marketing Code: AK2531
(4)AKM Logo



OUTLINE DIMENSIONS

Units: mm



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