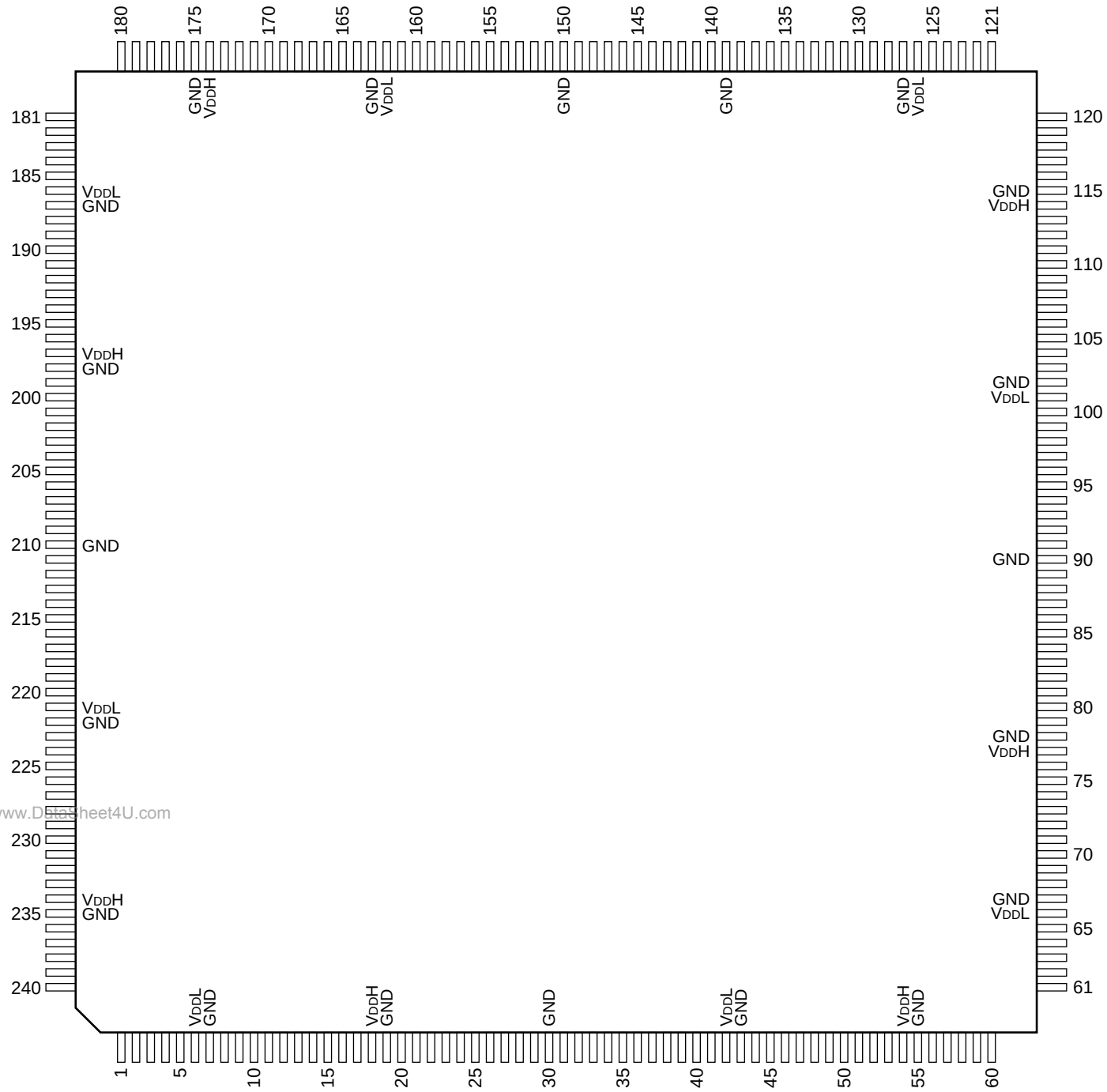
C-MOS MEMORY CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	M2CF	49	I	DID4	97	I	A2D4	145	O	MWC4	193	I/O	MAD2
2	I	M3D9	50	I	DID3	98	I	A2D3	146	O	MWC3	194	I/O	MAD1
3	I	M3D8	51	I	DID2	99	I	A2D2	147	O	MWC2	195	I/O	MAD0
4	I	M3D7	52	I	DID1	100	I	A2D1	148	O	MWC1	196	O	MPUCK
5	I	M3D6	53	I	DID0	101	—	$V_{DD}L$	149	O	MWC0	197	—	$V_{DD}H$
6	—	$V_{DD}L$	54	—	$V_{DD}H$	102	—	GND	150	—	GND	198	—	GND
7	—	GND	55	—	GND	103	I	A2D0	151	O	MWCK	199	I	R27
8	I	M3D5	56	I	DIHD	104	I	A2P	152	O	$\overline{MWRST}$	200	I	ADVCF
9	I	M3D4	57	I	DIVD	105	O	IVST	153	O	$\overline{MRCK}$	201	I	TEST
10	I	M3D3	58	I	DIP	106	I	M1D9	154	O	$\overline{MRRST}$	202	O	SRP
11	I	M3D2	59	O	CHD	107	I	M1D8	155	I	RDY9	203	O	REFCF0
12	I	M3D1	60	O	CVD	108	I	M1D7	156	I	RDY8	204	O	REFCF1
13	I	M3D0	61	I	ISY	109	I	M1D6	157	I	RDY7	205	O	REFCF2
14	I	M3HD	62	O	HR	110	I	M1D5	158	I	RDY6	206	I	FNTC
15	I	M3VD	63	I	SFTHR	111	I	M1D4	159	I	RDY5	207	I	$\overline{RST}$
16	I	M3CF	64	O	SMPP	112	I	M1D3	160	I	RDY4	208	O	R18
17	O	SAVP	65	O	PCEN	113	I	M1D2	161	O	WRSTL	209	O	SUPT
18	—	$V_{DD}H$	66	—	$V_{DD}L$	114	—	$V_{DD}H$	162	—	$V_{DD}L$	210	—	GND
19	—	GND	67	—	GND	115	—	GND	163	—	GND	211	O	BD9
20	I	DED9	68	I	W27	116	I	M1D1	164	I	RDY3	212	O	BD8
21	I	DED8	69	O	DTHP	117	I	M1D0	165	I	RDY2	213	O	BD7
22	I	DED7	70	O	CH	118	I	M1HD	166	I	RDY1	214	O	BD6
23	I	DED6	71	O	CLPP	119	I	M1VD	167	I	RDY0	215	O	BD5
24	I	DED5	72	I	A1D9	120	I	M1CF	168	I	RDP	216	O	BD4
25	I	DED4	73	I	A1D8	121	O	ICF0	169	I	RDFIN	217	O	BD3
26	I	DED3	74	I	A1D7	122	O	ICF1	170	I	RDC9	218	O	BD2
27	I	DED2	75	I	A1D6	123	O	ICF2	171	I	RDC8	219	O	BD1
28	I	DED1	76	I	A1D5	124	O	MWY9	172	I	RDC7	220	O	BD0
29	I	DED0	77	—	$V_{DD}H$	125	O	MWY8	173	I	RDC6	221	—	$V_{DD}L$
30	—	GND	78	—	GND	126	—	$V_{DD}L$	174	—	$V_{DD}H$	222	—	GND
31	I	DECCK	79	I	A1D4	127	—	GND	175	—	GND	223	O	BHD
32	I	DEHD	80	I	A1D3	128	O	MWY7	176	I	RDC5	224	O	BVD
33	I	DEVD	81	I	A1D2	129	O	MWY6	177	I	RDC4	225	O	BCF
34	I	DECF	82	I	A1D1	130	O	MWY5	178	I	RDC3	226	O	BP
35	I	DEP	83	I	A1D0	131	O	MWY4	179	I	RDC2	227	I	M2D9
36	I	DICPST	84	I	A1P	132	O	MWY3	180	I	RDC1	228	I	M2D8
37	I	DICR	85	O	YCER	133	O	MWY2	181	I	RDC0	229	I	M2D7
38	I	DICF2	86	O	BCER	134	O	MWY1	182	O	RDRSTL	230	I	M2D6
39	I	DICF1	87	O	RCER	135	O	MWY0	183	I	ASTB	231	I	M2D5
40	I	DICF0	88	O	COE	136	O	MWP	184	I	$\overline{WR}$	232	I	M2D4
41	I	DIFCK	89	O	HFCK	137	O	MWFIN	185	I	$\overline{RD}$	233	I	M2D3
42	—	$V_{DD}L$	90	—	GND	138	—	$V_{DD}H$	186	—	$V_{DD}L$	234	—	$V_{DD}H$
43	—	GND	91	O	QTCK	139	—	GND	187	—	GND	235	—	GND
44	I	DID9	92	I	A2D9	140	O	MWC9	188	I/O	MAD7	236	I	M2D2
45	I	DID8	93	I	A2D8	141	O	MWC8	189	I/O	MAD6	237	I	M2D1
46	I	DID7	94	I	A2D7	142	O	MWC7	190	I/O	MAD5	238	I	M2D0
47	I	DID6	95	I	A2D6	143	O	MWC6	191	I/O	MAD4	239	I	M2HD
48	I	DID5	96	I	A2D5	144	O	MWC5	192	I/O	MAD3	240	I	M2VD

INPUT

A1D0 - 9 ; A/D CONVERTED Y SIGNAL DATA FROM DIGITAL FILTER
A1P ; A/D CONVERTED Y SIGNAL DATA PARITY
A2D0 - 9 ; A/D CONVERTED R-Y/B-Y SIGNAL DATA FROM DIGITAL FILTER
A2P ; A/D CONVERTED R-Y/B-Y SIGNAL DATA PARITY
ADVCF ; ADVANCED REFERENCE COLOR FRAME
ASTB ; MPU INTERFACE ADDRESS STROBE
DECK ; COMPOSITE DECODER INPUT CLOCK
DECF ; COMPOSITE DECODER INPUT CF
DED0 - 9 ; COMPOSITE DECODER INPUT DATA
DEHD ; COMPOSITE DECODER INPUT HD
DEP ; COMPOSITE DECODER INPUT PARITY
DEVD ; COMPOSITE DECODER INPUT VD
DICF0 - 2 ; DIF (SERIAL DIGITAL) INPUT CF
DICPST ; DIF (SERIAL DIGITAL) INPUT COMPOSITE FLAG (H : COMPOSITE)
DICR ; DIF (SERIAL DIGITAL) INPUT CRCC ERROR FLAG (H : ERROR)
DID0 - 9 ; DIF (SERIAL DIGITAL) INPUT DATA
DIFCK ; DIF (SERIAL DIGITAL) INPUT CLOCK
DIHD ; DIF (SERIAL DIGITAL) INPUT HD
DIP ; DIF (SERIAL DIGITAL) INPUT PARITY
DIVD ; DIF (SERIAL DIGITAL) INPUT VD
FNTC ; FORCED NTSC MODE
ISY ; ANALOG COMPONENT SYNC INPUT
M1CF ; MULTI-LOOP (1) INPUT CF FOR SELF-DIAG.
M1D0 - 9 ; MULTI-LOOP (1) INPUT DATA FOR SELF-DIAG.
M1HD ; MULTI-LOOP (1) INPUT HD FOR SELF-DIAG.
M1VD ; MULTI-LOOP (1) INPUT VD FOR SELF-DIAG.
M2CF ; MULTI-LOOP (2) INPUT CF
M2D0 - 9 ; MULTI-LOOP (2) INPUT DATA
M2HD ; MULTI-LOOP (2) INPUT HD
M2VD ; MULTI-LOOP (2) INPUT VD

M3CF ; MULTI-LOOP (3) INPUT COLOR FRAME FOR SELF-DIAG.
M3D0 - 9 ; MULTI-LOOP (3) INPUT DATA FOR SELF-DIAG.
M3HD ; MULTI-LOOP (3) INPUT HD FOR SELF-DIAG.
M3VD ; MULTI-LOOP (3) INPUT VD FOR SELF-DIAG.
R27 ; REFERENCE 27MHz CLOCK
RD ; MPU INTERFACE READ REQUEST
RDC0 - 9 ; MEMORY READ R-Y/B-Y DATA
RDFIN ; MEMORY READ DATA FINISH BLOCK ID BIT
RDP ; MEMORY READ DATA PARITY
RDY0 - 9 ; MEMORY READ Y DATA
RST ; MASTER RESET
SFTHR ; SHIFTED HR INPUT
TEST ; TEST MODE ENABLE
W27 ; 27MHz CLOCK LOCKED TO ANALOG COMPONENT
WR ; MPU INTERFACE WRITE REQUEST

OUTPUT

BCER	;	B-Y SIGNAL CLAMP ERROR
BCF	;	BUFFERED CF
BD0 - 9	;	BUFFERED DATA
BHD	;	BUFFERED HD
BP	;	BUFFERED PARITY
BVD	;	BUFFERED VD
CH	;	COUNT H TIMING PULSE FOR PLL
CHD	;	ANALOG COMPONENT HD OUTPUT
CLPP	;	CLAMP PULSE FOR ANALOG COMPONENT
COE	;	ANALOG COMPONENT ODD/EVEN OUTPUT
CVD	;	ANALOG COMPONENT VD OUTPUT
DTHP	;	DITHER TIMING PULSE FOR A/D DITHER
HFCK	;	13.5MHz CLOCK (W27/2) FOR DIGITAL FILTER
HR	;	PHASE COMPARATOR PULSE OUT FOR PLL
ICF0 - 2	;	SELECTED INPUT SIGNAL COLOR FRAME
IVST	;	SELECTED INPUT SIGNAL V-START PULSE
MPUCK	;	MPU INTERFACE CLOCK (9MHz)
MRCK	;	MEMORY READ CLOCK
MRRST	;	MEMORY READ RESET PULSE
MWC0 - 9	;	MEMORY R-Y/B-Y DATA OUTPUT
MWCK	;	MEMORY WRITE CLOCK
MWFIN	;	MEMORY WRITE DATA FINISH BLOCK ID BIT
MWP	;	MEMORY WRITE DATA PARITY OUTPUT
MWRST	;	MEMORY WRITE RESET PULSE
MWY0 - 9	;	MEMORY WRITE Y DATA OUTPUT
PCEN	;	PHASE COMPARATE ENABLE
QTCK	;	6.75MHz CLOCK (W27/4) FOR DIGITAL FILTER
R18	;	18MHz CLOCK OUTPUT FOR PLAYER SELF-DIAG.
RCER	;	R-Y SIGNAL CLAMP ERROR
RDRSTL	;	MEMORY READ RESET LINE
REFCF0 - 2	;	REFERENCE CF
SAVP	;	SELECTED INPUT SIGNAL SAV TIMING PULSE
SMPP	;	SAMPLING PULSE FOR PLL
SRP	;	SERVO REFERENCE PULSE
SUPT	;	TIMING PULSE FOR SET-UP REMOVER
WRSTL	;	MEMORY WRITE RESET LINE
YCER	;	Y SIGNAL CLAMP ERROR

INPUT/OUTPUT

MAD0 - 7	;	MPU INTERFACE DATA BUS