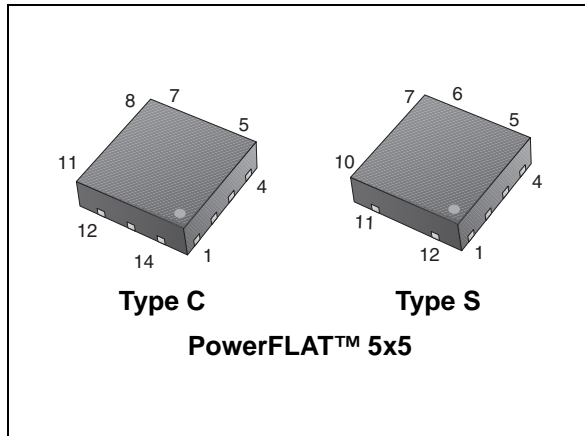


N-channel 400 V, 4.5 Ω typ., 0.43 A, SuperMESH™ Power MOSFET in a PowerFLAT™ 5x5 package

Datasheet - production data



Features

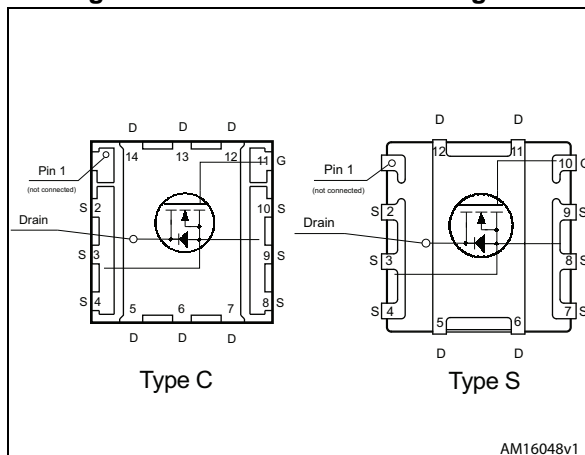
Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STL3NK40	400 V	5.5 Ω	0.43 A	2.5 W

- Extremely high dv/dt capability
- 100% avalanche rated
- Gate charge minimized
- Very low intrinsic capacitances

Applications

- Switching applications

Figure 1. Internal schematic diagram



Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STL3NK40	3NK40	PowerFLAT™ 5x5	Tape and reel

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2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	15

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	400	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	400	V
V_{GS}	Gate- source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25 \text{ }^\circ\text{C}$	0.43	A
	Drain current (continuous) at $T_{pcb} = 100 \text{ }^\circ\text{C}$	0.27	A
$I_{DM}^{(1)}$	Drain current (pulsed)	1.72	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25 \text{ }^\circ\text{C}$	2.5	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg} T_j	Storage temperature Max. operating junction temperature	-55 to 150	$^\circ\text{C}$

1. When mounted on FR-4 Board of 1 inch², 2 oz Cu ($t < 100 \text{ s}$)
2. $I_{SD} < 0.43 \text{ A}$, $di/dt < 200 \text{ A}/\mu\text{s}$, $V_{DD} < 320 \text{ V}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 Board of 1 inch², 2 oz Cu ($t < 100 \text{ s}$)

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j \text{ max}$)	0.43	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25 \text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	60	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	400			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 400\text{ V}$ $V_{DS} = 400\text{ V}$, $T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	0.8	1.6	2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.22\text{ A}$		4.5	5.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\text{ V}$, $I_D = 0.43\text{ A}$	-	1.2		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	128	200	pF
C_{oss}	Output capacitance		-	16	30	pF
C_{rss}	Reverse transfer capacitance		-	4	6	pF
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	12		Ω
Q_g	Total gate charge	$V_{DD} = 320\text{ V}$, $I_D = 1.4\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 10)	-	8.7	13	nC
Q_{gs}	Gate-source charge		-	0.9		nC
Q_{gd}	Gate-drain charge		-	3.8		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200\text{ V}$, $I_D = 0.7\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14)	-	3	-	ns
t_r	Rise time		-	4	-	ns
$t_{d(off)}$	Turn-off-delay time		-	18	-	ns
t_f	Fall time		-	16	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.43	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		1.72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.43\text{ A}$, $V_{GS} = 0$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ (see Figure 19)	-	166		ns
Q_{rr}	Reverse recovery charge		-	300		nC
I_{RRM}	Reverse recovery current		-	3.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 1.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19)	-	176		ns
Q_{rr}	Reverse recovery charge		-	340		nC
I_{RRM}	Reverse recovery current		-	3.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

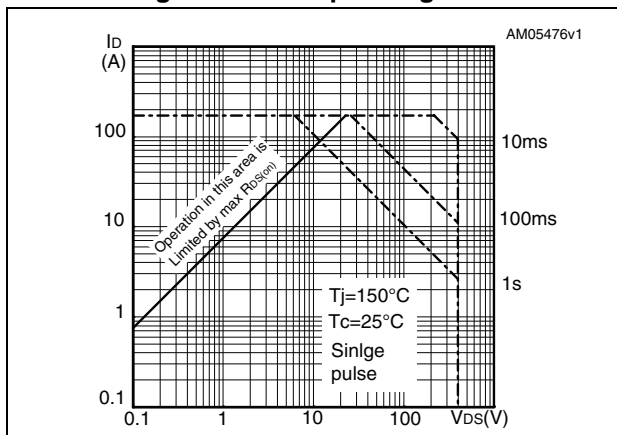


Figure 3. Thermal impedance

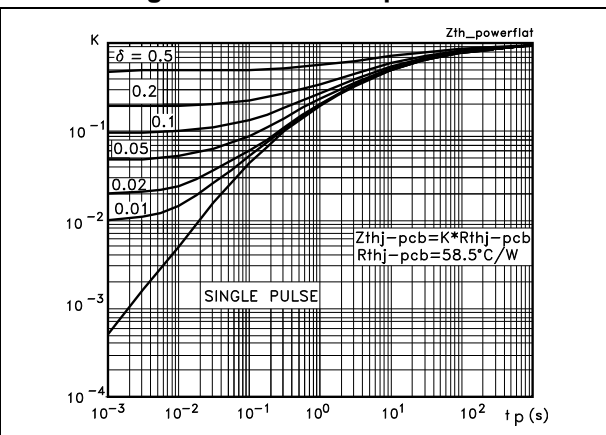


Figure 4. Saturation characteristics

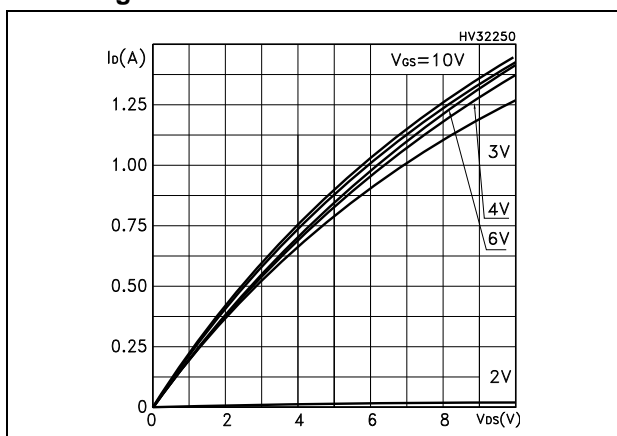


Figure 5. Transfer characteristics

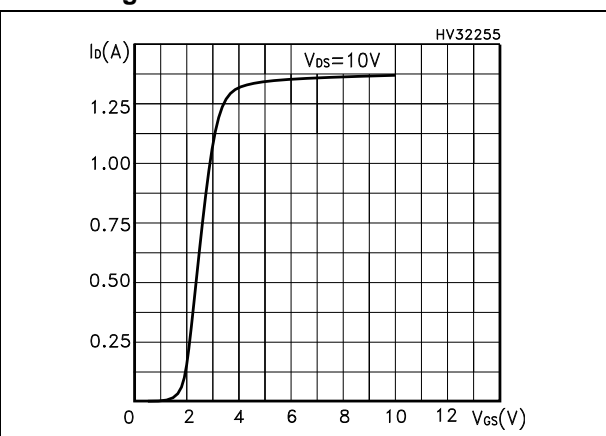


Figure 6. Output characteristics

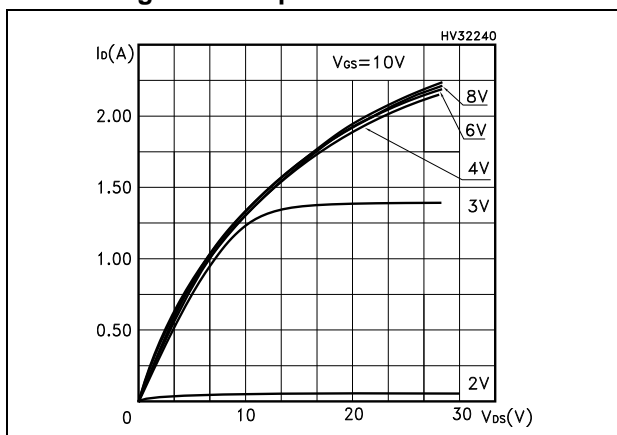


Figure 7. Static drain-source on-resistance

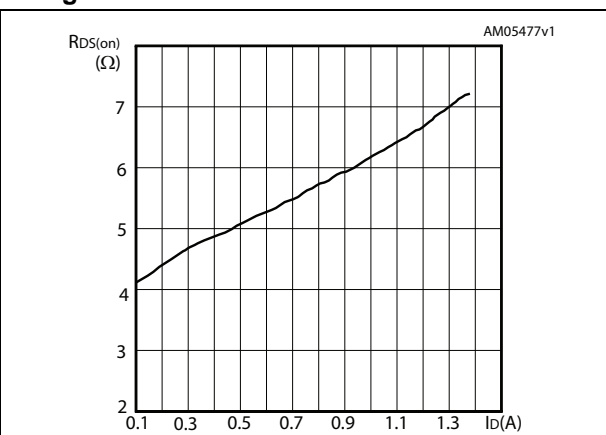


Figure 8. Gate charge vs gate-source voltage

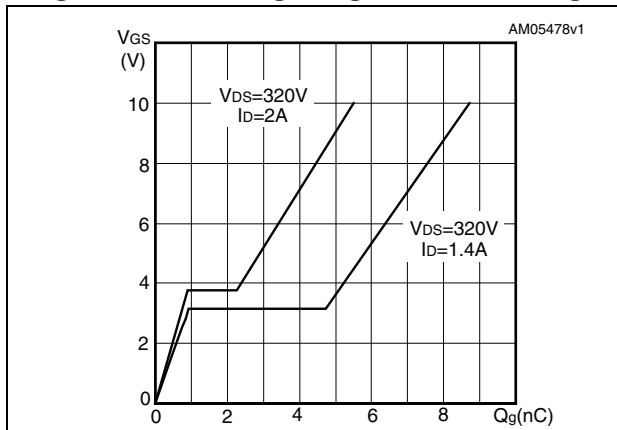


Figure 9. Capacitance variations

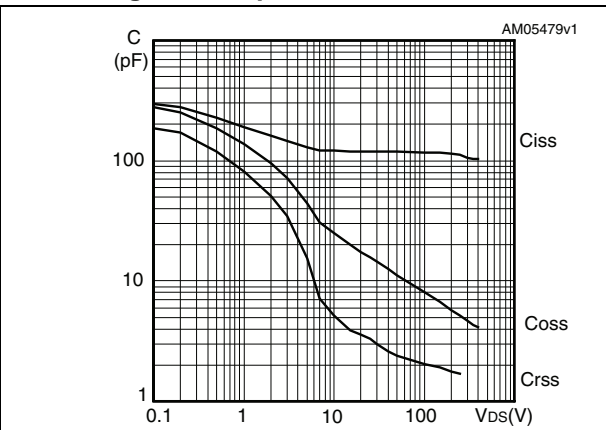


Figure 10. Transconductance

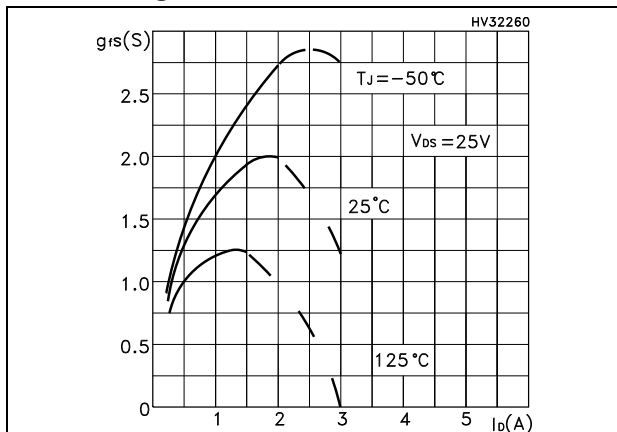


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

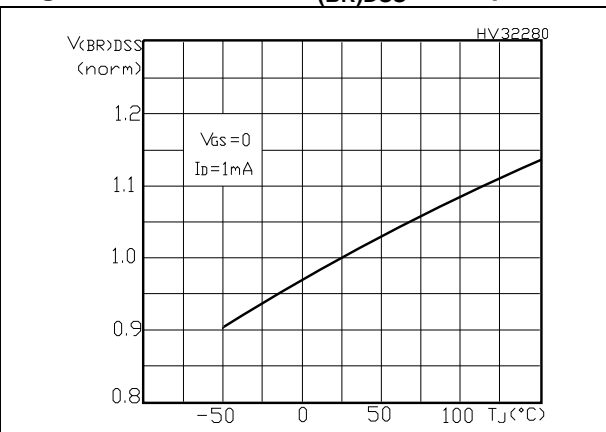


Figure 12. Normalized gate threshold voltage vs temperature

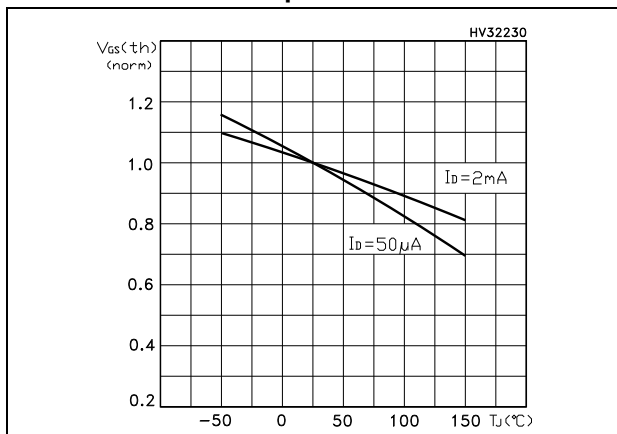
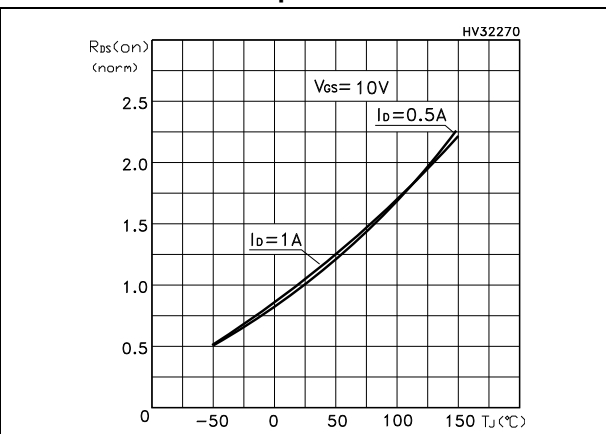


Figure 13. Normalized on-resistance vs temperature



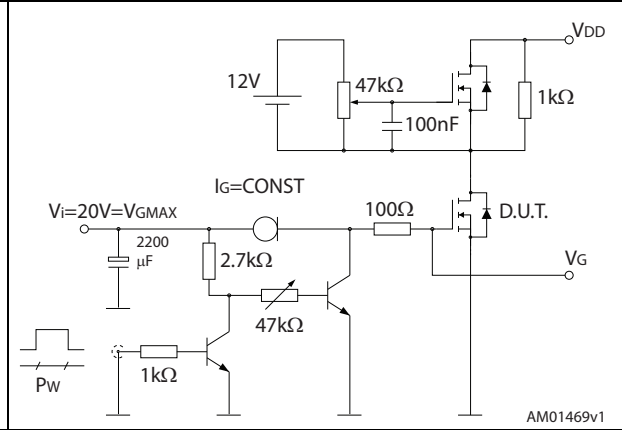
3 Test circuits

Figure 14. Switching times test circuit for resistive load



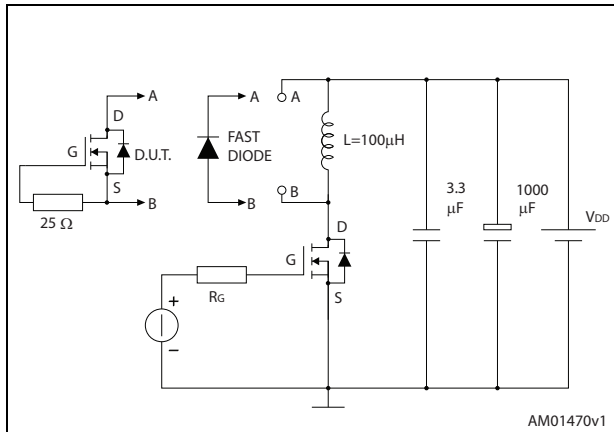
AM01468v1

Figure 15. Gate charge test circuit



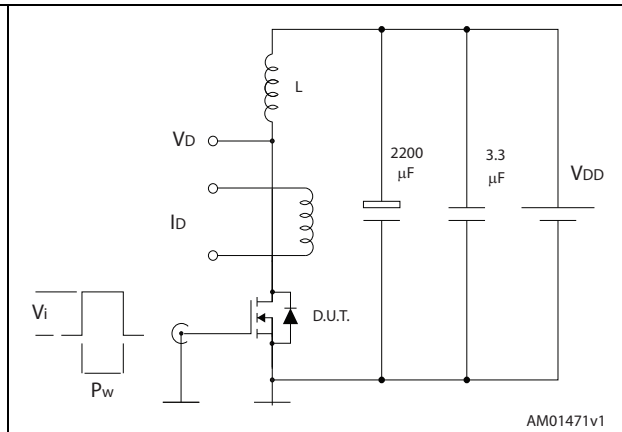
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Figure 16. Test circuit for inductive load switching and diode recovery times



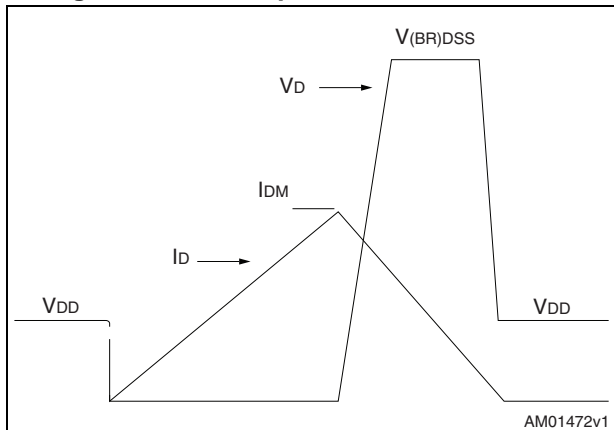
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Figure 17. Unclamped inductive load test circuit



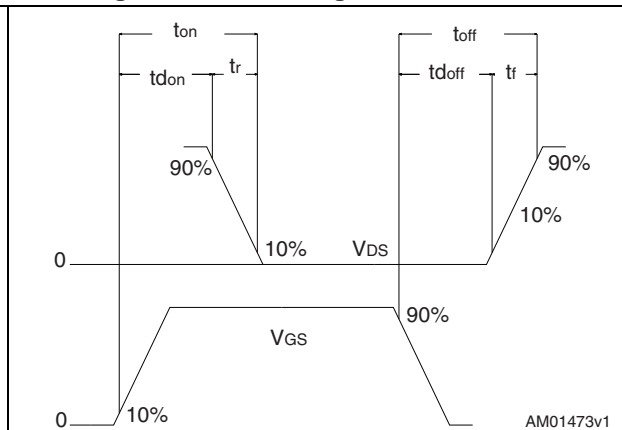
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM01473v1

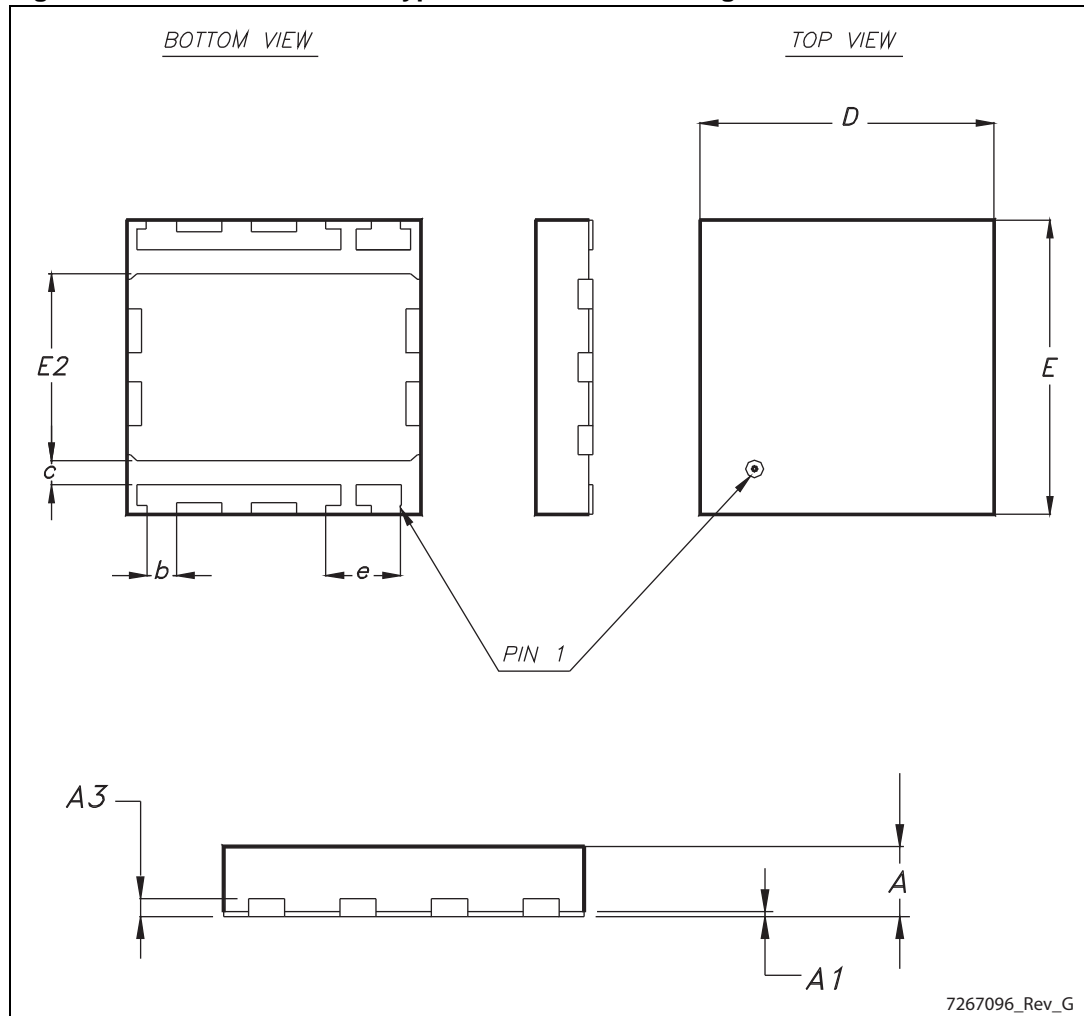
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. PowerFLAT™ 5x5 type C mechanical dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.002	0.05
A3		0.24	
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	1.22	1.27	1.32
b	0.43	0.51	0.58
E2	2.49	2.57	2.64
c	0.64	0.71	0.79

Figure 20. PowerFLAT™ 5x5 type C mechanical drawing



7267096_Rev_G

Figure 21. PowerFLAT™ 5x5 type C recommended footprint (mm)

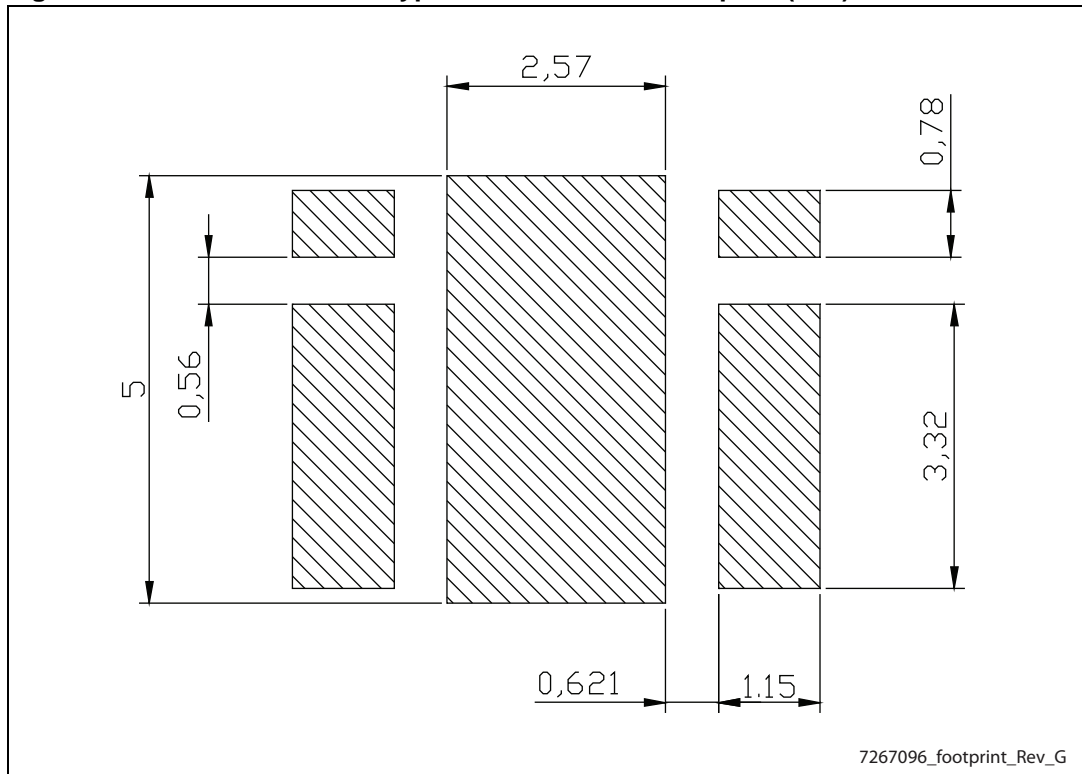


Table 10. PowerFLAT™ 5x5 type S mechanical dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.0
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.00	
D1	4.05		4.25
E		5.00	
E1	0.64		0.79
E2	2.25		2.45
e		1.27	
L	0.45		0.75

Figure 22. PowerFLAT™ 5x5 type S mechanical drawing

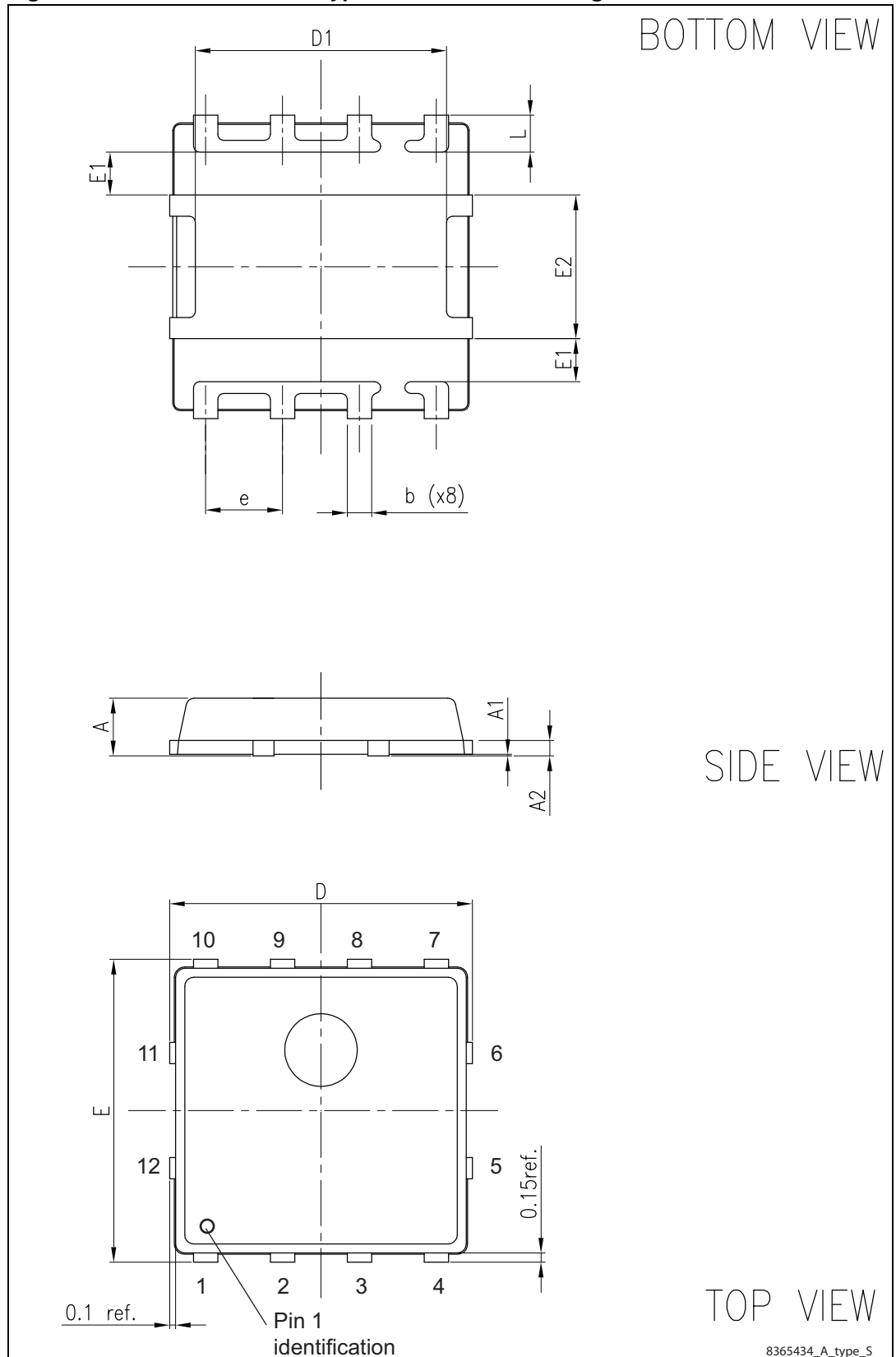
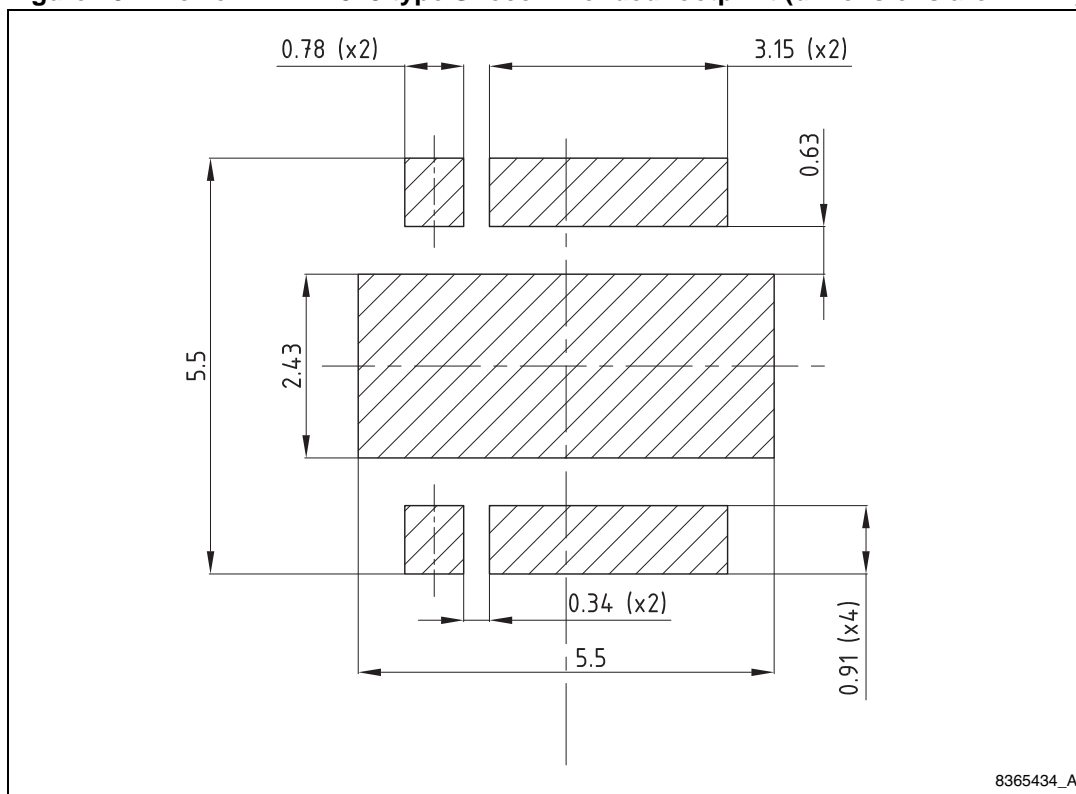


Figure 23. PowerFLAT™ 5x5 type S recommended footprint (dimensions are in mm)



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
18-Sep-2009	1	First release
29-Aug-2013	2	– Updated: Section 4: Package mechanical data – Minor text changes

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