



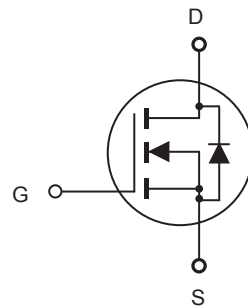
# CED840A/CEU840A

## N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

### FEATURES

- 500V, 7.5A,  $R_{DS(ON)} = 0.85\Omega$  @  $V_{GS} = 10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$	$I_D$	7.5	A
		4.7	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	30	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	$P_D$	107	W
		0.85	W/ $^\circ C$
Single Pulsed Avalanche Energy <sup>e</sup>	$E_{AS}$	196	mJ
Single Pulsed Avalanche Current <sup>e</sup>	$I_{AS}$	7.5	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.4	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ C/W$

This is preliminary information on a new product in development now .  
Details are subject to change without notice .

Rev 1. 2011.July  
<http://www.cetsemi.com>



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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	500			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 3.8A$		0.68	0.85	$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1580		pF
Output Capacitance	$C_{oss}$			125		pF
Reverse Transfer Capacitance	$C_{rss}$			15		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250V, I_D = 7A, V_{GS} = 10V, R_{GEN} = 9.1\Omega$		20	40	ns
Turn-On Rise Time	$t_r$			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			38	76	ns
Turn-Off Fall Time	$t_f$			4	8	ns
Total Gate Charge	$Q_g$	$V_{DS} = 400V, I_D = 7A, V_{GS} = 10V$		25	33.3	nC
Gate-Source Charge	$Q_{gs}$			5		nC
Gate-Drain Charge	$Q_{gd}$			6		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				7	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 7A$			1.5	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Device Mounted on FR4 Board, $t < 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d.Guaranteed by design, not subject to production testing e.L = 7mH, $I_{AS} = 7.5A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25\text{ C}$						



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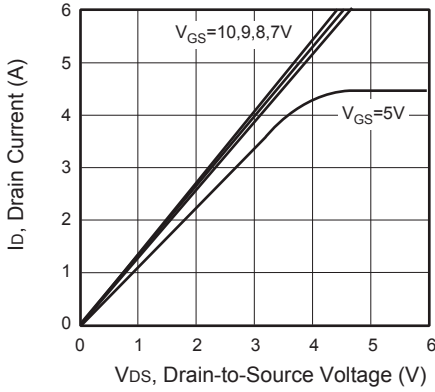


Figure 1. Output Characteristics

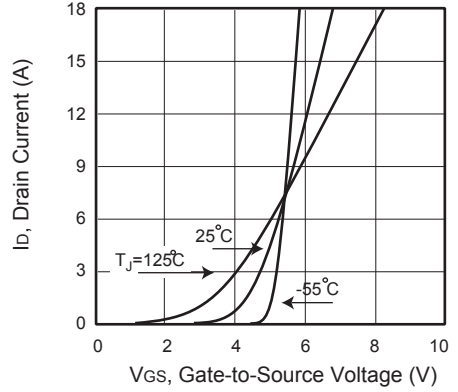


Figure 2. Transfer Characteristics

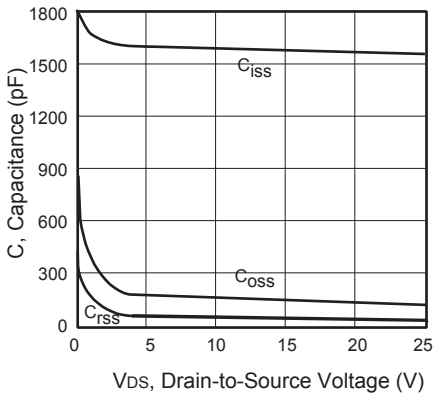


Figure 3. Capacitance

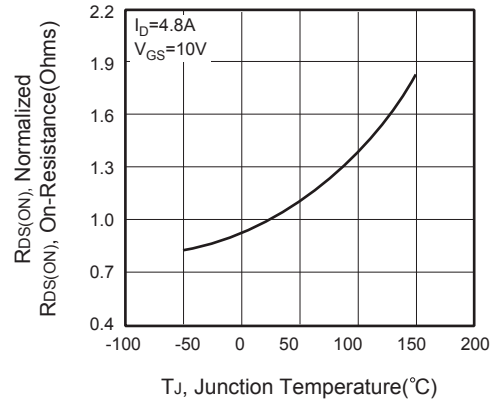


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

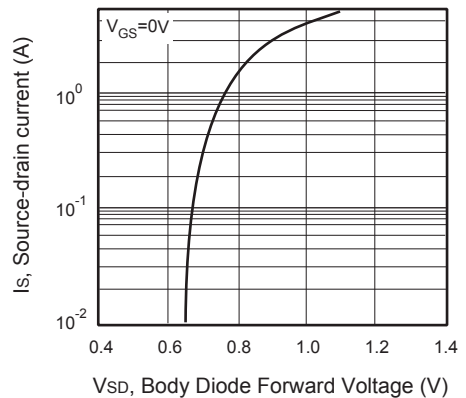


Figure 6. Body Diode Forward Voltage Variation with Source Current



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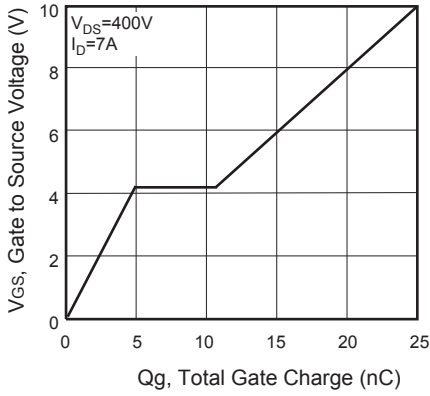


Figure 7. Gate Charge

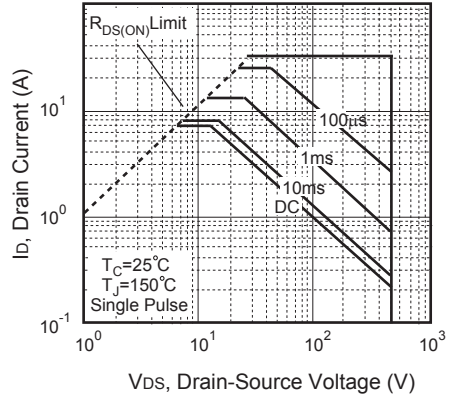


Figure 8. Maximum Safe Operating Area

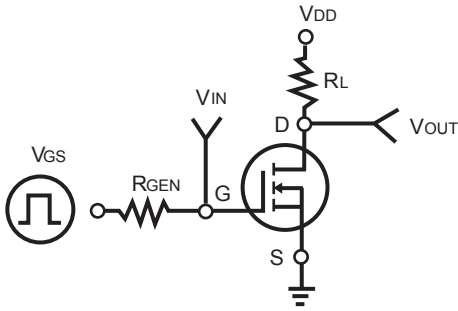


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

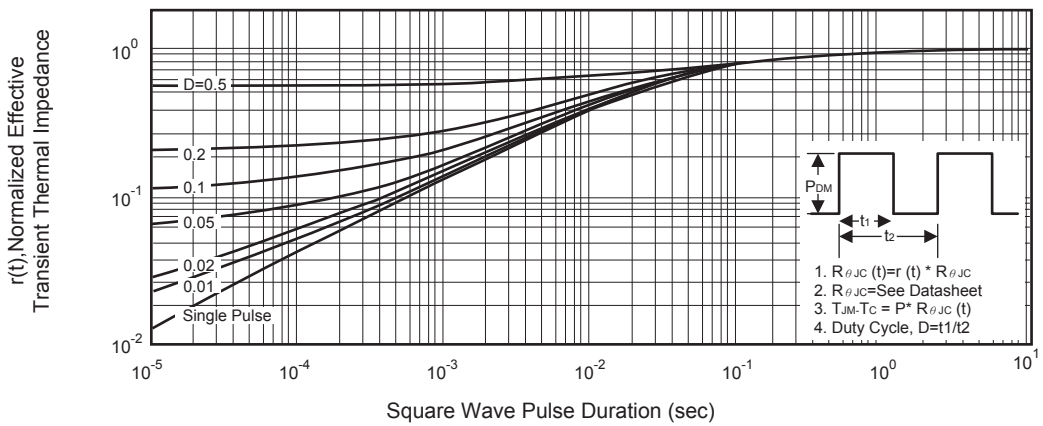


Figure 11. Normalized Thermal Transient Impedance Curve