

# MN101EA6/A5/A1/A0 Series

## 8-bit Single-chip Microcontroller

### ■ Overview

The MN101E series of 8-bit single-chip microcomputers (the memory expansion version of MN101C series) incorporate multiple types of peripheral functions. This chip series is well suited for automotive power window, camera, TV, CD, printer, telephone, home appliance, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. MN101EFA6A/A5A/A1A/A0A has an internal 32 KB of ROM and 1 KB of RAM. Peripheral functions include 5 external interrupts, including NMI, 8 timer counters, 3 (MN101EFA5/A0 series: 2) types of serial interfaces, A/D converter, watchdog timer and buzzer output (MN101EFA5/A0 series: no buzzer). The system configuration is suitable for system control microcontroller.

With 2 oscillation systems (internal frequency: 16 MHz, crystal/ceramic frequency: max. 10 MHz) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode) or PLL input (PLL mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has NORMAL mode which is based on the clock dividing  $f_{pll}$ , ( $f_{pll}$  is generated by original oscillation and PLL), by 2 ( $f_{pll}/2$ ), and the double speed mode which is based on the clock not dividing  $f_{pll}$ .

A machine cycle (minimum instruction execution time) in NORMAL mode is 200 ns when the original oscillation  $f_{osc}$  is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when  $f_{osc}$  is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

### ■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Capacitive Touch Detection Circuit	Package
MN101EFA6A	32 KB	1 KB	Flash EEPROM version	○	QFP044-P-1010F
MN101EFA1A				—	TQFP048-P-0707B
MN101EFA5A				○	SSOP032-P-0300D
MN101EFA0A				—	TQFP032-P-0707A

**■ Features**

- ROM capacity: 32 KB
- RAM capacity: 1 KB
- Package:
  - MN101EFA6/A1 series
    - 44-Pin QFP (10 mm × 10 mm / 0.8 mm pitch)
    - 48-Pin TQFP (7 mm × 7 mm / 0.5 mm pitch)
  - MN101EFA5/A0 series
    - 32-Pin TQFP (7 mm × 7 mm / 0.8 mm pitch)
    - 32-Pin SSOP (6.1 mm × 11 mm / 0.65 mm pitch)
- Machine Cycle:
  - 0.05 μs / fs: 20 MHz (4.0 V to 5.5 V)
- Oscillation circuit: 2 channel oscillation circuit
  - Internal oscillation (frc): 16 MHz
  - Crystal/ceramic (fosc): Maximum 10 MHz
- Clock Multiplication circuit (PLL Circuit)
  - PLL circuit output clock (fpll): fosc multiplied by 2, 3, 4, 5, 6, 8, 10,  
1/2 × frc multiplication by 4, 5 enable
- Clock Gear for System Clock
  - System Clock (fs): fppll divided by 1, 2, 4, 16, 32, 64, 128
- Clock Gear for control clock of peripheral function
  - Control clock of peripheral function (fppll-div): stop or fppll divided by 1, 2, 4, 8, 16
- Operation Mode:
  - NORMAL mode
  - HALT mode
  - STOP mode
  - (The operation clock can be switched in each mode.)
- Operating Voltage:
  - 4.0 V to 5.5 V
- Operation ambient temperature:
  - 40 °C to +85 °C

**■ Features (continued)**

## • Interrupt:

MN101EFA6 series: 27 levels

MN101EFA1 series: 23 levels

MN101EFA5 series: 25 levels

MN101EFA0 series: 21 levels

## &lt;Non-maskable interrupt&gt;

Non-maskable interrupt and Watchdog timer overflow interrupt

## &lt;Timer interrupts&gt;

Timer 0 interrupt

Timer 1 interrupt

Timer 2 interrupt

Timer 6 interrupt

Time base timer interrupt

Timer 7 interrupt

Timer 7 compare register 2 match interrupt

Timer 9 overflow interrupt

Timer 9 underflow interrupt

Timer 9 compare register 2 match interrupt

## &lt;Serial Interface interrupts&gt;

Serial interface 0 interrupt

Serial interface 0 UART reception interrupt

Serial interface 1 interrupt (MN101EFA5/A0 series don't have this function)

Serial interface 1 UART reception interrupt (MN101EFA5/A0 series don't have this function)

Serial interface 4 interrupt

Serial interface 4 stop condition interrupt

## &lt;A/D interrupt&gt;

A/D conversion interrupt

## &lt;External interrupts&gt;

IRQ0: Edge selectable, noise filter connection available

IRQ1: Edge selectable, noise filter connection available

IRQ2: Edge selectable, noise filter connection available, both edges interrupt

IRQ3: Edge selectable, noise filter connection available, both edges interrupt

IRQ4: Edge selectable, noise filter connection available, both edges interrupt, Key scan interrupt

## &lt;Touch Detect interrupts&gt;

Touch detect interrupt

Touch detect error interrupt

Touch round interrupt

Touch data transmission interrupt

(MN101EFA1/A0 series don't have this function)

## ■ Features (continued)

- Timer counter: 8 timers

- 8-bit timer for general use × 3 sets

- 16-bit timer for general use × 1 set

- Motor control 16-bit timer × 1 set

- 8-bit free-run timer × 1 set

- Time base timer × 1 set

- Baud rate timer × 1 set

Timer 0 (8-bit timer for general use)

- Square wave output (Timer pulse output)

- Added pulse (2-bit) type PWM output can be output to large current pin TM0IOB

- Event count

- Simple pulse measurement

- Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, External clock, Timer A output

Timer 1 (8-bit timer for general use)

- Square wave output (Timer pulse output) can be output to large current pin TM1IOB

- Event count

- 16-bit cascade connected (with Timer 0)

- Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, External clock, Timer A output

Timer 2 (8-bit timer for general use)

- Square wave output (Timer pulse output)

- Added pulse (2-bit) type PWM output can be output to large current pin TM2IOB

- Event count

- Simple pulse measurement

- 24-bit cascade connected (with Timer 0 and Timer 1)

- Clock source: fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, External clock, Timer A output

Timer 6 (8-bit free-run timer, Time base timer)

- 8-bit free-run timer

- Clock source: fpll-div, fpll-div/2<sup>12</sup>, fpll-div/2<sup>13</sup>, fs

- Time base timer

- Interrupt generation cycle: fpll-div/2<sup>7</sup>, fpll-div/2<sup>8</sup>, fpll-div/2<sup>9</sup>, fpll-div/2<sup>10</sup>, fpll-div/2<sup>13</sup>, fpll-div/2<sup>15</sup>

Timer 7 (16-bit timer for general use)

- Square wave output (Timer pulse output)

- High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOB

- Event count

- Input capture function (Both edges can be operated)

- Clock source: fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,

- Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer 9 (Motor control 16-bit timer)

- Square wave output (Timer pulse output)

- Event count

- Complementary 3-phase PWM output can be output to large current pin TM9OD0 to TM9OD5

- (Triangle wave and saw tooth wave are supported, dead time insertion available)

- Clock source: fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,

- Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

## ■ Features (continued)

- Timer counter (continued)

Timer A (Baud rate timer)

Clock output for peripheral functions

Clock source:  $f_{pll-div}$ ,  $f_{pll-div}/2$ ,  $f_{pll-div}/4$ ,  $f_{pll-div}/8$ ,  $f_{pll-div}/16$ ,  $f_{pll-div}/32$ ,  $f_s/2$ ,  $f_s/4$

- Watchdog timer

Time-out cycle can be selected from  $f_s/2^{16}$ ,  $f_s/2^{18}$ ,  $f_s/2^{20}$

On detection of 2 errors, forcibly hard reset inside LSI.

Operation start timing is selectable. (At reset release or write to register)

- Buzzer Output/ Reverse Buzzer Output

Output frequency can be selected from  $f_{pll-div}/2^9$ ,  $f_{pll-div}/2^{10}$ ,  $f_{pll-div}/2^{11}$ ,  $f_{pll-div}/2^{12}$ ,  $f_{pll-div}/2^{13}$ ,  $f_{pll-div}/2^{14}$

- A/D Converter:

10-bit × 12 channels (MN101EFA6/A1 series)

10-bit × 8 channels (MN101EFA5/A0 series)

- Serial Interface:

3 channels (MN101EFA6/A1 series)

2 channels (MN101EFA5/A0 series)

Serial 0: UART (full duplex)/ Clock synchronous

Clock synchronous serial interface

Transfer clock source:  $f_{pll-div}/2$ ,  $f_{pll-div}/4$ ,  $f_{pll-div}/16$ ,  $f_{pll-div}/64$ ,  $f_s/2$ ,  $f_s/4$ ,

Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock

MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.

Sequence transmission, reception or both are available

Full duplex UART

Baud rate timer, selected from Timer 0 to 2 or Timer A

Parity check, overrun error/ framing error detection

Transfer size 7 to 8 bits can be selected

Serial 1: UART (full duplex)/ Clock synchronous (MN101EFA5/A0 series don't have this function)

Clock synchronous serial interface

Transfer clock source:  $f_{pll-div}/2$ ,  $f_{pll-div}/4$ ,  $f_{pll-div}/16$ ,  $f_{pll-div}/64$ ,  $f_s/2$ ,  $f_s/4$ ,

Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock

MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.

Sequence transmission, reception or both are available.

Full duplex UART

Baud rate timer, selected from Timer 0 to 2 or Timer A

Parity check, overrun error/ framing error detection

Transfer size 7 to 8 bits can be selected

Serial 4: Multi master IIC/ Clock synchronous

Clock synchronous serial interface

Transfer clock source:  $f_{pll-div}/2$ ,  $f_{pll-div}/4$ ,  $f_{pll-div}/16$ ,  $f_{pll-div}/32$ ,  $f_s/2$ ,  $f_s/4$ ,

Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock

MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.

Sequence transmission, reception or both are available.

Multi master IIC

7-bit slave address is settable.

General call communication mode is supported.

## ■ Features (continued)

- Automatic Reset:

Power detection level: 4.3 V (at rising), 4.2 V (at falling)

- LED Driver:

16 pins (Port 0 or Port A)

- Touch Sensor Timer:

1 unit/ 8 channels (MN101EFA1/A0 series don't have this function)

- Ports

(MN101EFA6/A1 series)

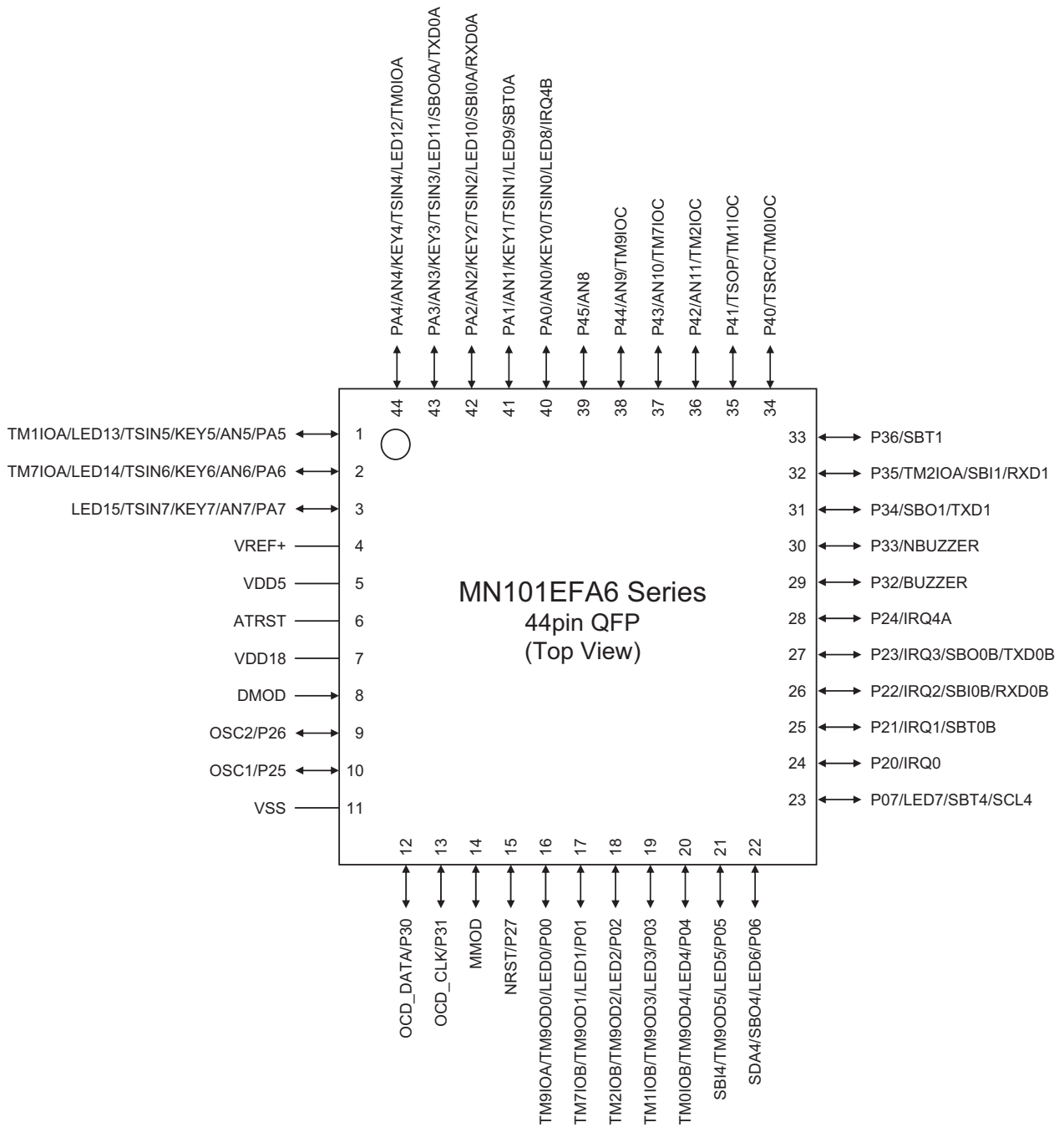
I/O ports	36 pins
Serial Interface pins	12 pins
Timer I/O	15 pins
Buzzer output pins	2 pins
A/D input pins	12 pins
External Interrupt pins	6 pins
LED (large current) driver	16 pins (Port 0 or Port A)
Touch sensor input pins	8 pins (MN101EFA1 series does not have this function)
Touch sensor resistor connect pins	2 pins (MN101EFA1 series does not have this function)
High-speed oscillation	2 pins
Special pins	8 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin
Power pins	3 pins

(MN101EFA5/A0 series)

I/O ports	24 pins
Serial Interface pins	9 pins
Timer I/O	9 pins
A/D input pins	8 pins
External Interrupt pins	5 pins
LED (large current) driver	16 pins (Port 0 or Port A)
Touch sensor input pins	8 pins (MN101EFA0 series does not have this function)
Touch sensor resistor connect pins	2 pins (MN101EFA0 series does not have this function)
High-speed oscillation	2 pins
Special pins	8 pins
Operation mode input pins	3 pins
Reset input pin	1 pin
Analog reference voltage input pin	1 pin

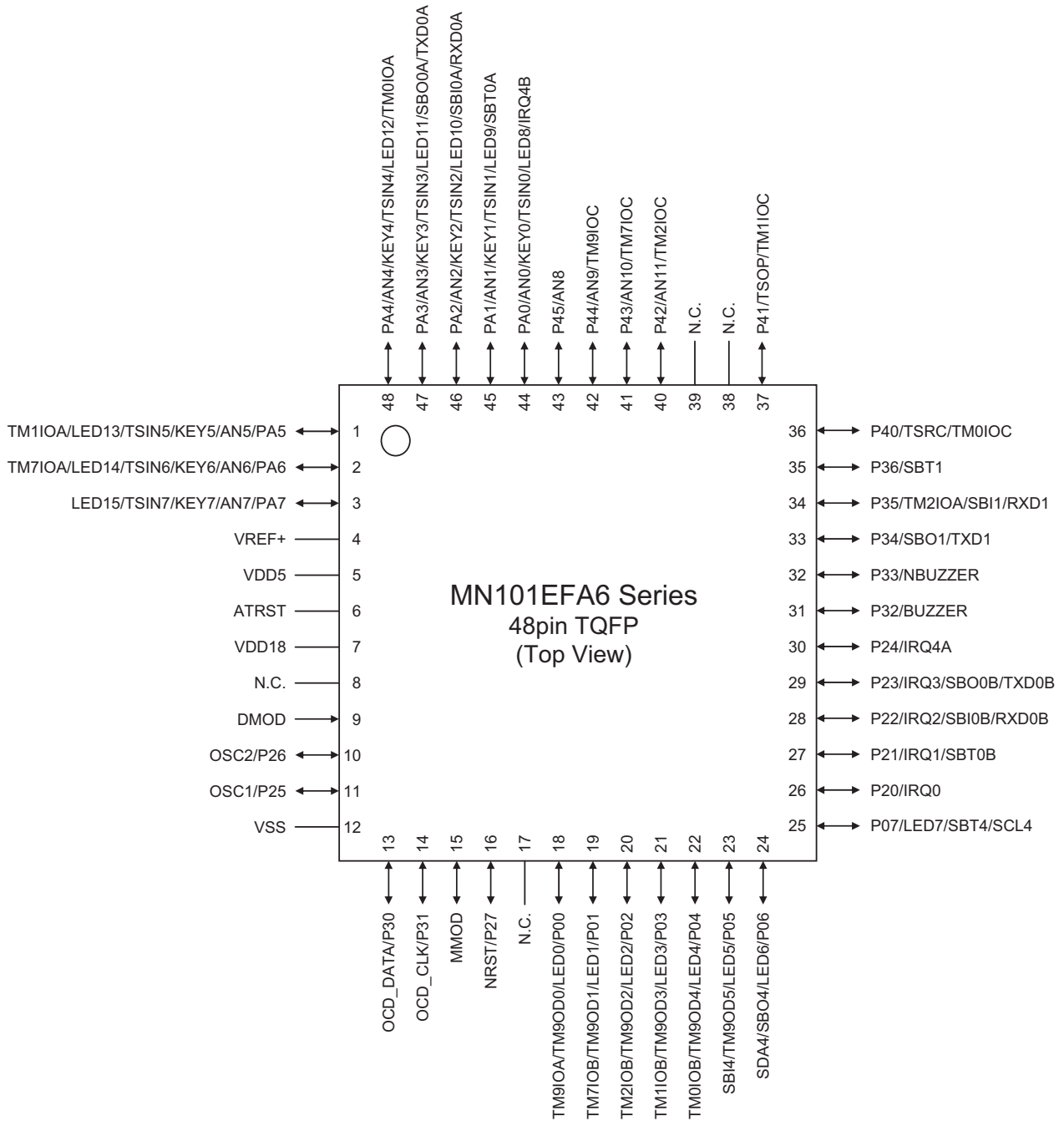
■ Pin Description

- MN101EFA6 series (QFP044-P-1010F)



■ Pin Description (continued)

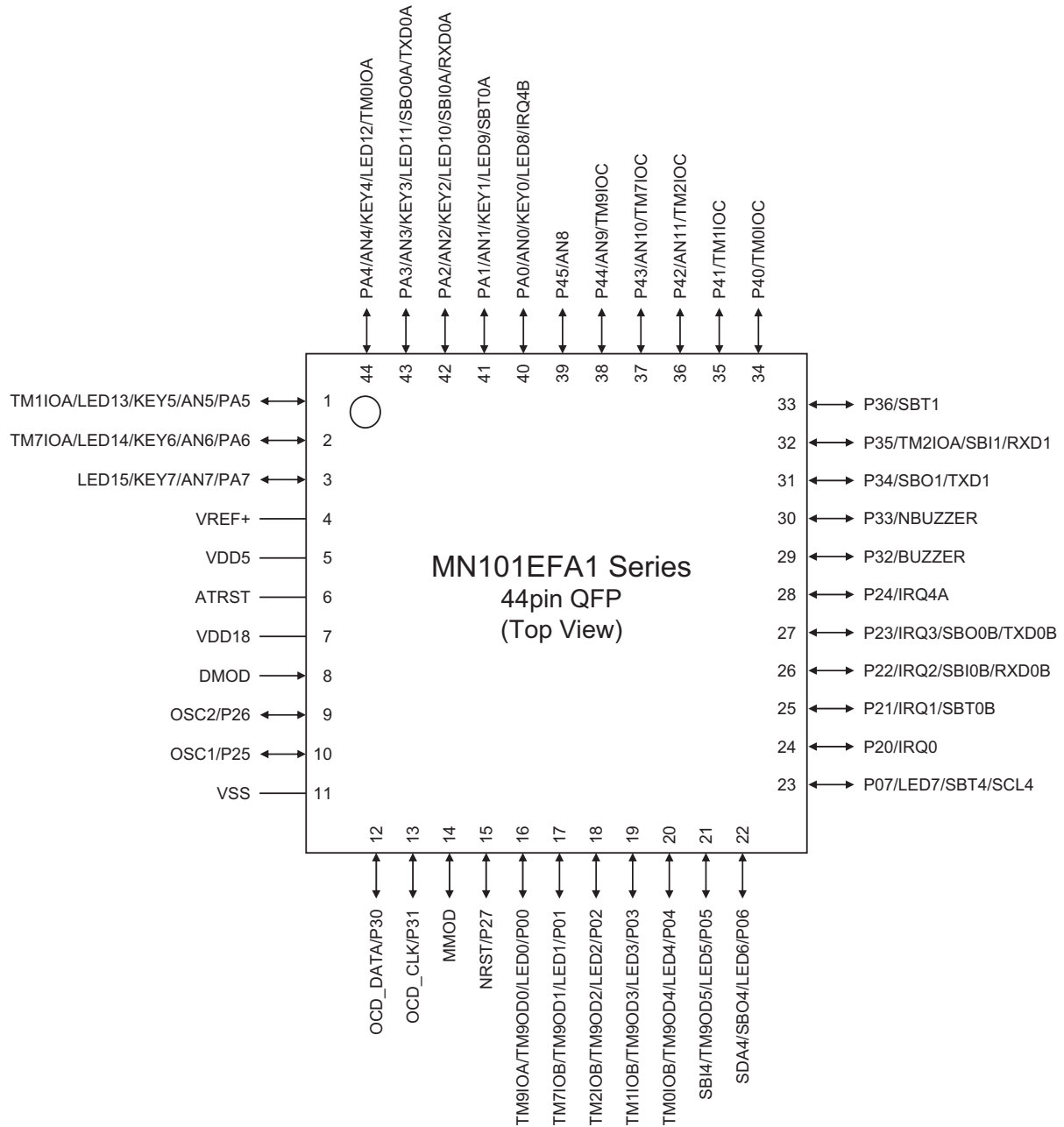
- MN101EFA6 series (TQFP048-P-0707B)





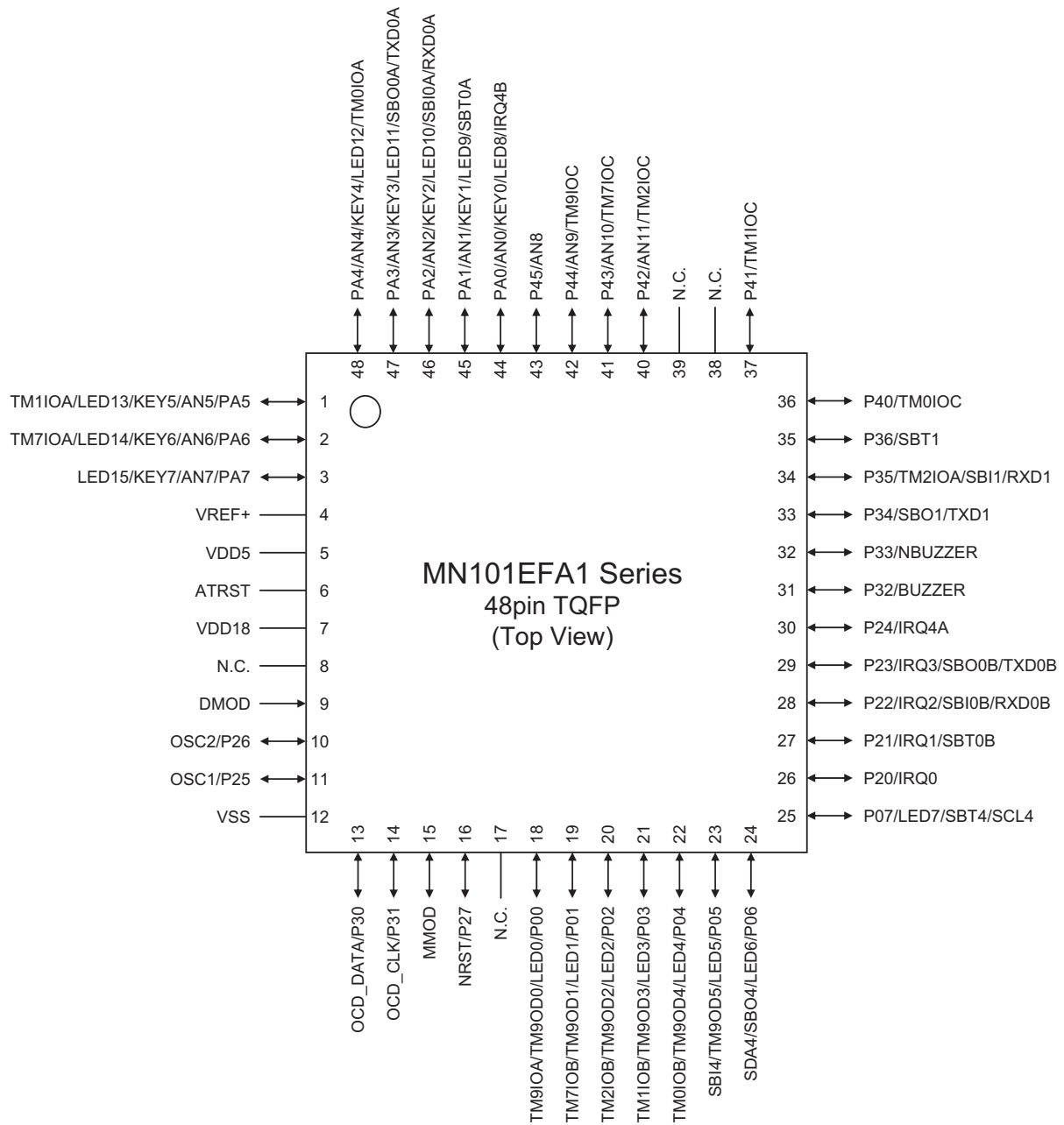
■ Pin Description (continued)

- MN101EFA1 series (QFP044-P-1010F)



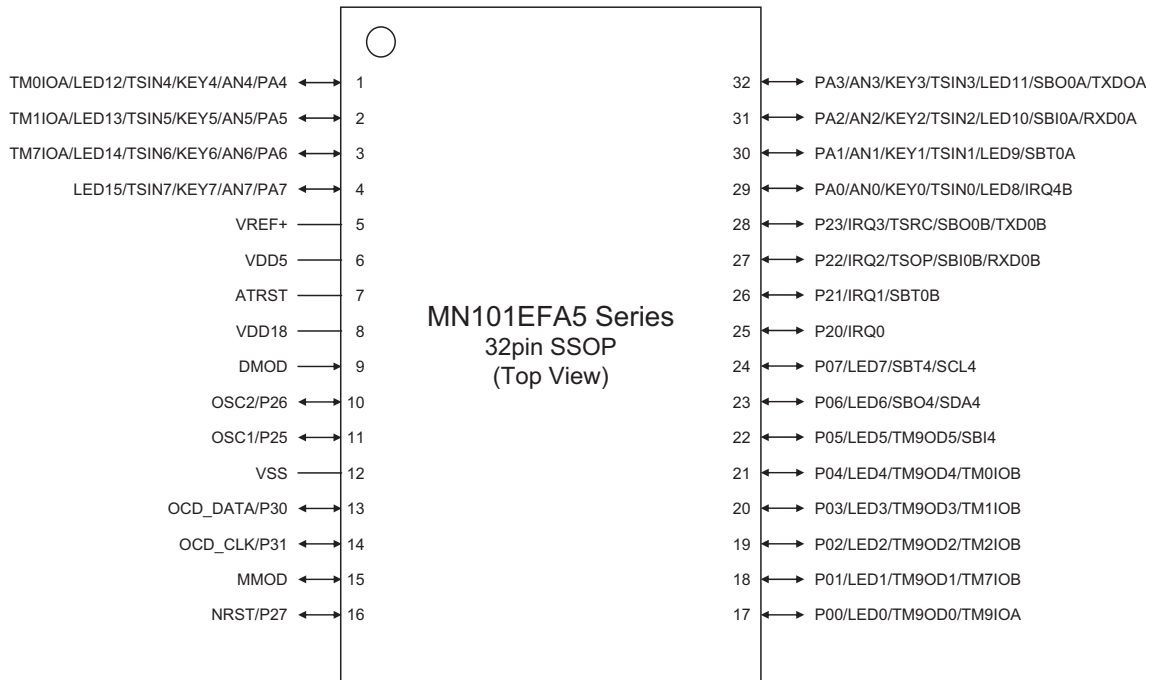
■ Pin Description (continued)

- MN101EFA1 series (TQFP048-P-0707B)

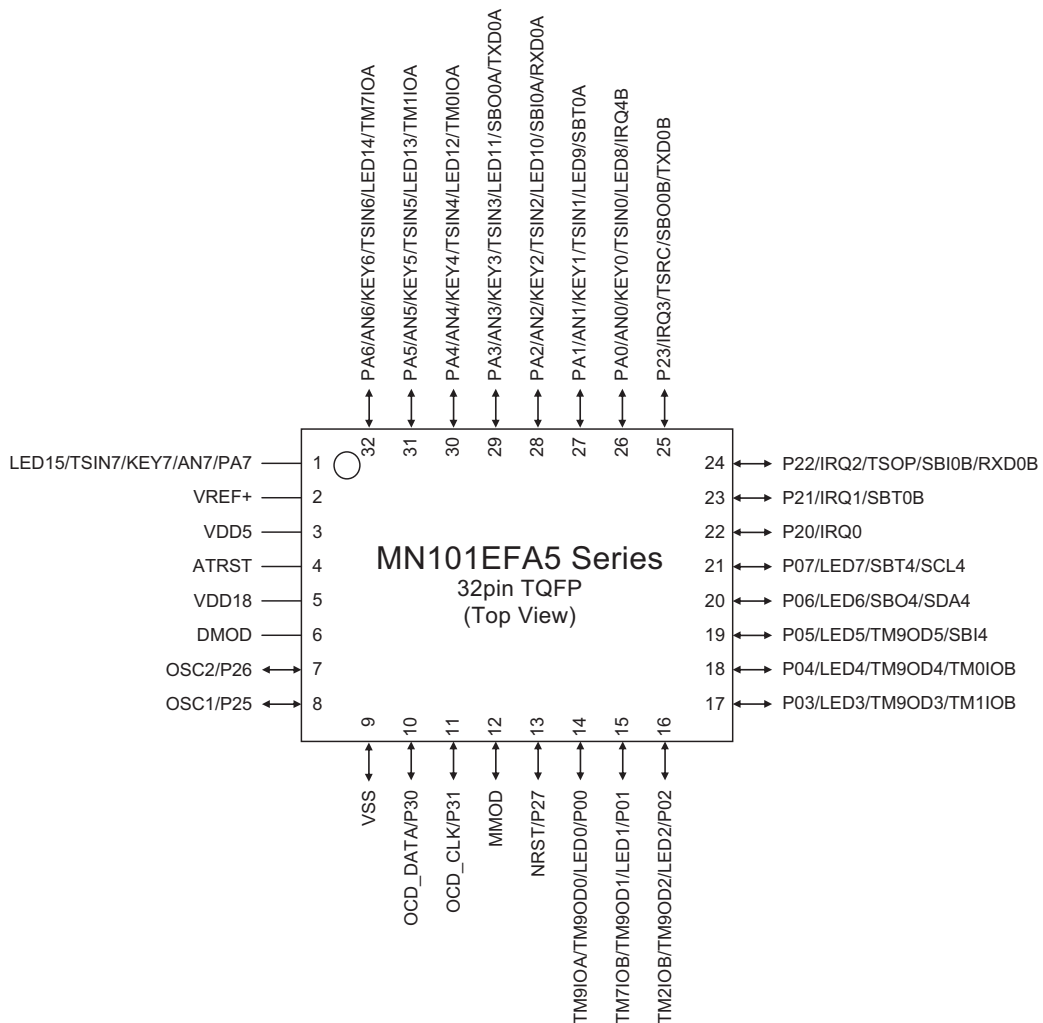


■ Pin Description (continued)

- MN101EFA5 series (SSOP032-P-0300D)

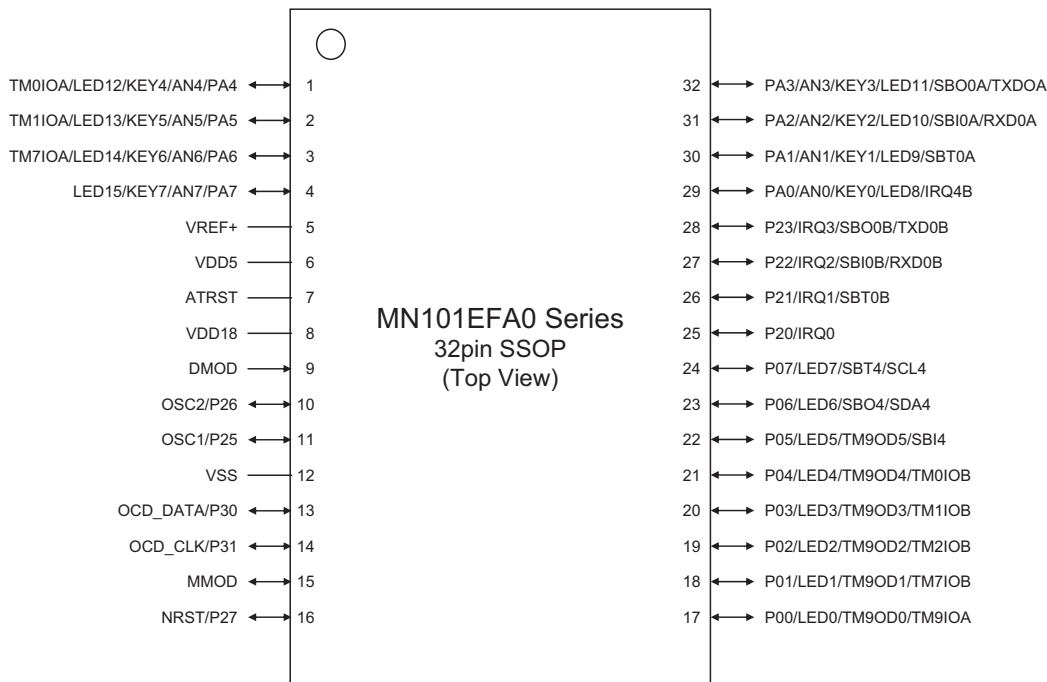


- MN101EFA5 series (TQFP032-P-0707A)

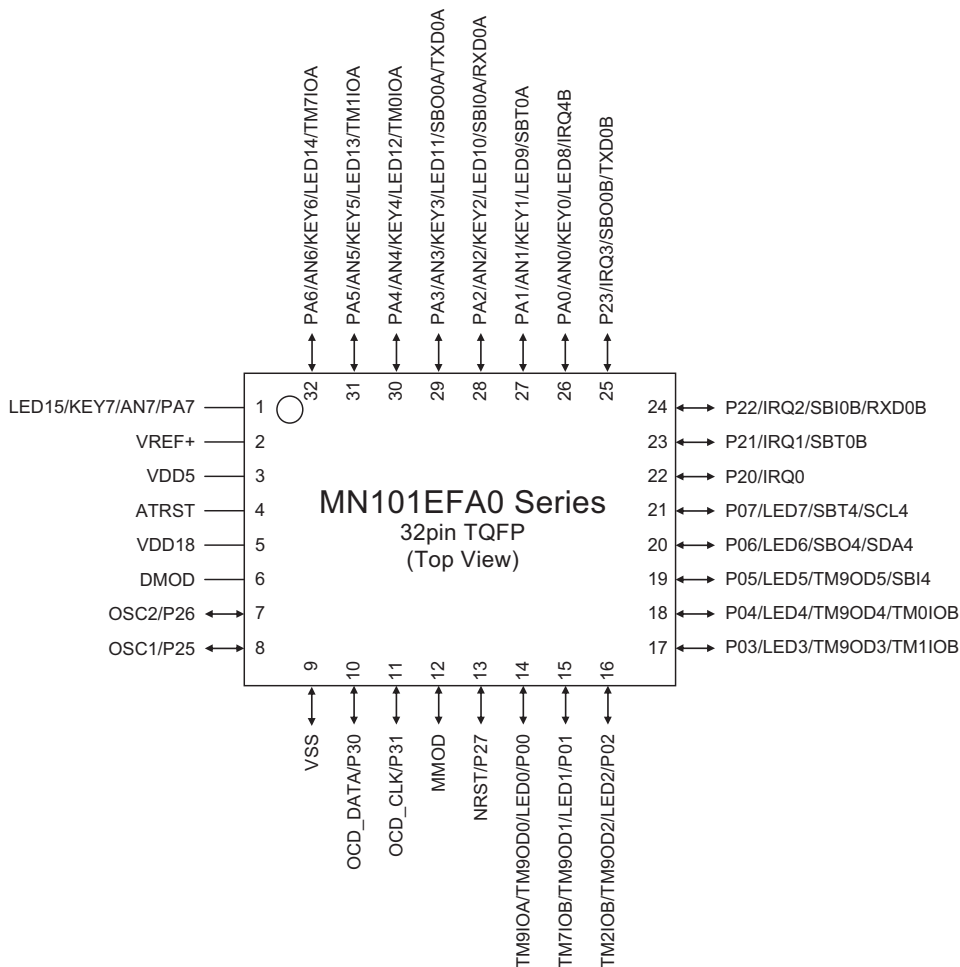


■ Pin Description (continued)

- MN101EFA0 series (SSOP032-P-0300D)



- MN101EFA0 series (TQFP032-P-0707A)



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