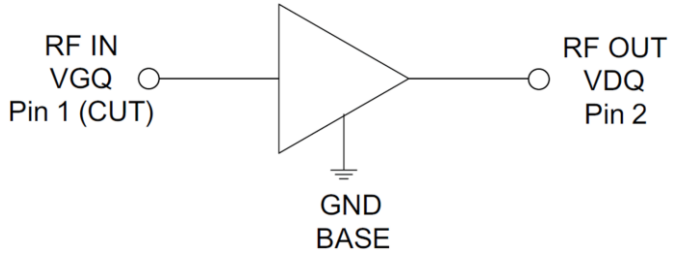
RFHA3942

35W GaN Wide-Band Power Amplifier

Package: Flanged Ceramic, 2 pin, RF360-2

The RFHA3942 is a 48V, 35W high power discrete amplifier designed for military communications, electronic warfare, general purpose broadband amplifier, commercial wireless infrastructure, and industrial/scientific/medical applications. Using a second generation advanced high power density gallium nitride (GaN) semiconductor process with improved linearity, these high-performance amplifiers achieve high efficiency, excellent linearity, and flat gain and power over a broad frequency range in a single amplifier design. The RFHA3942 is an unmatched GaN transistor, packaged in a flanged ceramic package. This package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished by incorporating simple, optimized matching networks external to the package that provide wideband gain and power performance in a single amplifier.



Functional Block Diagram

Features

- Broadband Operation
  - Tunable from DC to 4GHz
  - Instantaneous: 800MHz to 2500MHz
- Advanced GaN HEMT Technology
- Peak Modulated Power > 30W
- Advanced Heat-Sink Technology
- 48V Typical Modulated Performance
  - P_{OUT} 39.5dBm
  - Gain 16.3dB
  - Drain Efficiency 32.6%
  - ACP-40dBc
- 48V Typical CW Performance
  - P_{OUT} 45.2dBm
  - Gain 15.3dB
  - Drain Efficiency 58%
- -40°C to 85°C Operating Temperature

Applications

- Military Communications
- General Purpose Broadband Amplifiers
- Electronic Warfare
- Public Mobile Radios
- Commercial Wireless Infrastructure
- Cellular and WiMAX Infrastructure
- Industrial, Scientific, and Medical

Ordering Information

RFHA3942S2	Sample bag with 2 pieces
RFHA3942SB	Bag with 5 pieces
RFHA3942SQ	Bag with 25 pieces
RFHA3942SR	Short reel with 50 pieces
RFHA3942TR13	13” Reel with 400 pieces
RFHA3942PCBA-411	Fully assembled evaluation board optimized for 2.14GHz; 48V

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS131204

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to +2	V
Gate Current (I_G)	15	mA
Operational Voltage	50	V
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-65 to +125	°C
Operating Temperature Range (T_L)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C, 95% Confidence Limits)*	3.2E + 06	Hours
MTTF (T_J < 250°C, 95% Confidence Limits)*	5.3E + 04	Hours
Thermal Resistance, Rth (junction to case) measured at T_C = 85°C, DC bias only	3.0	°C/W

Caution! ESD sensitive device.

RoHS (Restriction of Hazardous Substances): Compliant per EU Directive 2011/65/EU.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

* MTTF – median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT (random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table above.

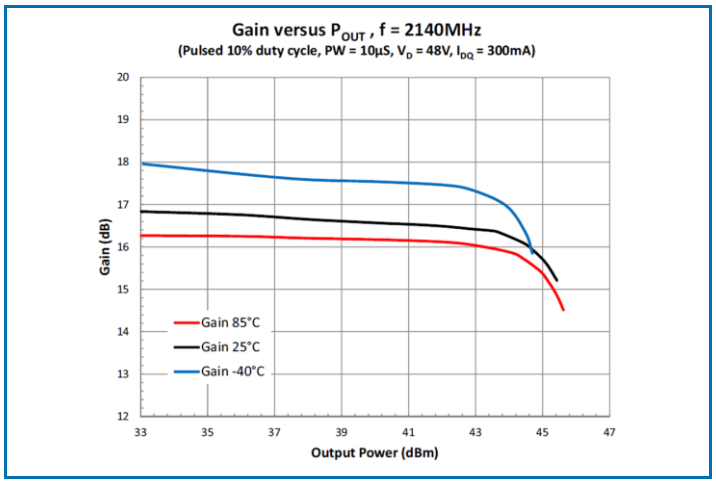
Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH\ J\text{-}C}$ and $T_C = T_{CASE}$

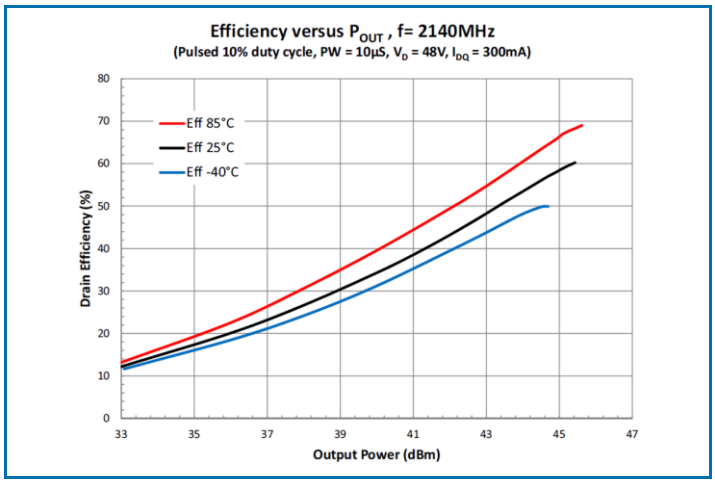
Nominal Operating Parameters

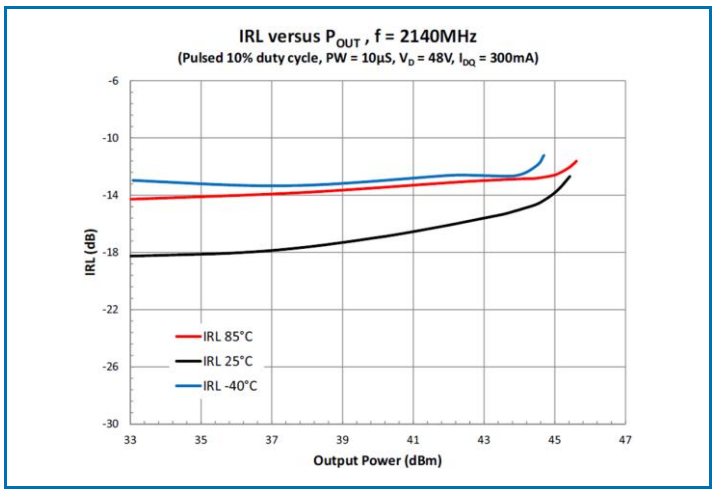
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})	28		48	V	
Gate Voltage (V_{GSQ})	-1.5	-0.9	-0.3	V	
Drain Bias Current (I_{DSQ})		300		mA	
Frequency of Operation	DC		4000	GHz	
DC Function Test					
$I_{G(OFF)}$ – Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D(OFF)}$ – Drain Leakage			2.5	mA	V_G = -8V, V_D = 48V
$V_{GS(TH)}$ – Threshold Voltage		-1.5		V	V_D = 48V, I_D = 11mA
$V_{DS(ON)}$ – Drain Voltage at High Current		1.5		V	V_G = 0V, I_D = 1.5A

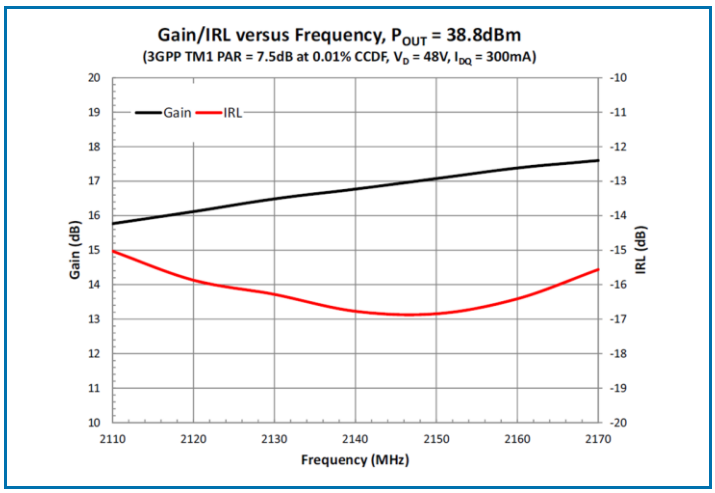
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Capacitance					
C_{RSS}		1.4		pF	V_G = -8V, V_D = 0V
C_{ISS}		15		pF	
C_{OSS}		11		pF	
RF Functional Test					**Test Conditions: V_{DSQ} = 48V, I_{DSQ} = 300mA, T = 25°C, Performance in a standard tuned test fixture**
V_{GSQ}	-1.5	-0.9	-0.3	V	V_{DSQ} = 48V, I_{DSQ} = 300mA
Gain	15.2	16.3		dB	IS95 (9 channel model, 9.8dB PAR at 0.01% CCDF), P_{OUT} = 39.5dBm, f = 2140MHz
Drain Efficiency	30	32.6		%	
Input Return Loss		-11.5	-8	dB	
Output PAR (CCDF at 0.01%)	4.7	6.1		d**B**	
RF Typical Performance					**Test Conditions: V_{DSQ} = 48V, I_{DSQ} = 300mA, T = 25°C, Performance in a standard tuned test fixture**
Gain		16.8		dB	3GPP (TM1, 7.5dB PAR at 0.01% CCDF), P_{OUT} = 38.8dBm, f = 2140MHz
Drain Efficiency		29.2		%	
Input Return Loss		-12		dB	
Adjacent Channel Power		-39.7		dBc	
Gain		15.3		dB	CW, f = 2140MHz
Output Power		45.2		dBm	
Drain Efficiency		58		%	

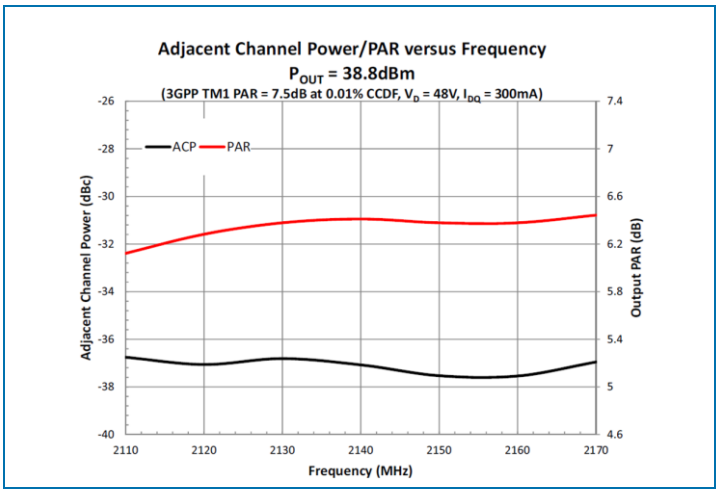
Typical Performance in Standard Fixed Tuned Test Fixture Optimized for Linearity (T = 25°C unless noted)



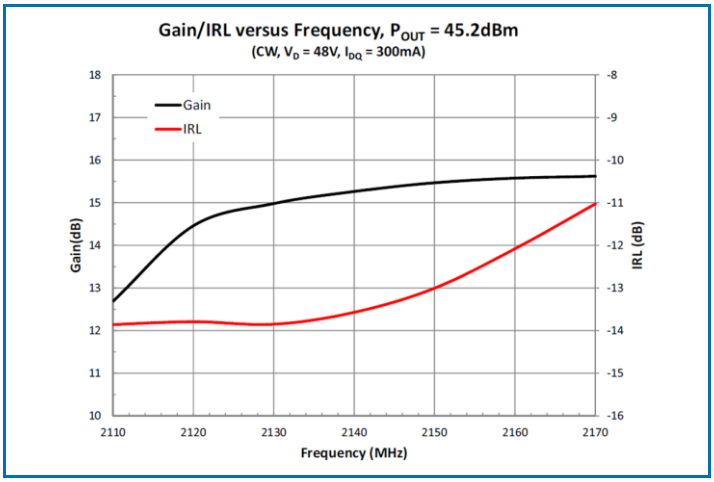


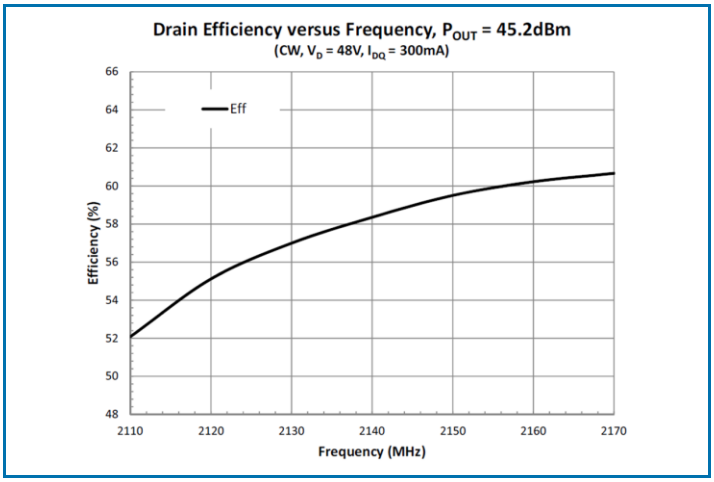


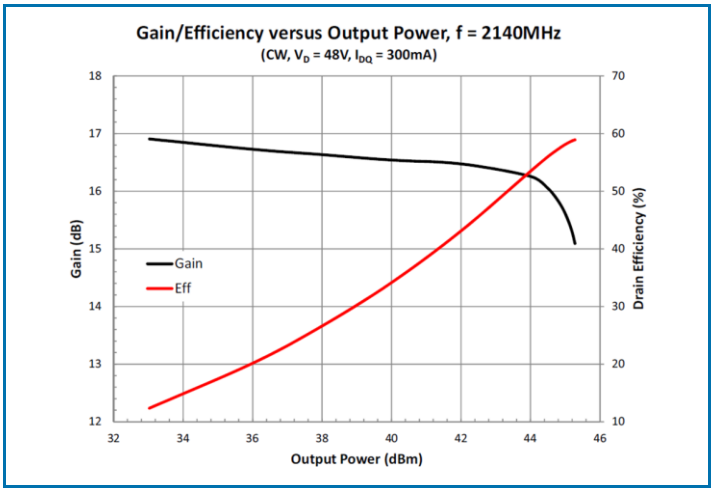


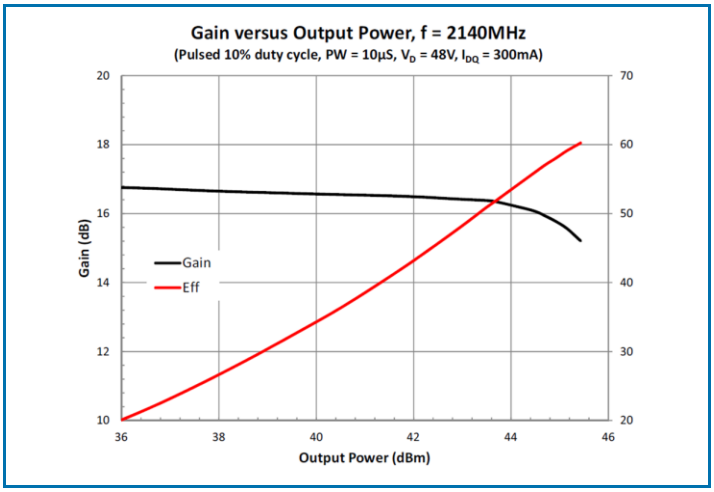


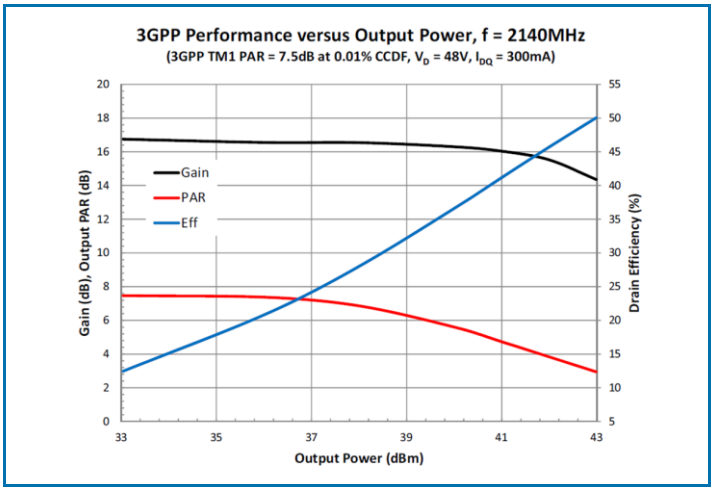
Typical Performance in Standard Fixed Tuned Test Fixture Optimized for Linearity (T = 25°C unless noted) (continued)

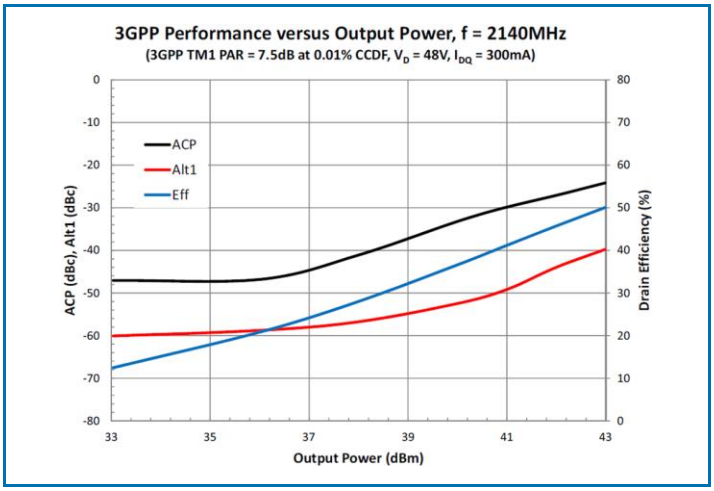




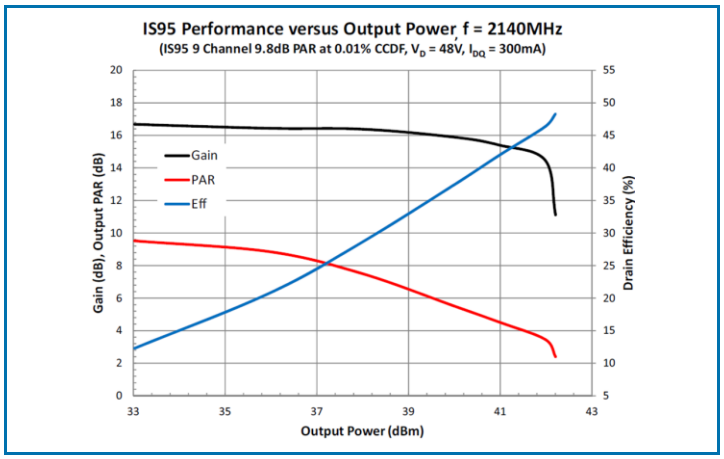


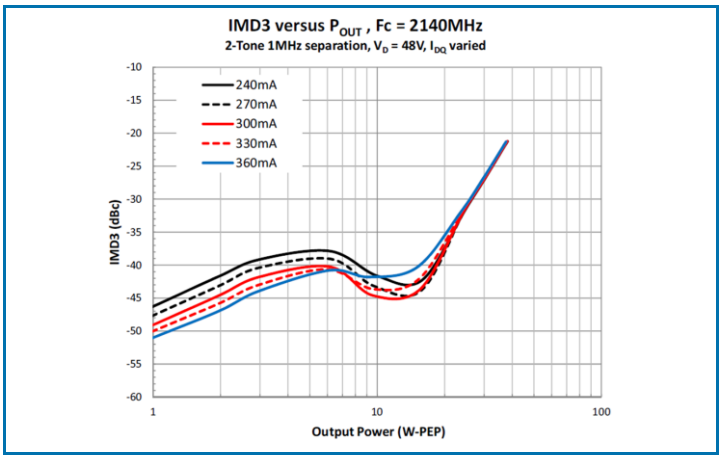


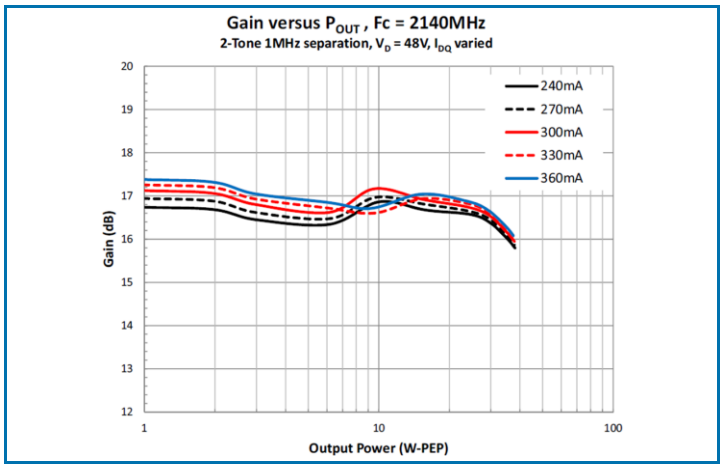


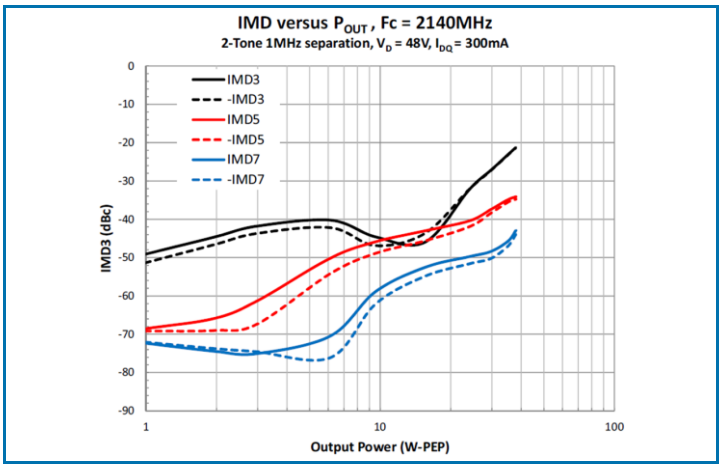


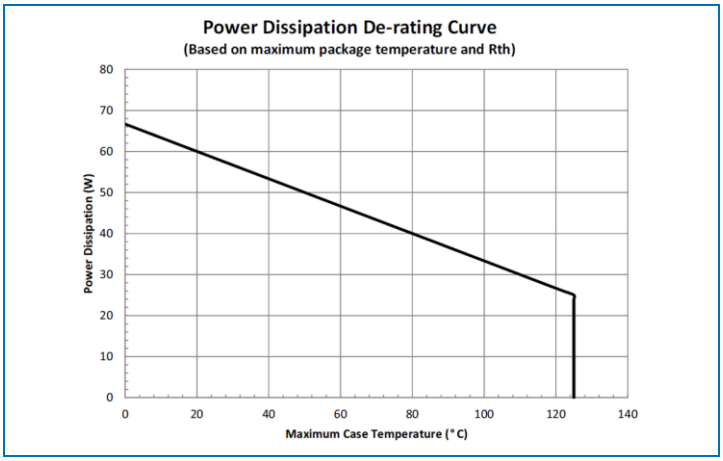
Typical Performance in Standard Fixed Tuned Test Fixture Optimized for Linearity (T = 25°C unless noted) (continued)



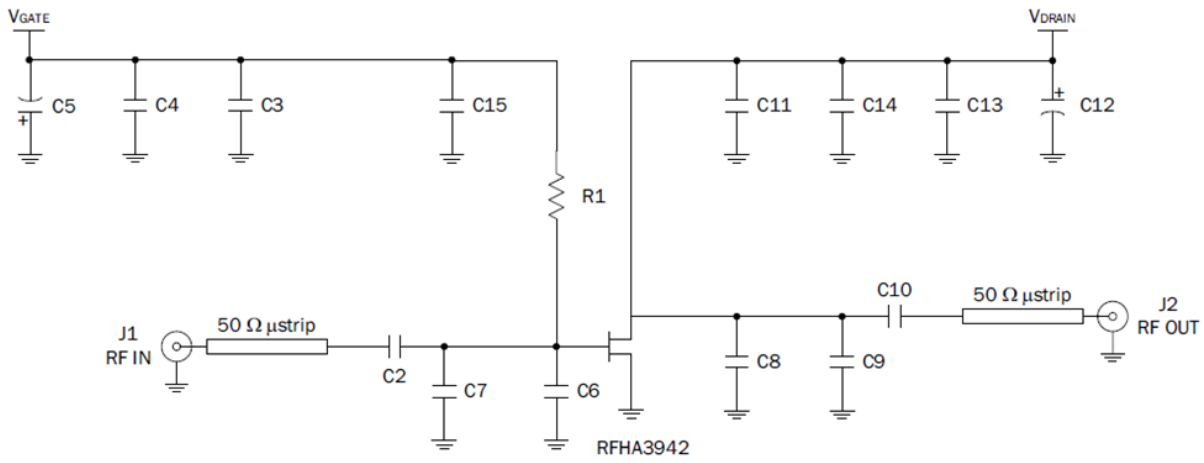








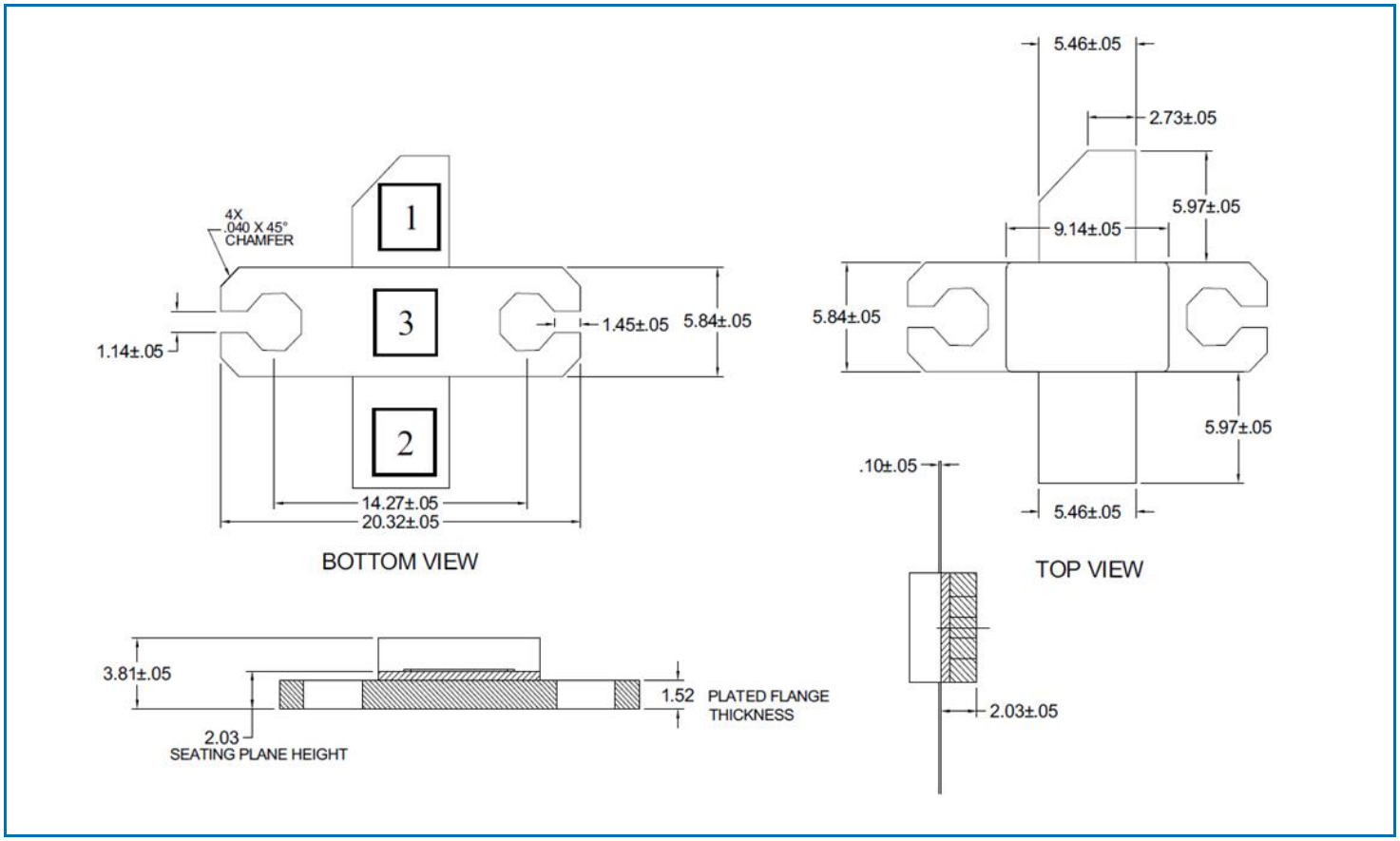
2.14GHz Evaluation Board Schematic



2.14GHz Evaluation Board Bill of Materials (BOM)

Item	Value	Manufacturer	Manufacturer's P/N
C2, C10, C11, C15	33pF	ATC	ATC800A330JT
C3, C14	0.1uF	Murata	GRM32NR72A104KA01L
C4, C13	4.7uF	Murata	GRM55ER72A475KA01L
C6	2.2pF	ATC	ATC800A2R2BT
C7	0.6pF	ATC	ATC800A0R6BT
C8	1.2pF	ATC	ATC800A1R2BT
C9	2.7pF	ATC	ATC800A2R7BT
C12	330µF	Panasonic	EEU-FC2A331
R1	10Ω	Panasonic	ERJ-8GEYJ100V
C1, C16, C17, C18, C19	Not used	-	-
PCB	RO4350, 0.030" thick dielectric	Rogers	-

Package Drawing



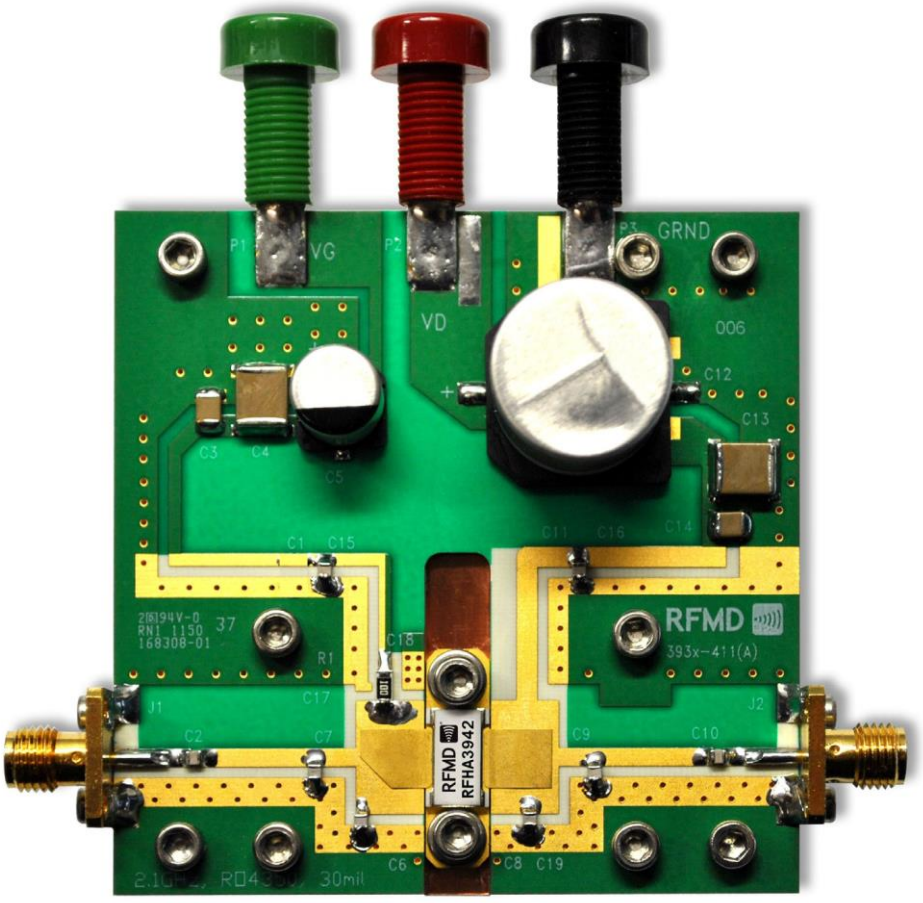
Pin Names and Descriptions

Pin	Name	Description
1	GATE	V_{GQ} RF Input
2	DRAIN	V_{DQ} RF Output
3	SOURCE	Ground Base

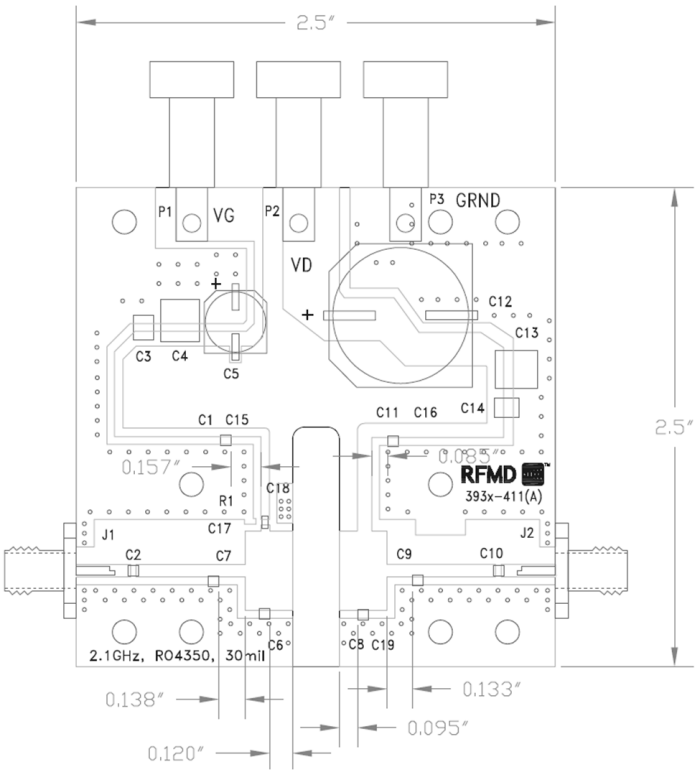
Bias Instruction for RFHA3942 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
Evaluation board requires additional external fan cooling.
Connect all supplies before powering evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -5V to VG.
4. Apply 48V to VD.
5. Increase V_G until drain current reaches 300mA or desired bias point.
6. Turn on the RF input.



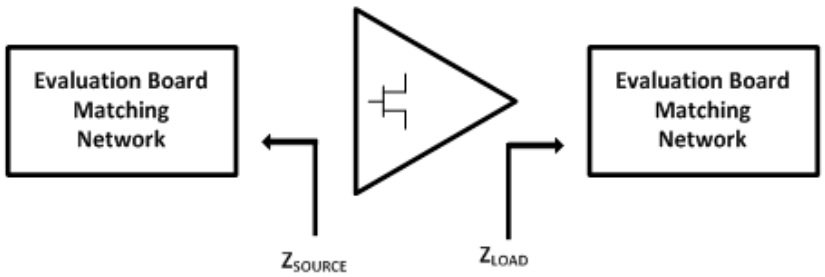
2.14GHz Evaluation Board Layout



Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
2110	3.3 - j0.5	7.8 + j6.5
2140	3.4 - j0.0	8 + j7.0
2170	3.5 + j0.7	8.2 + j7.7

NOTE: Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



Device Handling/Environmental Conditions

RFMD does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.