# Si53102-A1/A2/A3

# PCI-Express Gen 1, Gen 2, Gen 3, and Gen 4 1:2 Fan-out Clock Buffer

## Features

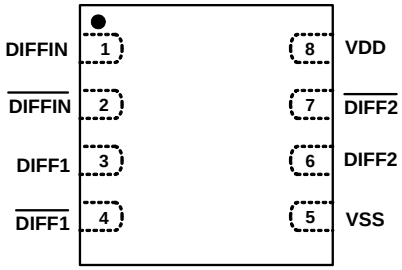
- PCI-Express Gen 1, Gen 2, Gen 3, and Gen 4 common clock compliant
- Two low-power PCIe clock outputs
- Supports Serial-ATA (SATA) at 100 MHz
- No termination resistors required for differential clocks
- 2.5 V or 3.3 V Power supply
- Spread Spectrum Tolerant
- Extended Temperature: –40 to 85 °C
- Small package 8-pin TDFN (1.4x1.6 mm)
- For PCIe Gen 1: Si53102-A1
- For PCIe Gen 2: Si53102-A2
- For PCIe Gen 3/4: Si53102-A3


**Ordering Information:**
See page 11

## Applications

- Network Attached Storage
- Multi-function Printer
- Wireless Access Point
- Server/Storage

**Pin Assignments**

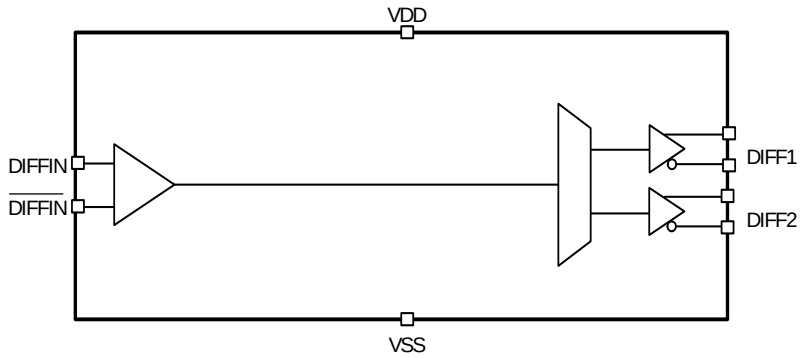



Patents pending

## Description

Si53102-A1/A2/A3 is a family of high-performance 1:2 PCIe fan output buffers. This low-additive-jitter clock buffer family is compliant to PCIe Gen 1, Gen 2, Gen 3, and Gen 4 specifications. The ultra-small footprint (1.4x1.6 mm) and industry-leading low power consumption make the Si53102-A1/A2/A3 the ideal clock solution for consumer and embedded applications. Measuring PCIe clock jitter is quick and easy with the Silicon Labs PCIe Clock Jitter Tool. Download it for free at www.silabs.com/pcie-learningcenter.

## Functional Block Diagram



# TABLE OF CONTENTS

## Table of Contents

Page

# 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage (3.3 V Supply) | $V_{DD}$ | 3.3 V ± 10% | 2.97 | 3.3 | 3.63 | V |
| Supply Voltage (2.5 V Supply) | $V_{DD}$ | 2.5 V ± 10% | 2.25 | 2.5 | 2.75 | V |

**Table 2. DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage (VDD = 3.3 V) | $V_{DD}$ | 3.3 V ± 10% | 2.97 | 3.30 | 3.63 | V |
| Operating Voltage (VDD = 2.5 V) | $V_{DD}$ | 2.5 V ± 10% | 2.25 | 2.5 | 2.75 | V |
| Operating Supply Current | $I_{DD}$ | Full Active | — | — | 12 | mA |
| Input Pin Capacitance | $C_{IN}$ | Input Pin Capacitance | — | 3 | 5 | pF |
| Output Pin Capacitance | $C_{OUT}$ | Output Pin Capacitance | — | — | 5 | pF |

## Table 3. AC Electrical Specifications

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DIFFIN at 0.7 V** | | | | | | |
| Input frequency | Fin | | 10 | 100 | 175 | MHz |
| DIFFIN and $\overline{\text{DIFFIN}}$ Rising/Falling Slew Rate | $T_R$ / $T_F$ | Single ended measurement: $V_{OL}$ = 0.175 to $V_{OH}$ = 0.525 V (Averaged) | 0.6 | — | 4 | V/ns |
| Differential Input High Voltage | $V_{IH}$ | | 150 | — | — | mV |
| Differential Input Low Voltage | $V_{IL}$ | | — | — | –150 | mV |
| Crossing Point Voltage at 0.7 V Swing | $V_{OX}$ | Single-ended measurement | 250 | — | 550 | mV |
| Vcross Variation Over All edges | $\Delta V_{OX}$ | Single-ended measurement | — | — | 140 | mV |
| Differential Ringback Voltage | $V_{RB}$ | | –100 | — | 100 | mV |
| Time before Ringback Allowed | $T_{STABLE}$ | | 500 | — | — | ps |
| Absolute Maximum Input Voltage | $V_{MAX}$ | | | — | 1.15 | V |
| Absolute Minimum Input Voltage | $V_{MIN}$ | | –0.3 | — | — | V |
| DIFFIN and $\overline{\text{DIFFIN}}$ Duty Cycle | $T_{DC}$ | Measured at crossing point $V_{OX}$ | 45 | — | 55 | % |
| Rise/Fall Matching | $T_{RFM}$ | Determined as a fraction of $2 \times (T_R - T_F)/(T_R + T_F)$ | — | — | 20 | % |
| **DIFF Clocks** | | | | | | |
| Duty Cycle | $T_{DC}$ | Measured at crossing point $V_{OX}$ | 45 | — | 55 | % |
| Output Skew | $T_{SKEW}$ | Measured at 0 V differential | — | — | 100 | ps |
| Frequency Accuracy | $F_{ACC}$ | All output clocks | — | — | 100 | ppm |
| Slew Rate | $t_{r/f2}$ | Measured differentially from ±150 mV | 0.6 | — | 4.0 | V/ns |
| PCIe Gen 1 Pk-Pk Additive Jitter | Pk-$Pk_{GEN1}$ | PCIe Gen 1 Si53102-A1 | — | — | 10 | ps |
| PCIe Gen 2 Additive Phase Jitter | $RMS_{GEN2}$ | 10 kHz < F < 1.5 MHz, Si53102-A2 | — | — | 0.50 | ps |
| PCIe Gen 2 Additive Phase Jitter | $RMS_{GEN2}$ | 1.5 MHz < F < Nyquist, Si53102-A2 | — | — | 0.50 | ps |
| PCIe Gen 3 Additive Phase Jitter | $RMS_{GEN3}$ | Includes PLL BW 2–4 MHz, CDR = 10 MHz, Si53102-A3 | — | — | 0.20 | ps |
| PCIe Gen 4 Additive Phase Jitter | $RMS_{GEN4}$ | PCIe Gen 4 | — | — | 0.20 | ps |
| Crossing Point Voltage at 0.7 V Swing | $V_{OX}$ | | 300 | — | 550 | mV |
| **Enable/Disable and Setup** | | | | | | |
| Clock Stabilization from Powerup | $T_{STABLE}$ | Power up to first output | — | — | 3.0 | ms |

**Notes:**
1. Visit www.pcisig.com for complete PCIe specifications.
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

### Table 4. Thermal Conditions

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature, Storage | $T_S$ | Non-functional | –65 | | 150 | °C |
| Temperature, Operating Ambient | $T_A$ | Functional | –40 | | 85 | °C |
| Temperature, Junction | $T_J$ | Functional | — | | 150 | °C |
| Dissipation, Junction to Case | $\theta_{JC}$ | JEDEC (JESD 51) | — | | 38.3 | °C/W |
| Dissipation, Junction to Ambient | $\theta_{JA}$ | JEDEC (JESD 51) | — | | 90.4 | °C/W |

### Table 5. Absolute Maximum Conditions

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Main Supply Voltage | $V_{DD\_3.3V}$ | | — | | 4.6 | V |
| Input Voltage | $V_{IN}$ | Relative to $V_{SS}$ | –0.5 | | 4.6 | $V_{DC}$ |
| ESD Protection (Human Body Model) | $ESD_{HBM}$ | JEDEC (JESD 22-A114) | 2000 | | — | V |
| Flammability Rating | UL-94 | UL (Class) | V–0 | | | |

**Note:** While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is NOT required.

## 2. Test and Measurement Setup

Figures 1 through 3 show the test load configuration for the differential clock signals.

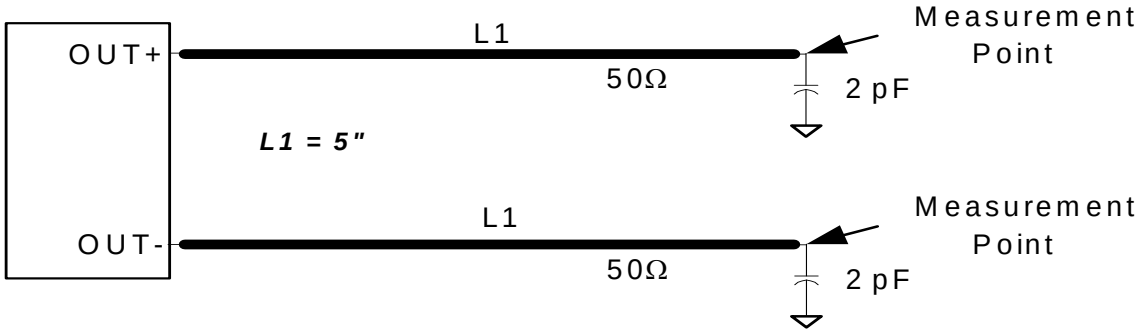



**Figure 1. 0.7 V Differential Load Configuration**

The outputs from this device can also support LVDS, LVPECL, or CML differential signaling levels using alternative termination. For recommendations on how to achieve this, see “AN781: Alternative Output Termination for Si5213x, Si5214x, Si5121x, and Si5315x PCIe Clock Generator and Buffer Families” at www.silabs.com.

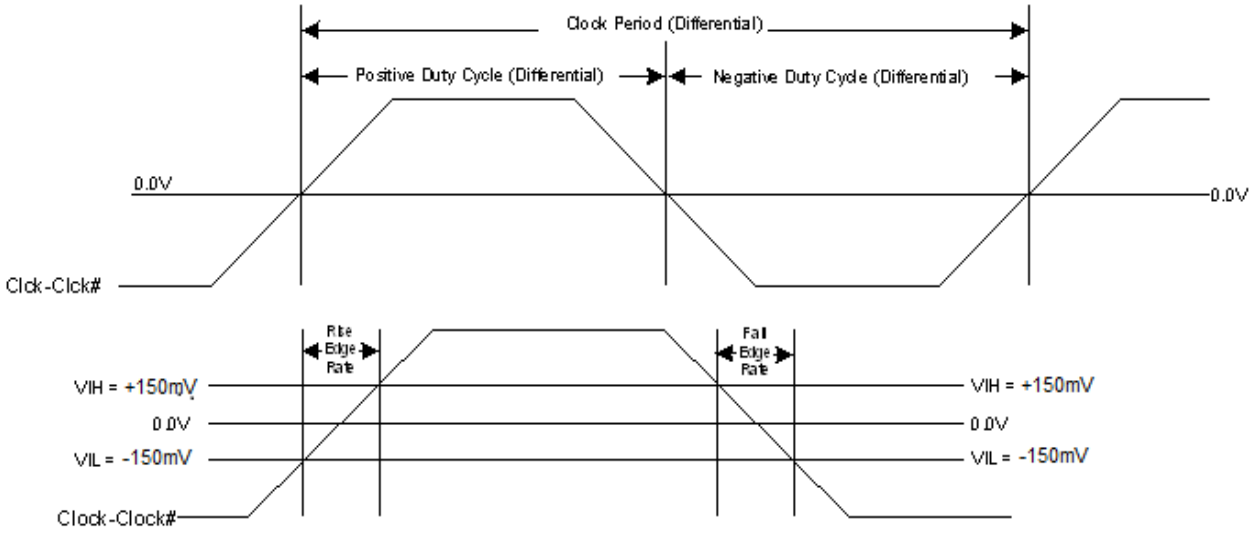



**Figure 2. Differential Measurement for Differential Output Signals (AC Parameters Measurement)**

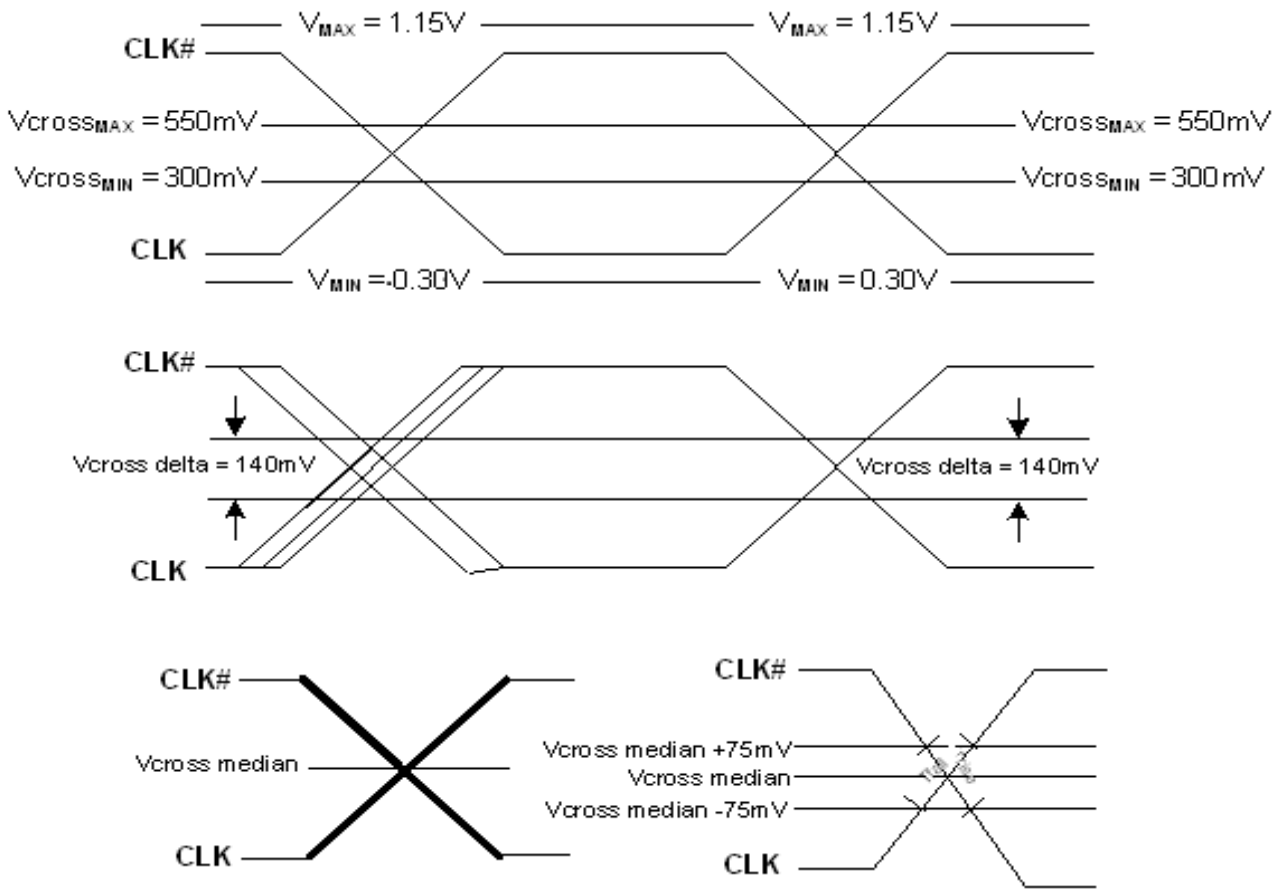
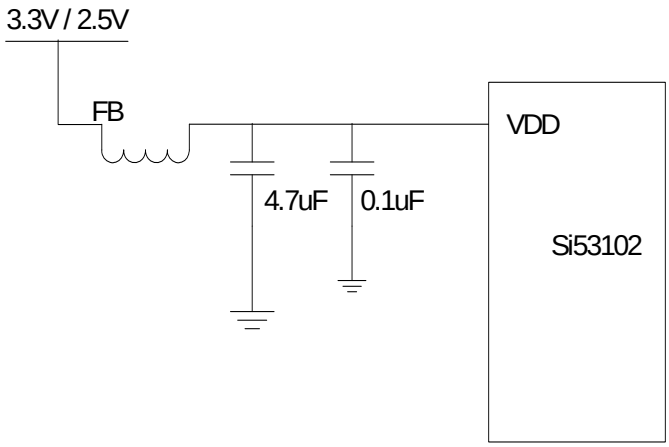



**Figure 3. Single-Ended Measurement for Differential Output Signals (AC Parameters Measurement)**

## 3. Recommended Design Guideline




**Note:** FB Specifications:
DC resistance 0.1–0.3 Ω
Impedance at 100 MHz ≥ 1000 Ω

**Figure 4. Recommended Application Schematic**

## 4. Pin Descriptions

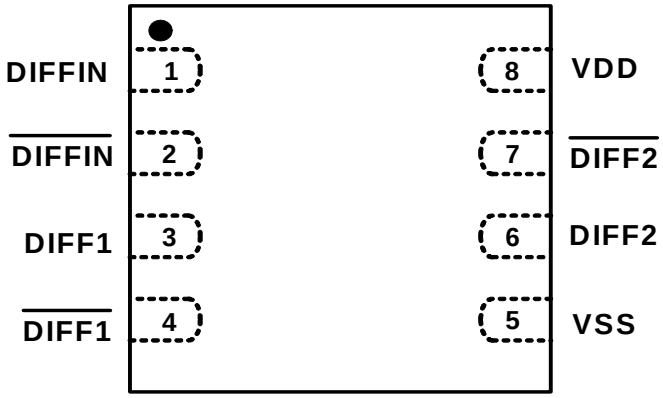



**Figure 5. 8-Pin TDFN**

**Table 6. Si53102-Ax-GM 8-Pin TDFN Descriptions**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | DIFFIN | O, DIF | 0.7 V, 100 MHz differentials clock input |
| 2 | $\overline{\text{DIFFIN}}$ | O, DIF | 0.7 V, 100 MHz differentials clock input |
| 3 | DIFF1 | O, DIF | 0.7 V, 100 MHz differential clock output |
| 4 | $\overline{\text{DIFF1}}$ | O, DIF | 0.7 V, 100 MHz differential clock output |
| 5 | GND | GND | Ground |
| 6 | DIFF2 | O, DIF | 0.7 V, 100 MHz differential clock output |
| 7 | $\overline{\text{DIFF2}}$ | O, DIF | 0.7 V, 100 MHz differential clock output |
| 8 | VDD | PWR | 2.5 V or 3.3 V Power supply |

## 5. Ordering Guide

| Part Number | Package Type | Temperature |
|---|---|---|
| **Si53102-A1-GM** | 8-pin TDFN | Extended, –40 to 85 °C |
| **Si53102-A1-GMR** | 8-pin TDFN—Tape and Reel | Extended, –40 to 85 °C |
| **Si53102-A2-GM** | 8-pin TDFN | Extended, –40 to 85 °C |
| **Si53102-A2-GMR** | 8-pin TDFN—Tape and Reel | Extended, –40 to 85 °C |
| **Si53102-A3-GM** | 8-pin TDFN | Extended, –40 to 85 °C |
| **Si53102-A3-GMR** | 8-pin TDFN—Tape and Reel | Extended, –40 to 85 °C |

## 6. Package Outlines

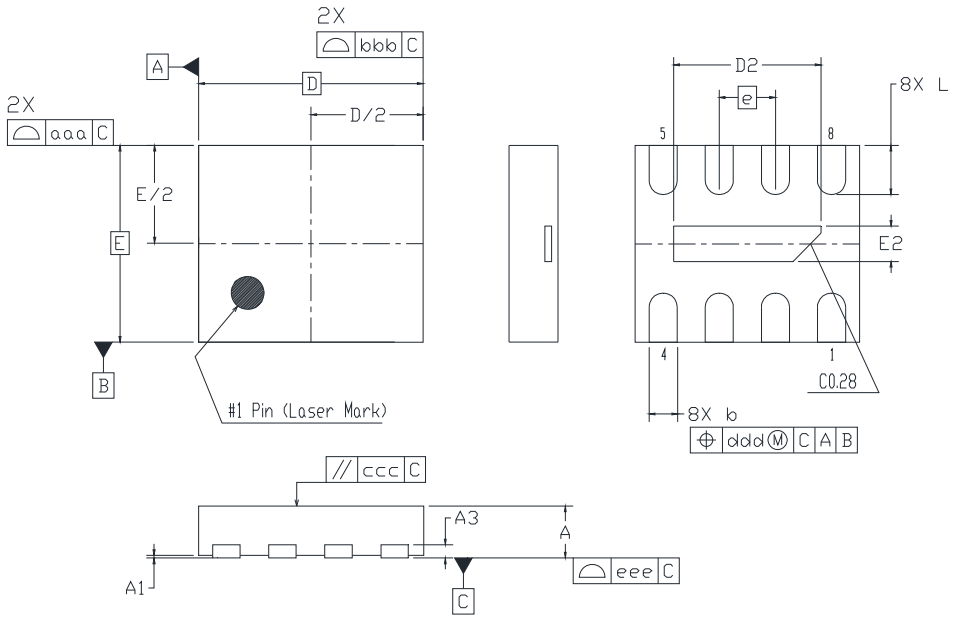



**Figure 6. 8-Pin TDFN Package Drawing**

**Table 7. Package Diagram Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 1.60 BSC | | |
| D2 | 1.00 | 1.05 | 1.10 |
| e | 0.40 BSC | | |
| E | 1.40 BSC | | |
| E2 | 0.20 | 0.25 | 0.30 |
| L | 0.30 | 0.35 | 0.40 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.07 | | |
| eee | 0.08 | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. PCB Land Pattern

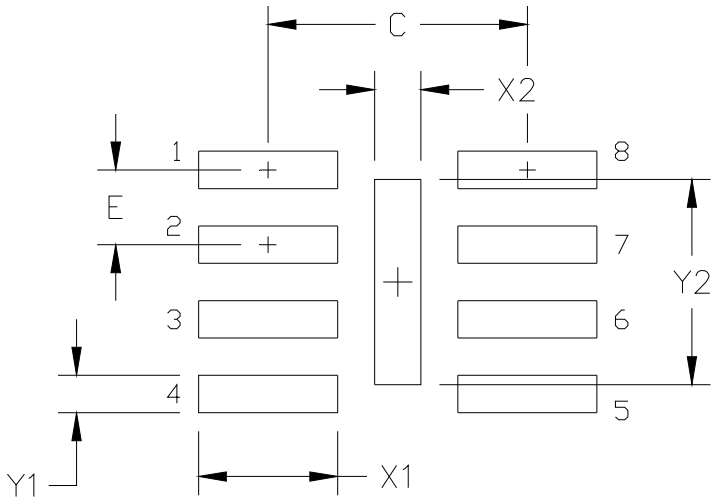



**Figure 7. Si53102 8-Pin TDFN Land Pattern**

**Table 8. Si53102 8-Pin Land Pattern Dimensions**

| Dimension | mm |
|---|---|
| C | 1.40 |
| E | 0.40 |
| X1 | 0.75 |
| Y1 | 0.20 |
| X2 | 0.25 |
| Y2 | 1.10 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

**Card Assembly**

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# Document Change List

## Revision 0.4 to Revision 1.0

- Updated Table 3 on page 5.
  - Updated input frequency min and max specs.
- Updated "2. Test and Measurement Setup" on page 7.
  - Added text and reference to AN781.

## Revision 1.0 to Revision 1.1

- Moved “3. Recommended Design Guideline” to page 9.
- Corrected Figure 5 title on page 10.
- Corrected Table 6 title on page 10.
- Corrected Figure 6 title on page 12.
- Added "7. PCB Land Pattern" on page 13.

## Revision 1.1 to Revision 1.2

- Updated Features on page 1.
- Updated Description on page 1.
- Updated specs in Table 3, “AC Electrical Specifications,” on page 5.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