



# STS9D8NH3LL

Dual N-channel 30 V - 0.012  $\Omega$  - 9 A - SO-8  
low on-resistance STripFET™ Power MOSFET

## Features

Type		V <sub>DSS</sub>	R <sub>DS(on)</sub>	Qg	I <sub>D</sub>
STS9D8NH3LL	Q <sub>1</sub>	30V	< 0.022 $\Omega$	7nC	8A
	Q <sub>2</sub>	30V	< 0.015 $\Omega$	8nC	9A

- Optimal R<sub>DS(on)</sub> x Qg trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced

## Application

- Switching applications

## Description

This device uses the latest advanced design rules of ST's STrip based technology. The Q1 and Q2 transistors, show respectively, the best gate charge and on-resistance for minimizing the switching and conduction losses. This application specific Power MOSFET has been designed to replace two SO-8 packages in DC-DC converters.

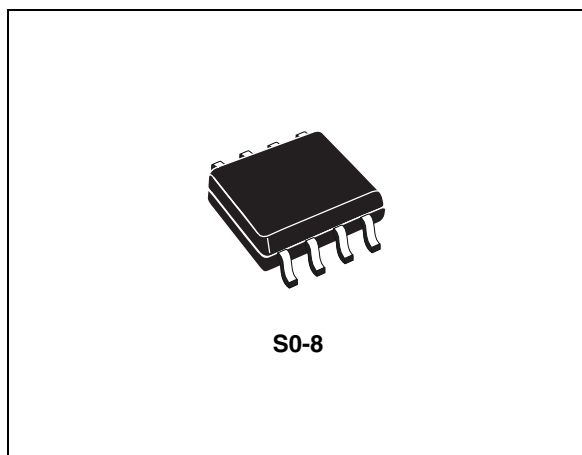


Figure 1. Internal schematic diagram

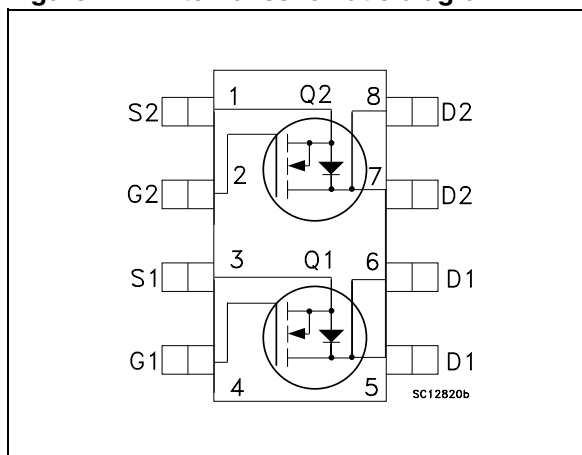


Table 1. Device summary

Order code	Marking	Package	Packaging
STS9D8NH3LL	9D8H3LL-	SO-8	Tape & reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	5
<b>3</b>	<b>Test circuit</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>11</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Type	Value	Unit
$V_{DS}$	Drain-source voltage ( $v_{GS} = 0$ )	Q <sub>1</sub>	30	V
		Q <sub>2</sub>	30	V
$V_{GS}$	Gate- source voltage	Q <sub>1</sub>	±16	V
		Q <sub>2</sub>	±16	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	Q <sub>1</sub>	8	A
		Q <sub>2</sub>	9	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	Q <sub>1</sub>	5	A
		Q <sub>2</sub>	6.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	Q <sub>1</sub>	32	A
		Q <sub>2</sub>	36	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	Q <sub>1</sub>	2	W
		Q <sub>2</sub>	2	W
$E_{AS}^{(2)}$	Single pulse avalanche energy		150	mJ

1. Pulse width limited by safe operating area

2. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 7.5\text{ A}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-a}^{(1)}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
$T_J$	Thermal operating junction-ambient	150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu.,  $t \leq 10\text{ s}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	Q <sub>1</sub>	30			V
			Q <sub>2</sub>	30			V
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$	Q <sub>1</sub>			1	$\mu A$
			Q <sub>2</sub>			1	$\mu A$
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ @ 125°C	Q <sub>1</sub>			10	$\mu A$
			Q <sub>2</sub>			10	$\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 16 V$	Q <sub>1</sub>			$\pm 100$	nA
			Q <sub>2</sub>			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS},$ $I_D = 250 \mu A$	Q <sub>1</sub>	1			V
			Q <sub>2</sub>	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 4 A$ $V_{GS} = 10 V, I_D = 4.5 A$	Q <sub>1</sub>		0.018	0.022	$\Omega$
			Q <sub>2</sub>		0.012	0.015	$\Omega$
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5 V, I_D = 4 A$ $V_{GS} = 4.5 V, I_D = 4.5 A$	Q <sub>1</sub>		0.020	0.025	$\Omega$
			Q <sub>2</sub>		0.014	0.0175	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance		Q <sub>1</sub>		857		pF
			Q <sub>2</sub>		1070		pF
$C_{oss}$	Output capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$	Q <sub>1</sub>		147		pF
			Q <sub>2</sub>		290		pF
$C_{rss}$	Reverse transfer capacitance		Q <sub>1</sub>		20		pF
			Q <sub>2</sub>		34		pF
$Q_g$	Total gate charge		Q <sub>1</sub>		7	10	nC
			Q <sub>2</sub>		8	11	nC
$Q_{gs}$	Gate-source charge	$V_{DD} = 15 V, I_D = 8 A,$ $V_{GS} = 4.5 V$ (see Figure 25)	Q <sub>1</sub>		2.5		nC
			Q <sub>2</sub>		2		nC
$Q_{gd}$	Gate-drain charge		Q <sub>1</sub>		2.3		nC
			Q <sub>2</sub>		2.8		nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=4\text{ A}$ , $R_G=4.7\ \Omega$ ,	$Q_1$		12		ns
$t_r$	Rise time	$V_{GS}=4.5\text{ V}$ (see Figure 27)	$Q_2$		8.2		ns
			$Q_1$		14.5		ns
			$Q_2$		6		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=15\text{ V}$ , $I_D=4\text{ A}$ , $R_G=4.7\ \Omega$ ,	$Q_1$		23		ns
$t_f$	Fall time	$V_{GS}=4.5\text{ V}$ (see Figure 27)	$Q_2$		27.8		ns
			$Q_1$		8		ns
			$Q_2$		3.6		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Type	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current	$V_{DD}=15\text{ V}$ , $I_D=4\text{ A}$ $R_G=4.7\ \Omega$ $V_{GS}=4.5\text{ V}$	$Q_1$			8	A
			$Q_2$			9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)	$V_{DD}=15\text{ V}$ , $I_D=4\text{ A}$ $R_G=4.7\ \Omega$ $V_{GS}=4.5\text{ V}$	$Q_1$			32	A
			$Q_2$			36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=8\text{ A}$ , $V_{GS}=0$	$Q_1$			1.5	V
			$Q_2$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=8\text{ A}$ , $V_{DD}=15\text{ V}$	$Q_1$		15		ns
$Q_{rr}$	Reverse recovery charge	$di/dt=100\text{ A}/\mu\text{s}$ , $T_j=150^\circ\text{C}$	$Q_2$		22.8		ns
		(see Figure 26)	$Q_1$		5.7		nC
$I_{RRM}$	Reverse recovery current		$Q_2$		14.9		nC
			$Q_1$		0.76		A
			$Q_2$		1.3		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for Q1

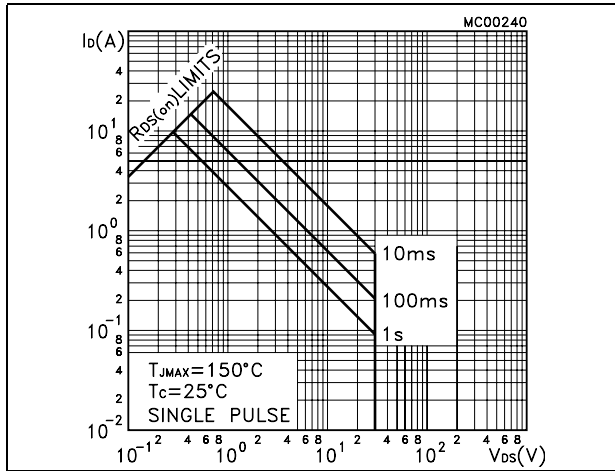


Figure 3. Safe operating area for Q2

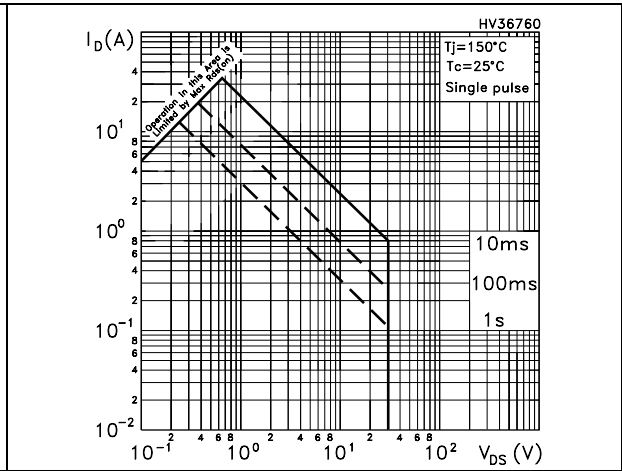


Figure 4. Thermal impedance for Q1

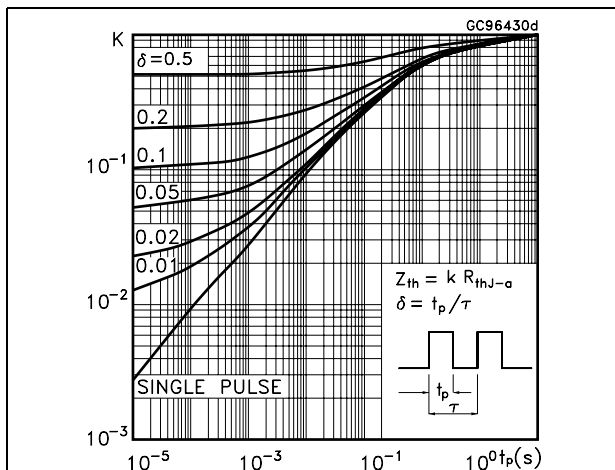


Figure 5. Thermal impedance for Q2

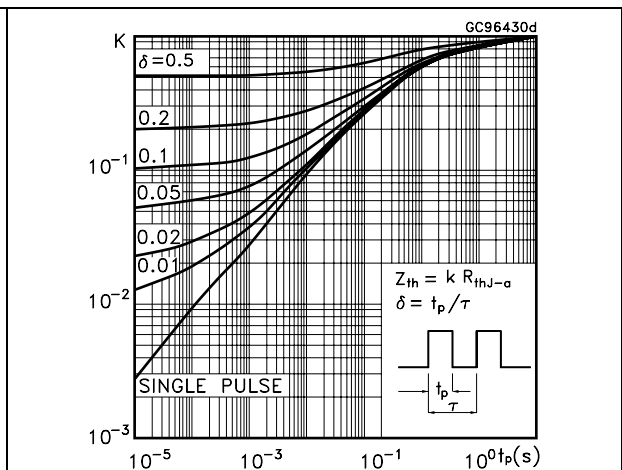


Figure 6. Output characteristics for Q1

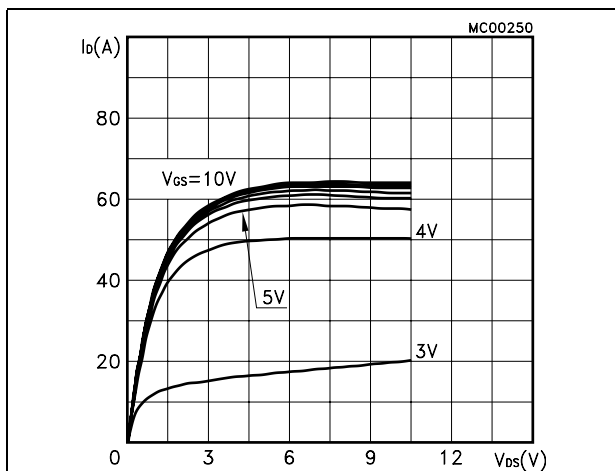


Figure 7. Output characteristics for Q2

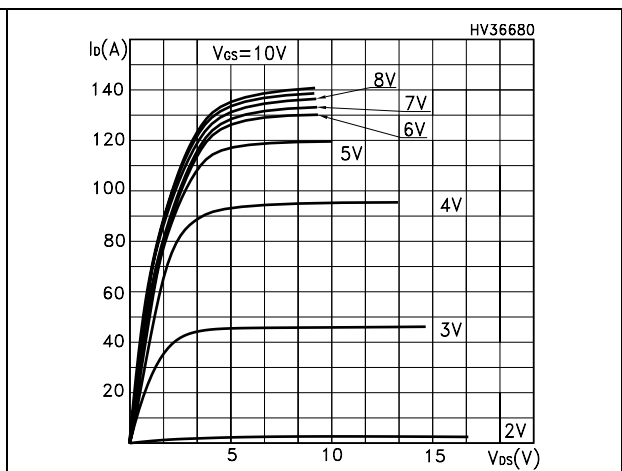


Figure 8. Transfer characteristics for Q1

Figure 9. Transfer characteristics for Q2

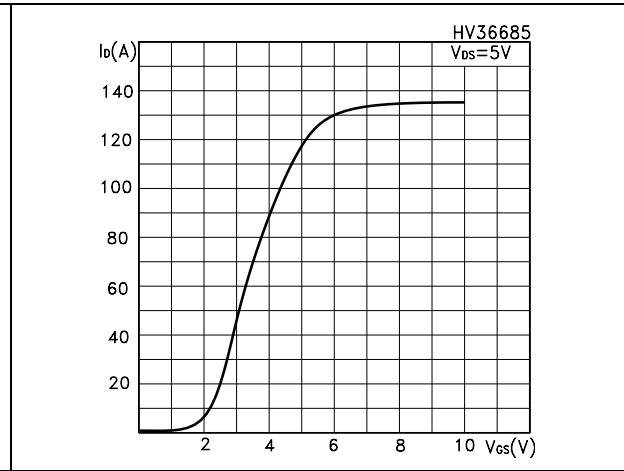
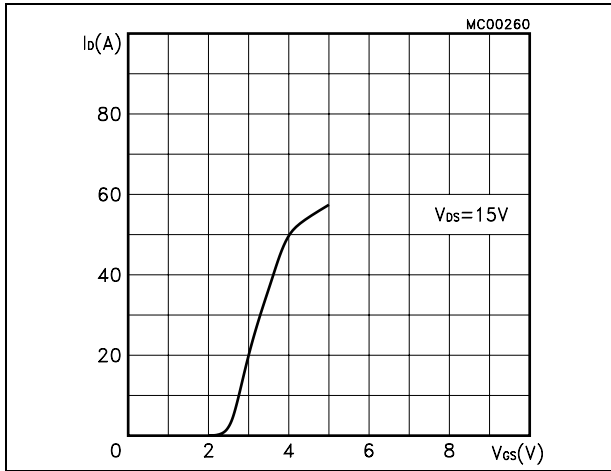


Figure 10. Static drain-source on resistance for Q1

Figure 11. Static drain-source on resistance for Q2

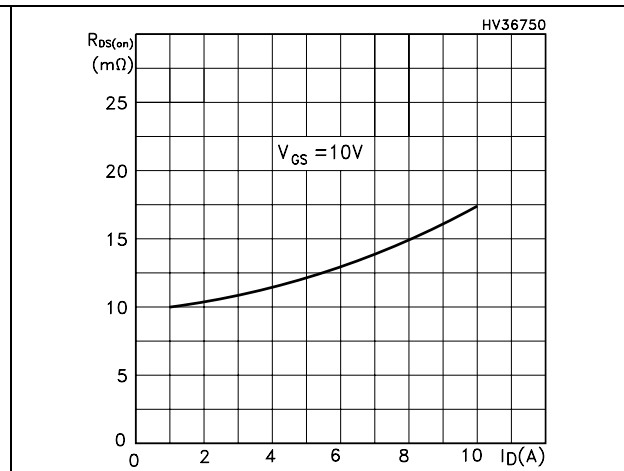
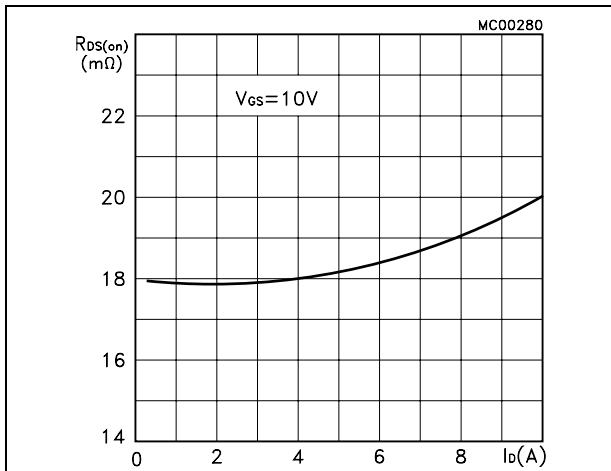


Figure 12. Normalized BV<sub>DSS</sub> vs temperature for Q1

Figure 13. Normalized BV<sub>DSS</sub> vs temperature for Q2

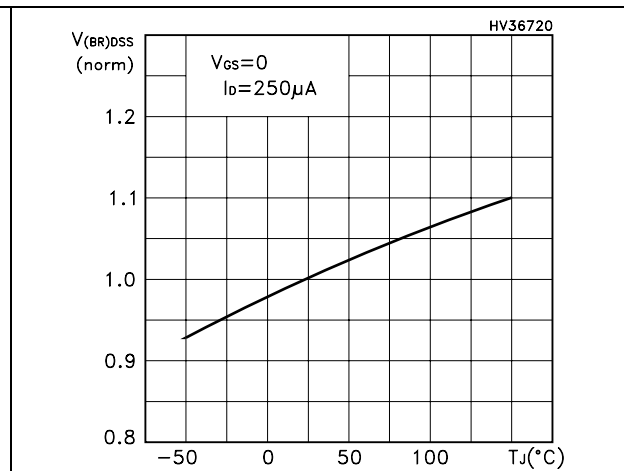
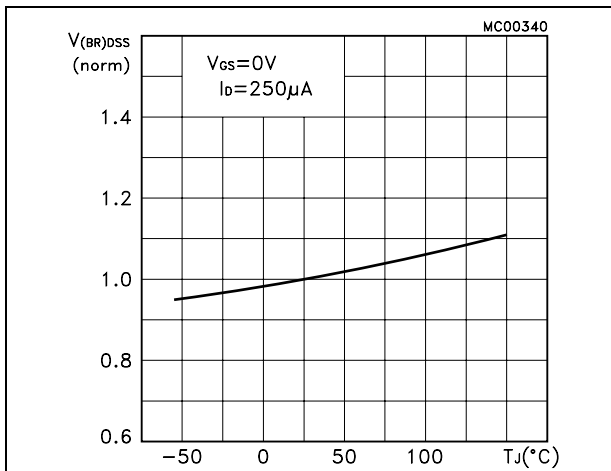


Figure 14. Gate charge vs gate-source voltage for Q1      Figure 15. Gate charge vs gate-source voltage for Q2

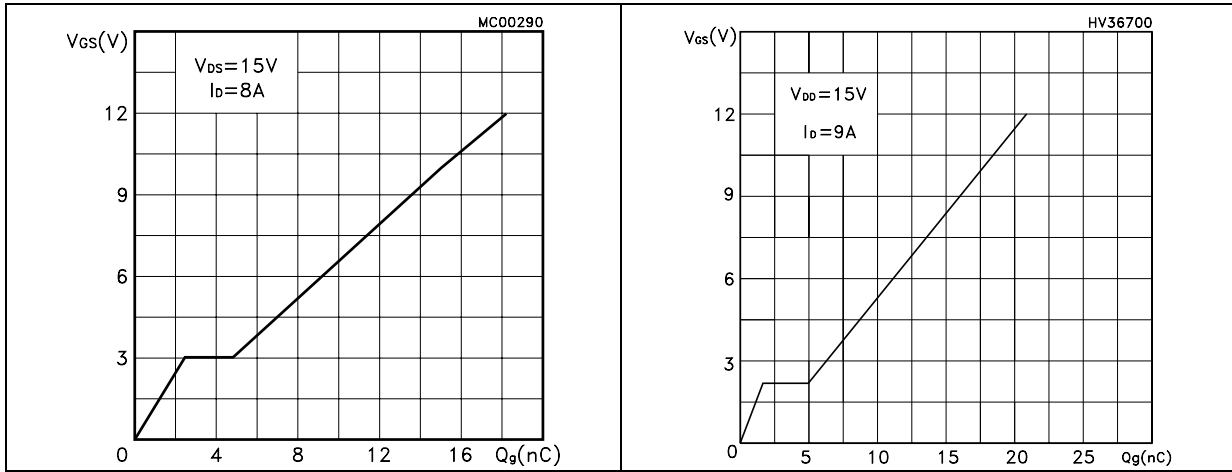


Figure 16. Capacitance variations for Q1

Figure 17. Capacitance variations for Q2

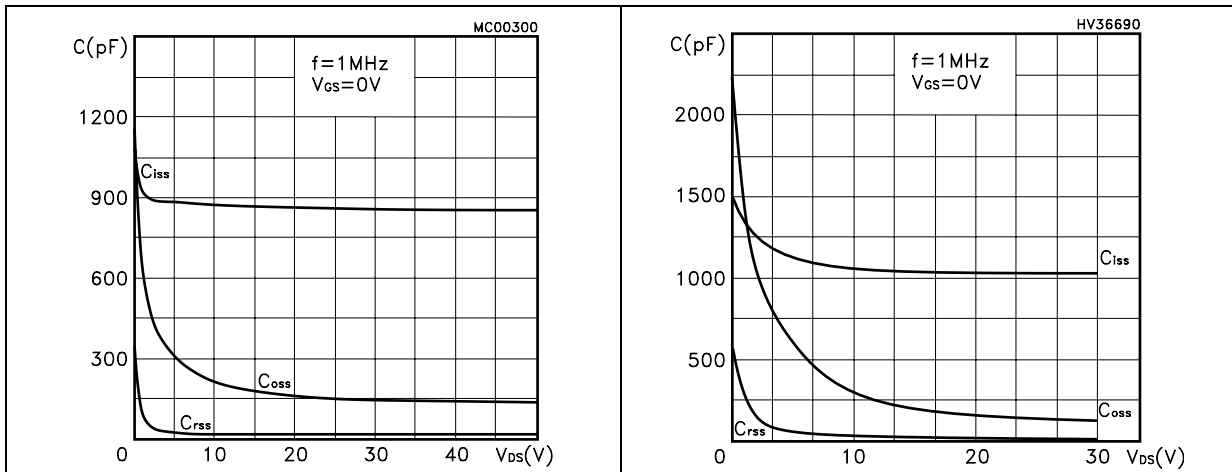
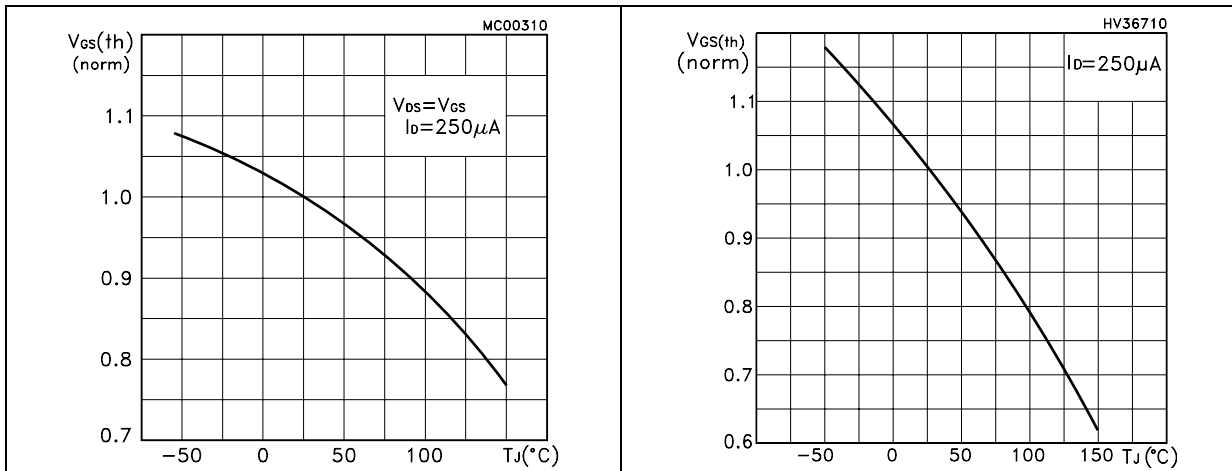


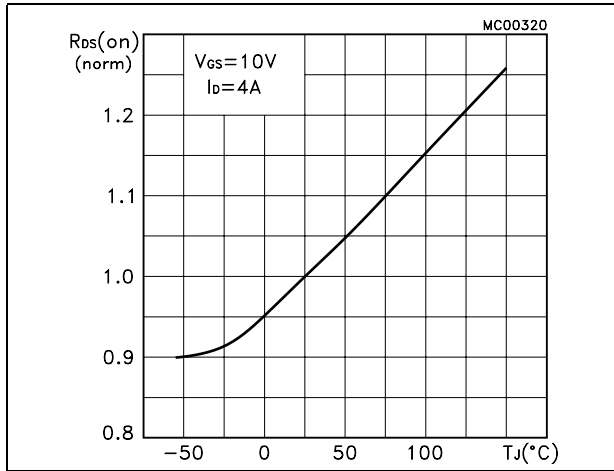
Figure 18. Normalized gate threshold voltage vs temperature for Q1

Figure 19. Normalized gate threshold voltage vs temperature for Q2

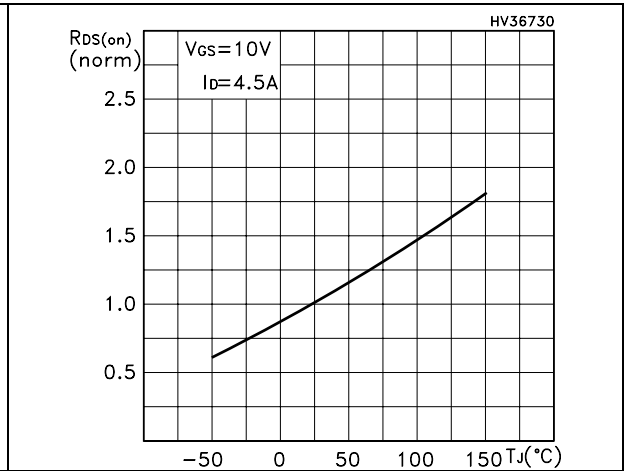




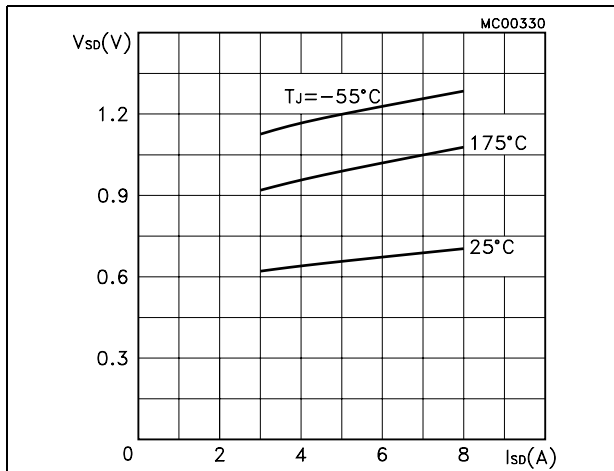
**Figure 20. Normalized on resistance vs temperature for Q1**



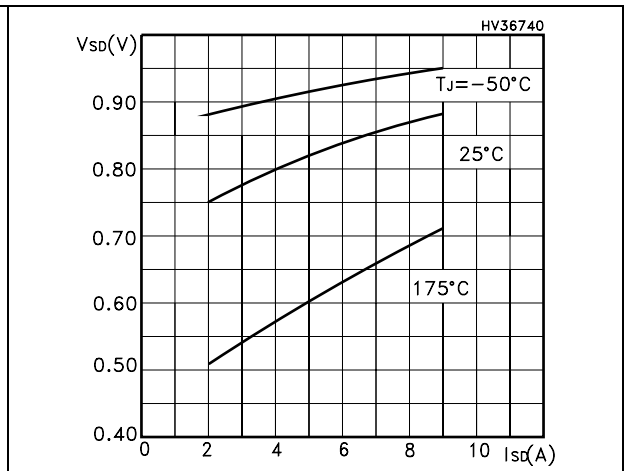
**Figure 21. Normalized on resistance vs temperature for Q2**



**Figure 22. Source-drain diode forward characteristics for Q1**



**Figure 23. Source-drain diode forward characteristics for Q2**



### 3 Test circuit

Figure 24. Switching times test circuit for resistive load

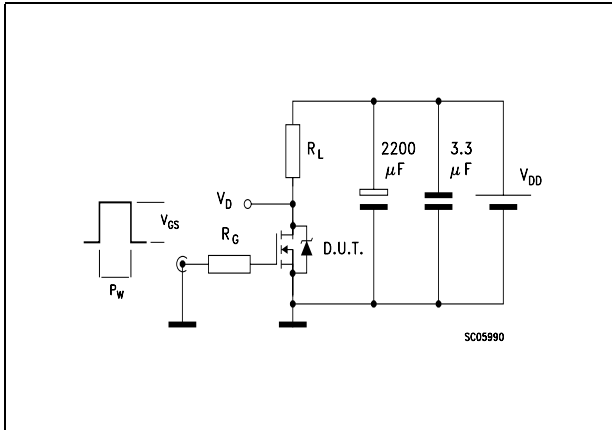


Figure 25. Gate charge test circuit

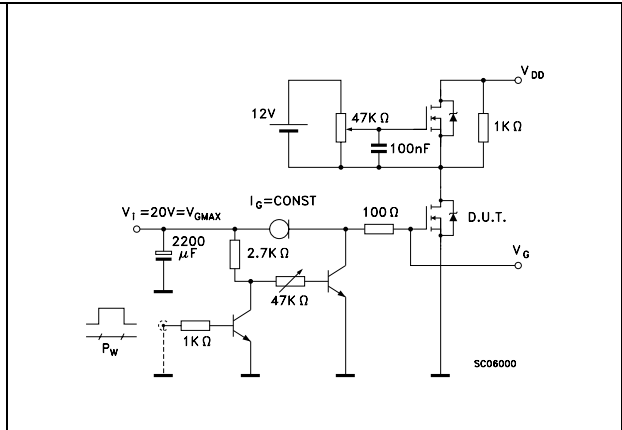


Figure 26. Test circuit for inductive load switching and diode recovery times

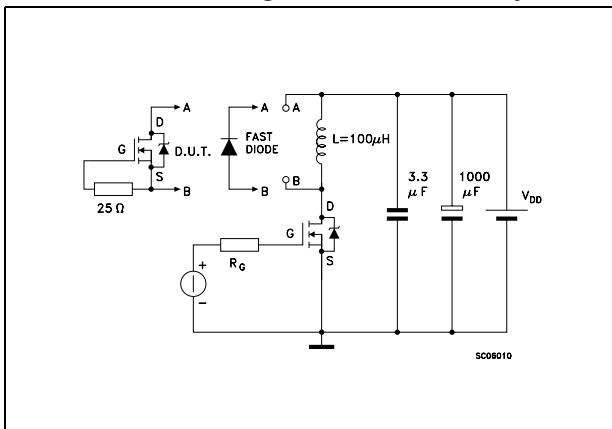


Figure 27. Unclamped Inductive load test circuit

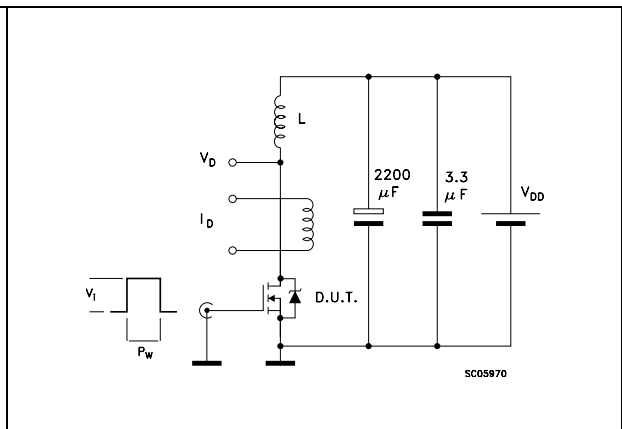


Figure 28. Unclamped inductive waveform

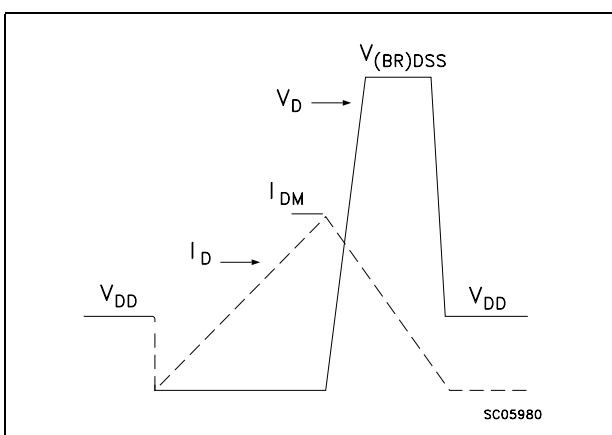
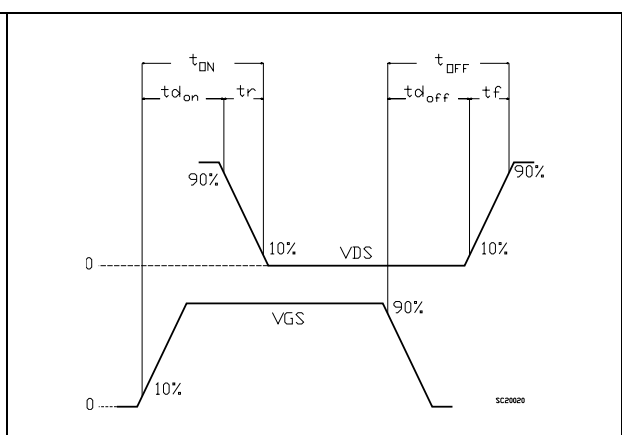


Figure 29. Switching time waveform

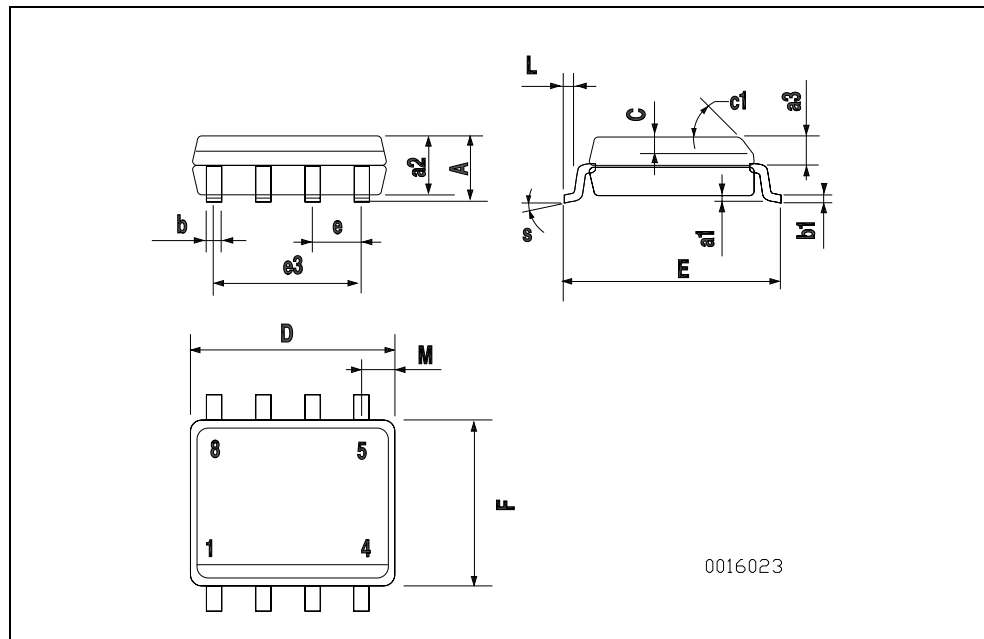


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
05-Jan-2007	1	First release
06-Mar-2007	2	Some value changed on <a href="#">Table 4</a> ( $R_{DS(on)}$ for Q2)
10-Dec-2007	3	Added $E_{AS}$ value on <a href="#">Table 2: Absolute maximum ratings</a>

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