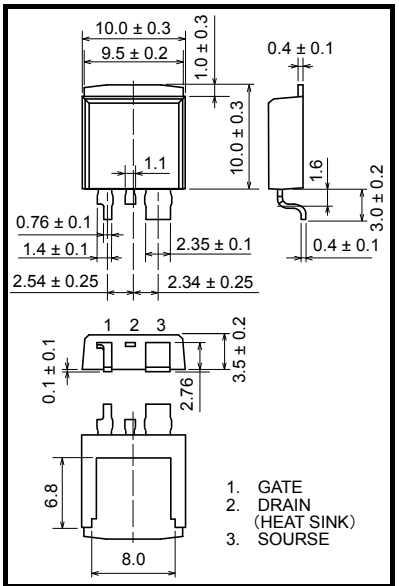
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIV)

TK100F04K3

Swiching Regulator, DC-DC Converter Applications
Motor Drive Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 2.5 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 174 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 40 V)
- Enhancement-model: V_{th} = 3.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-10W1A

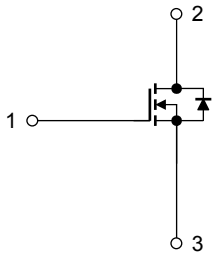
Weight: 1.07 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	40	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	40	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	100	A
	Pulse (Note 1)	I_{DP}	300	
Drain power dissipation (Tc = 25°C)		P_D	180	W
Single pulse avalanche energy (Note 2)		E_{AS}	125	mJ
Avalanche current		I_{AR}	100	A
Repetitive avalanche energy (Note 3)		E_{AR}	18	mJ
Channel temperature (Note 4)		T_{ch}	175	°C
Storage temperature range (Note 4)		T_{stg}	−55 to 175	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch\text{-}c)}$	0.83	°C/W



Note 1: Please use devices on condition that the channel temperature is below 175°C.

Note 2: V_{DD} = 25 V, T_{ch} = 25°C, L = 13 μH, R_G = 25 Ω, I_{AR} = 100 A

Note 3: Repetitive rating; pulse width limited by maximum channel temperature.

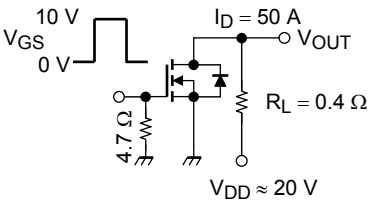
Note 4: 175°C refers to AEC-Q101.

Note 5: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic sensitive device. Please handle with caution

Start of commercial production
2008-03

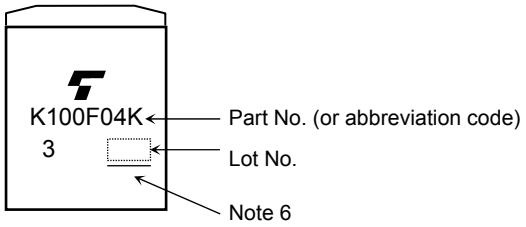
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	40	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	20	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	3.0	—	4.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 50 A	—	2.5	3.0	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 50 A	87	174	—	S
Input capacitance		C_{iss}	V_{DS} = 10V, V_{GS} = 0 V, f = 1 MHz	—	4500	—	pF
Reverse transfer capacitance		C_{rss}		—	900	—	
Output capacitance		C_{oss}		—	1100	—	
Switching time	Rise time	t_r	 Duty ≤ 1%, t_w = 10 μs	—	21	—	ns
	Turn-ON time	t_{on}		—	37	—	
	Fall time	t_f		—	31	—	
	Turn-OFF time	t_{off}		—	75	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 32 V, V_{GS} = 10 V, I_D = 100 A	—	102	—	nC
Gate-source charge		Q_{gs}		—	56	—	
Gate-drain (“miller”) charge		Q_{gd}		—	46	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	100	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	300	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 100 A, V_{GS} = 0 V	—	—	−1.2	V
Reverse recovery time	t_{rr}	I_{DR} = 100 A, V_{GS} = 0 V,	—	61	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = 50 A/μs	—	49	—	nC

Marking



Note 6: A line under a Lot No. identifies the indication of product Labels.
[[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

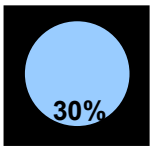
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Moisture-Proof Packing

The TK100F04K3 is packed in a moisture-proof laminated aluminum bag.

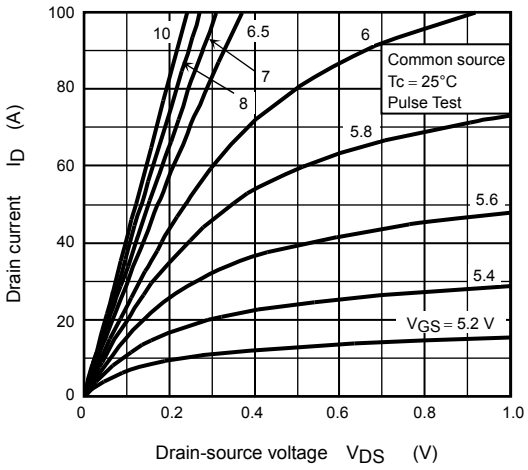
Precautions for Transportation and Storage

(1) Avoid excessive vibration during transportation.
(2) Do not toss or drop the packed devices to avoid ripping of the bag.
(3) After opening the moisture-proof bag, the devices should be assembled within two weeks in an environment of 5°C to 30°C and RH70% or below. Perform reflow at most twice.
(4) The moisture-proof bag may be stored unopened for up to 12 months at 5°C to 30°C and RH90% or below.
(5) If, upon opening the bag, the moisture indicator card shows humidity of 30% or above (the color of the 30% dot has changed from blue to pink) or the expiration date has passed, the devices should be baked as follows:
Baking conditions: 125°C for 48 hours.
Since the tape materials are not heat-proof, devices should be placed on either heat-proof trays or aluminum magazines when baking.

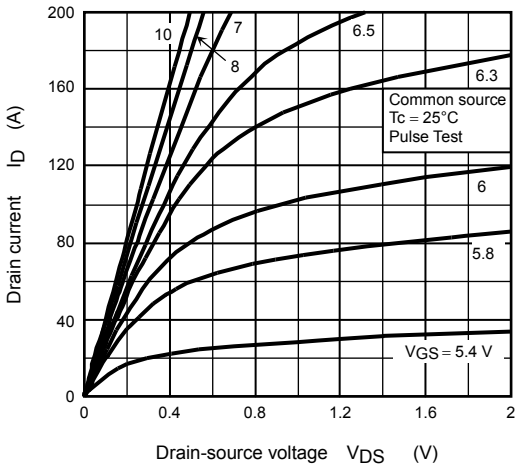


The humidity indicator shows an approximate ambient humidity at 25°C.
If the ambient humidity is below 30%, the color of all the indicator dots is blue.
If, upon opening the bag, the color of the 30% dot has changed from blue to pink, the devices should be baked before assembly.

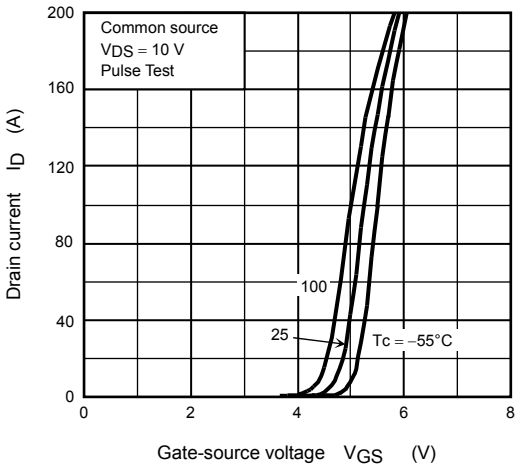
$I_D - V_{DS}$



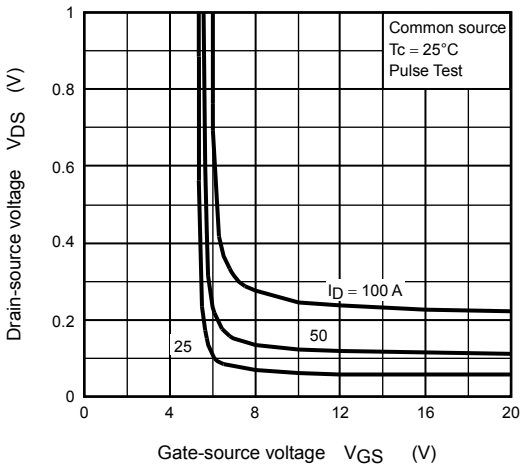
$I_D - V_{DS}$



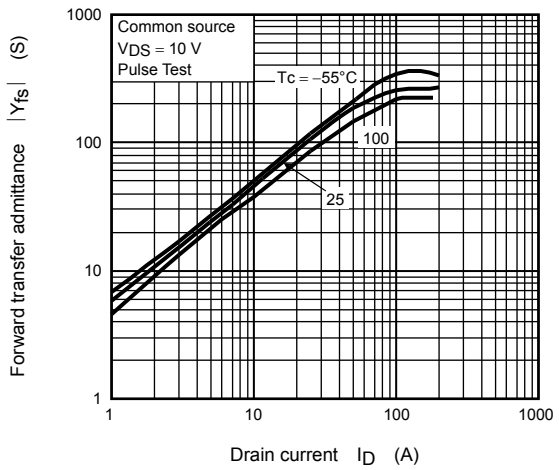
$I_D - V_{GS}$



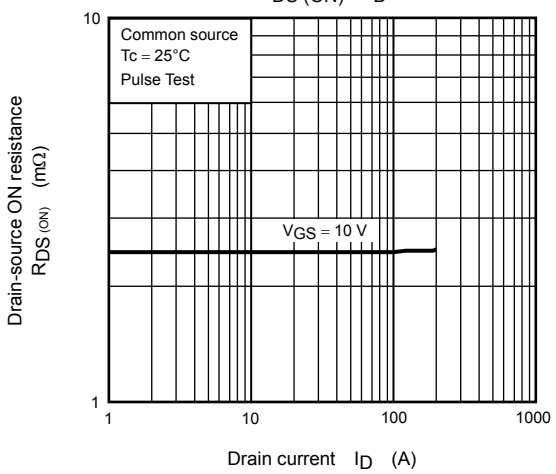
$V_{DS} - V_{GS}$



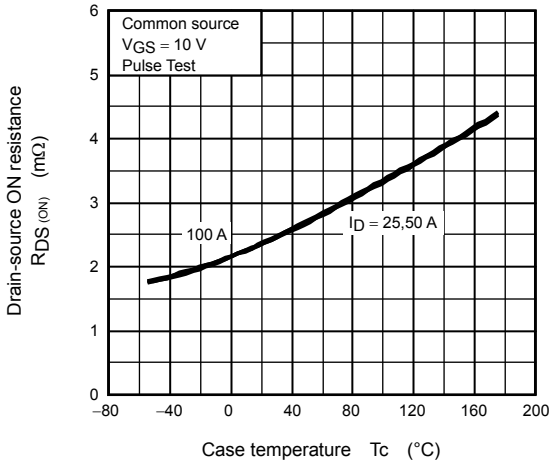
$|Y_{fs}| - I_D$



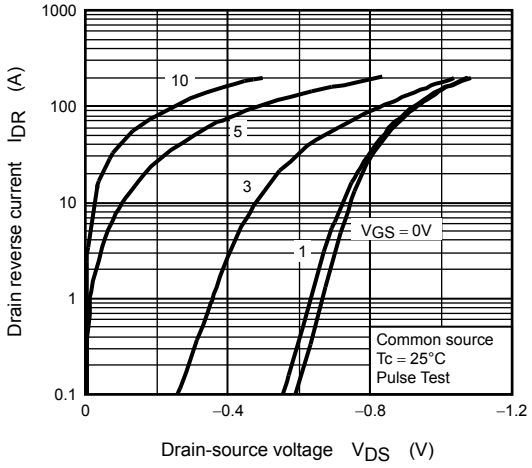
$R_{DS\ (ON)} - I_D$



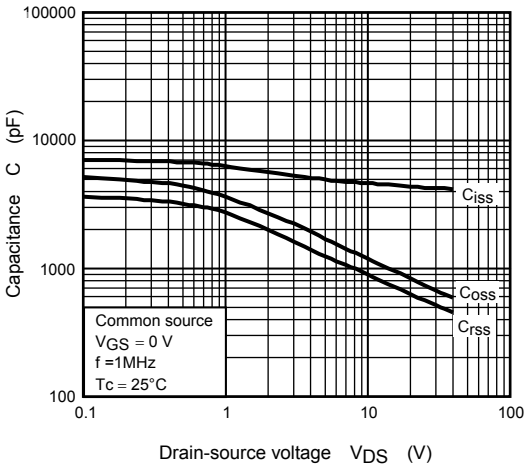
$R_{DS\ (ON)}$ – Tc



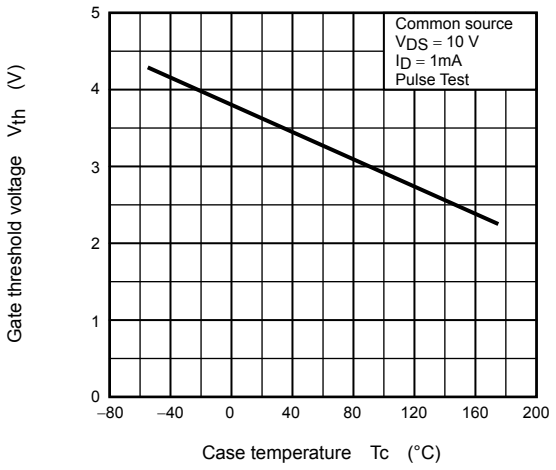
I_{DR} – V_{DS}



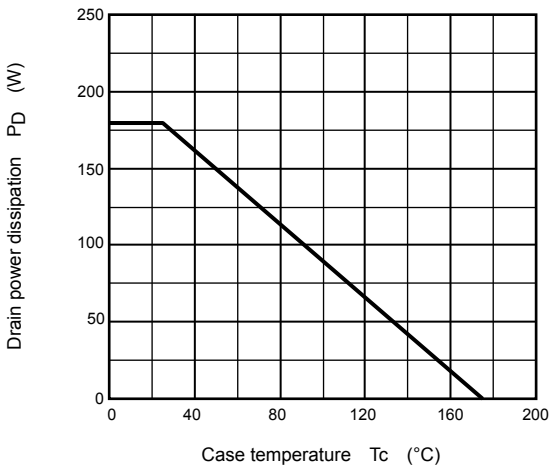
Capacitance – V_{DS}



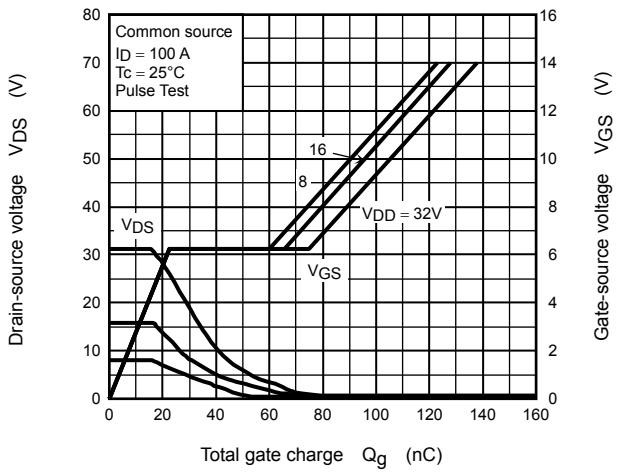
V_{th} – Tc



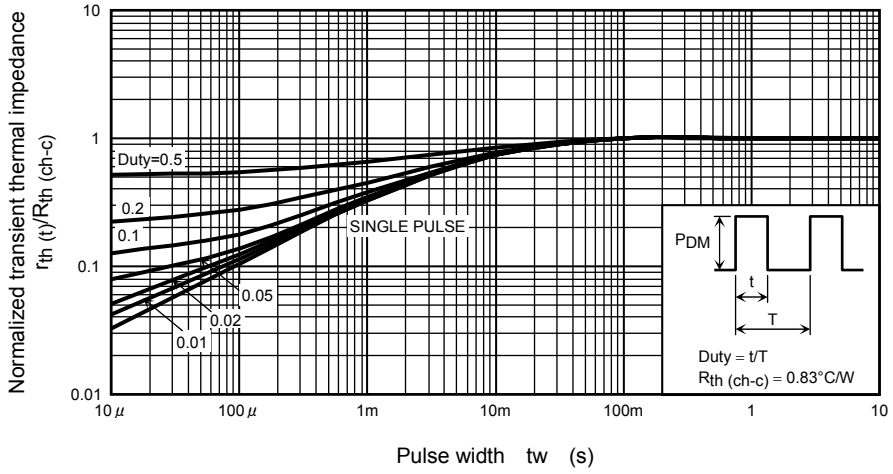
P_D – Tc



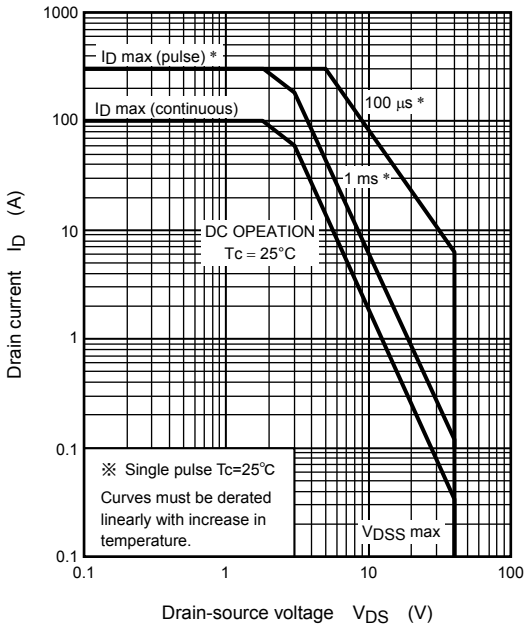
Dynamic input / output characteristics



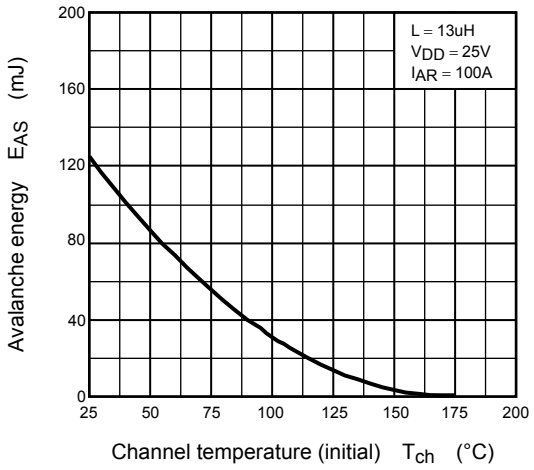
$r_{th} - t_w$

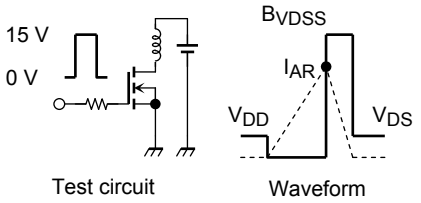


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





$R_G = 25\ \Omega$
V_{DD} = 25 V, L = 13 μH

$$E = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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