

# LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

## FEATURES

Improved Replacement for SILICONIX, FAIRCHILD, & NATIONAL: 2N5911 & 2N5912

LOW NOISE (10kHz)  $e_n \sim 4nV/\sqrt{Hz}$

HIGH TRANSCONDUCTANCE (100MHz)  $g_{fs} \geq 4000\mu S$

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

@ 25 °C (unless otherwise stated)

## Maximum Temperatures

Storage Temperature -55 to +150 °C

Operating Junction Temperature -55 to +150 °C

## Maximum Power Dissipation

Continuous Power Dissipation (Total)<sup>4</sup> 500mW

## Maximum Currents

Gate Current 50mA

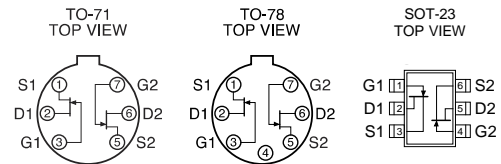
## Maximum Voltages

Gate to Drain -25V

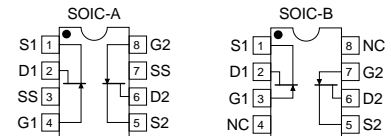
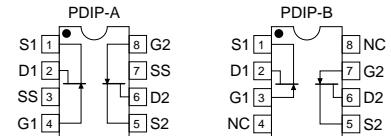
Gate to Source -25V

## LS5911 LS5912 LS5912C

IMPROVED LOW NOISE WIDEBAND  
MONOLITHIC DUAL N-CHANNEL  
JFET AMPLIFIER



## TOP VIEW



## MATCHING ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$ V_{GS1} - V_{GS2} $	Differential Gate to Source Cutoff Voltage			10		15		40	mV	$V_{DG} = 10V, I_D = 5mA$
$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	Differential Gate to Source Voltage Change with Temperature			20		40		40	$\mu V/^\circ C$	$V_{DG} = 10V, I_D = 5mA$ $T_A = -55 \text{ to } +125^\circ C$
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio		0.95	1	0.95	1	0.95	1		$V_{DS} = 10V, V_{GS} = 0V$ Notes 2, 3
$ I_{G1} - I_{G2} $	Differential Gate Current			20		20		20	nA	$V_{DG} = 10V, I_D = 5mA$ $T_A = +125^\circ C$
$\frac{g_{fs1}}{g_{fs2}}$	Forward Transconductance Ratio		0.95	1	0.95	1	0.95	1		$V_{DS} = 10V, I_D = 5mA$ $f = 1kHz^3$
CMRR	Common Mode Rejection Ratio	85							dB	$V_{DG} = 5V \text{ to } 10V$ $I_D = 5mA$

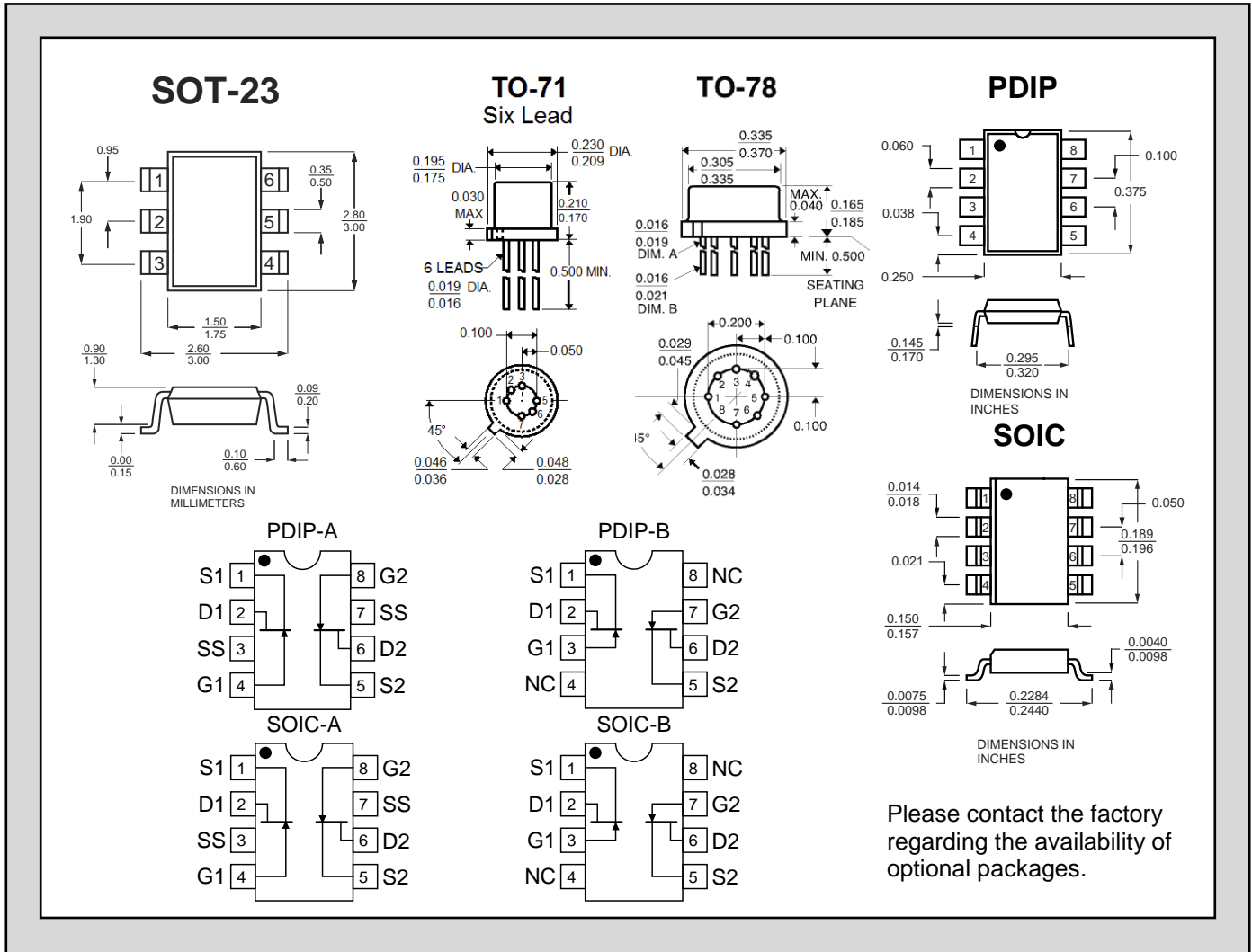
## STATIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)

SYM.	CHARACTERISTIC	TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{GSS}$	Gate to Source Breakdown		-25		-25		-25		V	$I_G = -1\mu A, V_{DS} = 0V$
$V_{GS(off)}$	Gate to Source Cutoff Voltage		-1	-5	-1	-5	-1	-5		$V_{DS} = 10V, I_D = 1nA$
$V_{GS(F)}$	Gate to Source Forward Voltage	0.7								$I_G = 1mA, V_{DS} = 0V$
$V_{GS}$	Gate to Source Voltage		-0.3	-4	-0.3	-4	-0.3	-4		$V_{DG} = 10V, I_G = 5mA$
$I_{DSS}$	Drain to Source Saturation		7	40	7	40	7	40	mA	$V_{DS} = 10V, V_{GS} = 0V$
$I_{GSS}$	Gate Leakage Current	-1		-50		-50		-50	pA	$V_{GS} = -15V, V_{DS} = 0V$
$I_G$	Gate Operating Current	-1		-50		-50		-50		$V_{DG} = 10V, I_D = 5mA$
$I_{G1G2}$	Gate to Gate Isolation Current			$\pm 1$		$\pm 1$		$\pm 1$		$V_{G1} - V_{G2} = \pm 25V, I_D = I_S = 0$

Linear Integrated Systems

**DYNAMIC ELECTRICAL CHARACTERISTICS @25 °C (unless otherwise stated)**

SYM.	CHARACTERISTIC	TYP	LS5911		LS5912		LS5912C		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX	MIN	MAX		
g <sub>fs</sub>	Forward Transconductance	f = 1kHz	4000	10000	4000	10000	4000	10000	μS	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA
		f = 100MHz	7000							
g <sub>os</sub>	Output Conductance	f = 1kHz		100		100		100	pF	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 1MHz
		f = 100MHz	120							
C <sub>iss</sub>	Input Capacitance			5		5		5	pF	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 1MHz
C <sub>rss</sub>	Reverse Transfer Capacitance			1.2		1.2		1.2		
NF	Noise Figure			1		1		1	dB	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 10kHz, R <sub>G</sub> = 100KΩ
e <sub>n</sub>	Equivalent Input Noise Voltage	f = 100Hz	7	20		20		20	nV/√Hz	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 100Hz
		f = 10kHz	4	10		10		10	nV/√Hz	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 10kHz



## NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test:  $PW \leq 300\mu s$  Duty Cycle  $\leq 3\%$
3. Assumes smaller value in numerator.
4. Derate  $4mW/^{\circ}C$  above  $25^{\circ}C$ .

Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.