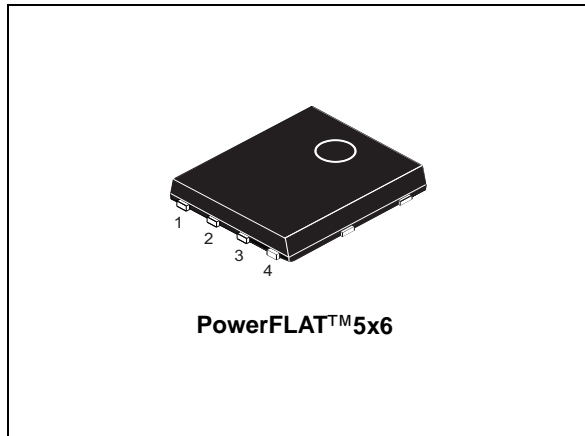


N-channel 30 V, 0.0027  $\Omega$  typ., 28 A STripFET™ VII DeepGATE™ Power MOSFET plus monolithic Schottky in a PowerFLAT™ 5x6

Datasheet - preliminary data



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL110NS3LLH7	30 V	0.0034 $\Omega$	28 A

- Very low on-resistance
- Very low Q<sub>g</sub>
- High avalanche ruggedness
- Embedded Schottky diode
- High junction temperature capability (175 °C)

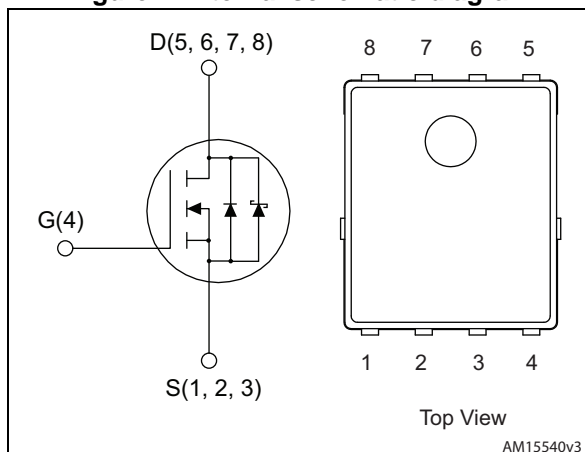
## Applications

- Switching applications

## Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL110NS3LLH7	110NS3LL	PowerFLAT™ 5x6	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous)	110	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	78	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	440	A
$I_D^{(3)}$	Drain current (continuous)	28	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	20	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	112	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	75	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ °C}$	4.8	W
$T_j$	Max. operating junction temperature	-55 to 175	°C

1. This value is rated according to  $R_{thj-c}$
2. Pulse width limited by safe operating area.
3. This value is rated according to  $R_{thj-pcb}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	°C/W
$R_{thj-case}$	Thermal resistance junction-case max	2	°C/W

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}$			500	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	1.2			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 14\text{ A}$		0.0027	0.0034	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 14\text{ A}$		0.004	0.005	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	2080	-	pF
$C_{oss}$	Output capacitance		-	660	-	pF
$C_{riss}$	Reverse transfer capacitance		-	34	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}, I_D = 28\text{ A},$ $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 3</a> )	-	13	-	nC
$Q_{gs}$	Gate-source charge		-	6.7	-	nC
$Q_{gd}$	Gate-drain charge		-	2.5	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}, I_D = 14\text{ A},$ $R_G = 2\text{ }\Omega, V_{GS} = 4.5\text{ V}$	-	10	-	ns
$t_r$	Rise time		-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
$t_f$	Fall time		-	7.5	-	ns

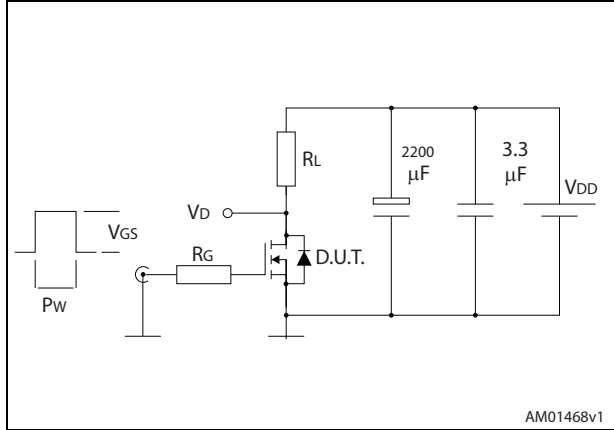
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		28	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		112	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2 \text{ A}, V_{GS} = 0$	-	0.4	0.7	V
$t_{rr}$	Reverse recovery time	$I_D = 28 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 20 \text{ V}$	-	31.2		ns
$Q_{rr}$	Reverse recovery charge		-	18.7		nC
$I_{RRM}$	Reverse recovery current		-	1.2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

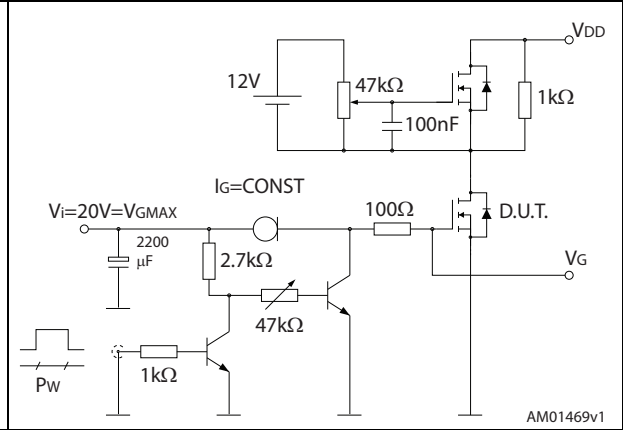
### 3 Test circuits

Figure 2. Switching times test circuit for resistive load



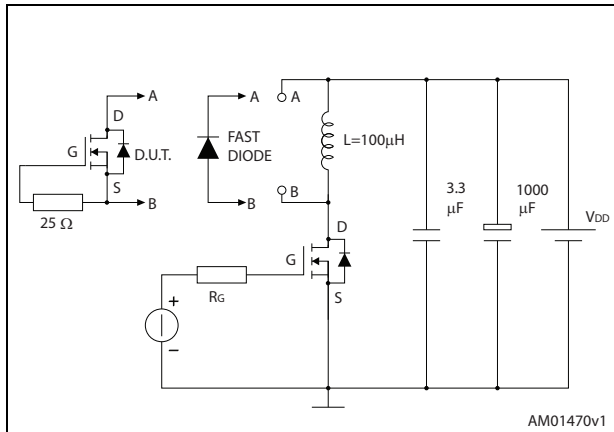
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Figure 3. Gate charge test circuit



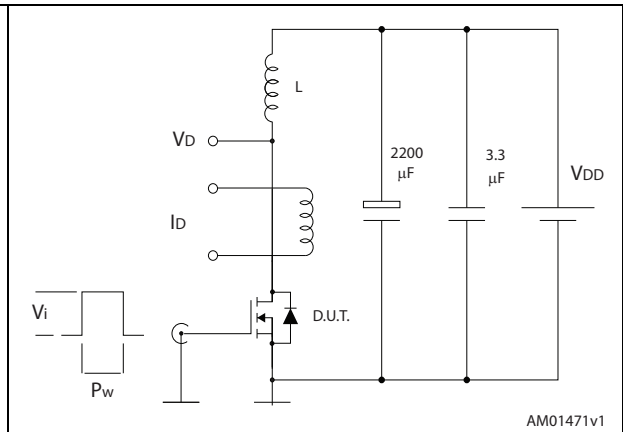
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Figure 4. Test circuit for inductive load switching and diode recovery times



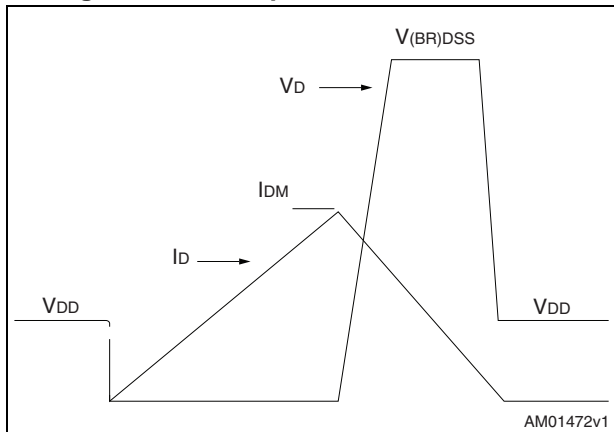
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Figure 5. Unclamped inductive load test circuit



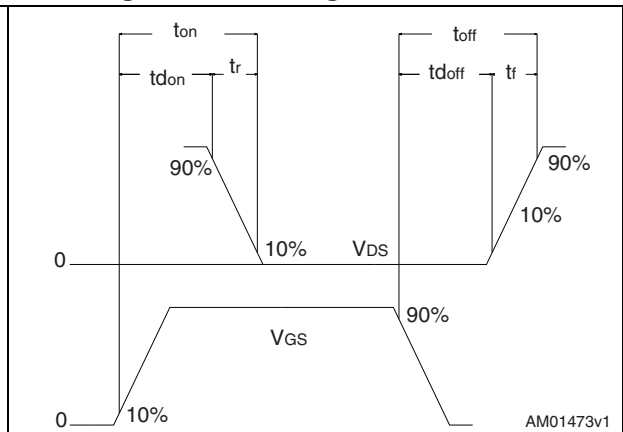
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35



Figure 8. PowerFLAT™ 5x6 type S-C mechanical data

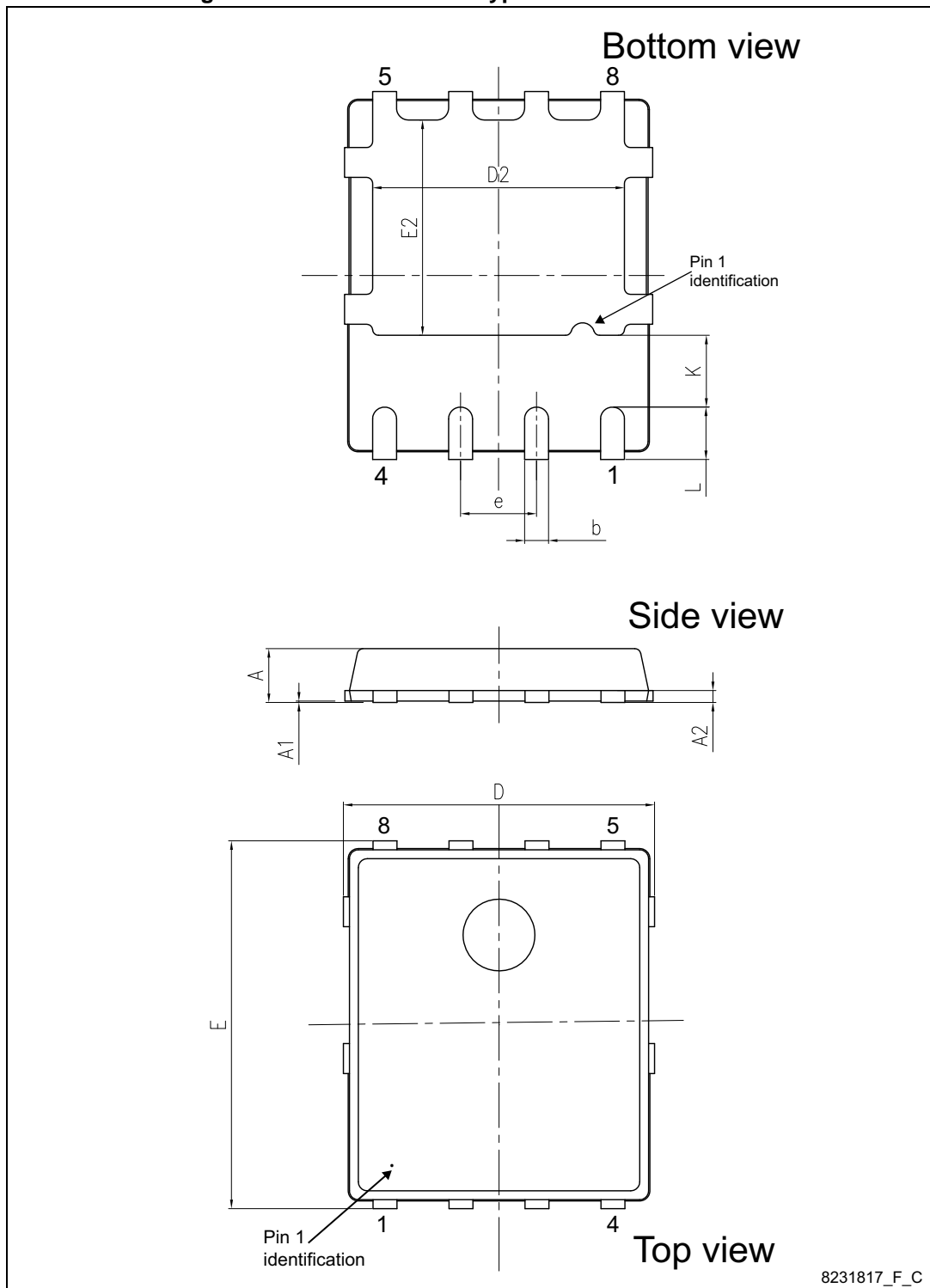
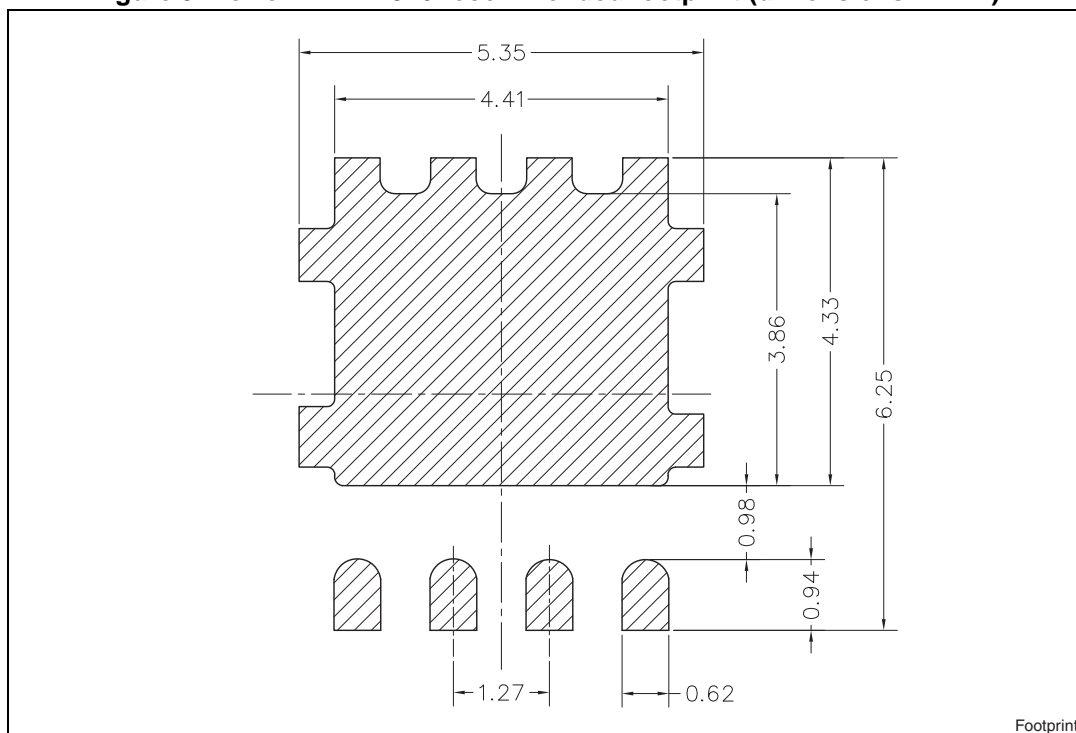


Figure 9. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



Footprint

# 5 Packaging mechanical data

Figure 10. PowerFLAT™ 5x6 tape(a)

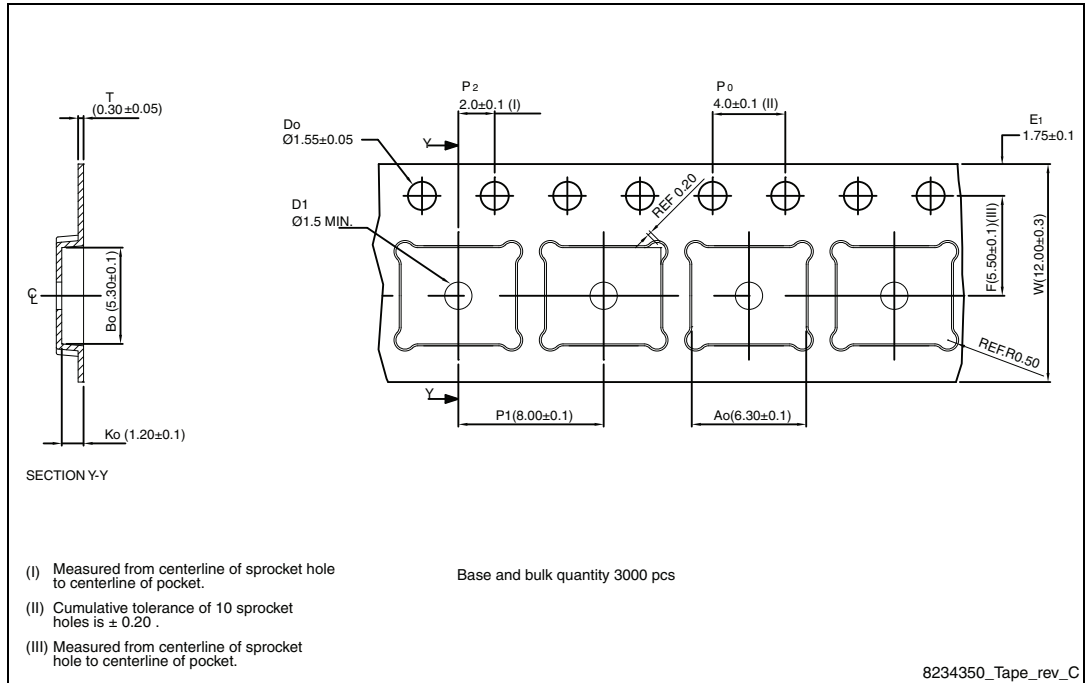
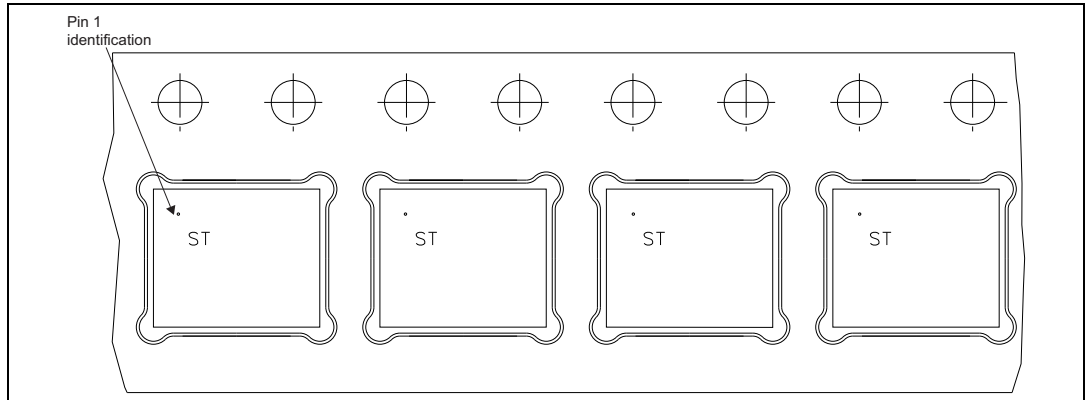
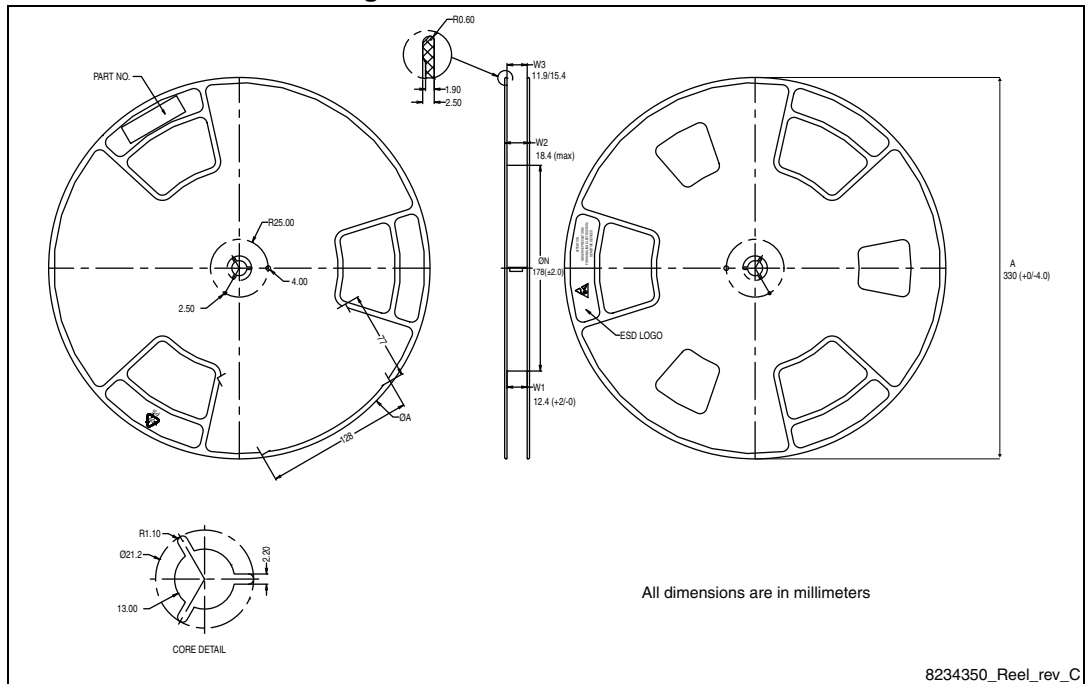


Figure 11. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 12. PowerFLAT™ 5x6 reel



## 6 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Apr-2013	1	First release.
11-Jun-2013	2	– Changed: <i>Description</i> – Minor text changes

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