Standard Products

UT54ACS299E

CMOS 8-bit Universal Shift/Storage Register with Three-State Outputs
Datasheet

July 2, 2013
www.aeroflex.com/Logic

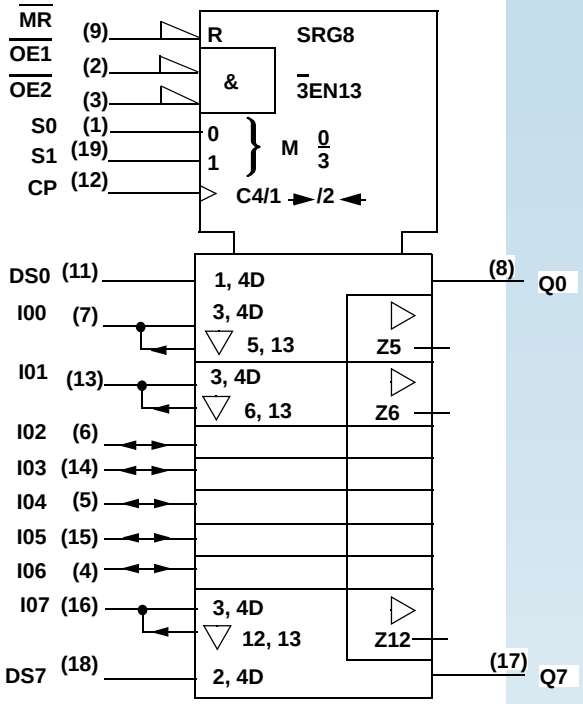
FEATURES

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Three-state outputs for bus-oriented applications
- Operate with outputs enabled or at high impedance
- Four operating modes: shift left, shift right, load and store
- Can be cascaded for n-bit word lengths
- 0.6µm Commercial RadHard™ CMOS
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
  - SEU Onset LET: 95 MeV-cm^2/mg (4.5V) and 48MeV-cm^2/mg (3.0V)
- Applications:
  - Stacked or push-down registers
  - Buffer storage
  - Accumulator registers
- Output source/sink 24mA
- Available QML Q or V processes
- Standard Microcircuit Drawing 5962-06238
- Package:
  - 20-lead flatpack

DESCRIPTION

The UT54ACS299E 8-bit shift/storage register is built using Aeroflex's Commercial RadHard™ epitaxial CMOS technology and is ideal for space applications. The UT54ACS299E is an 8-bit universal shift/storage register featuring multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) inputs and two output enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the mode of operation listed in the function table. Additional outputs are provided for flip flops Q0, Q7 to allow easy serial cascading. A separate active low master reset ($\overline{MR}$) is used to reset the register, overriding the select and CP inputs. All flip-flops are brought out through three-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. All other state changes are initiated by the rising edge of the clock.

LOGIC SYMBOL



PIN DESCRIPTION

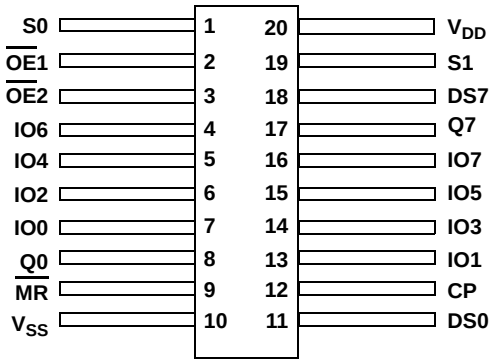
Pin Names	Description
CP	Clock Pulse Input
DS0	Serial Data Input for Right Shift
DS7	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE1}$, $\overline{OE2}$	Three-State Output Enable Inputs
IO0-IO7	Parallel Data Inputs or Three-State Parallel Outputs
Q0, Q7	Serial Outputs

FUNCTION TABLE

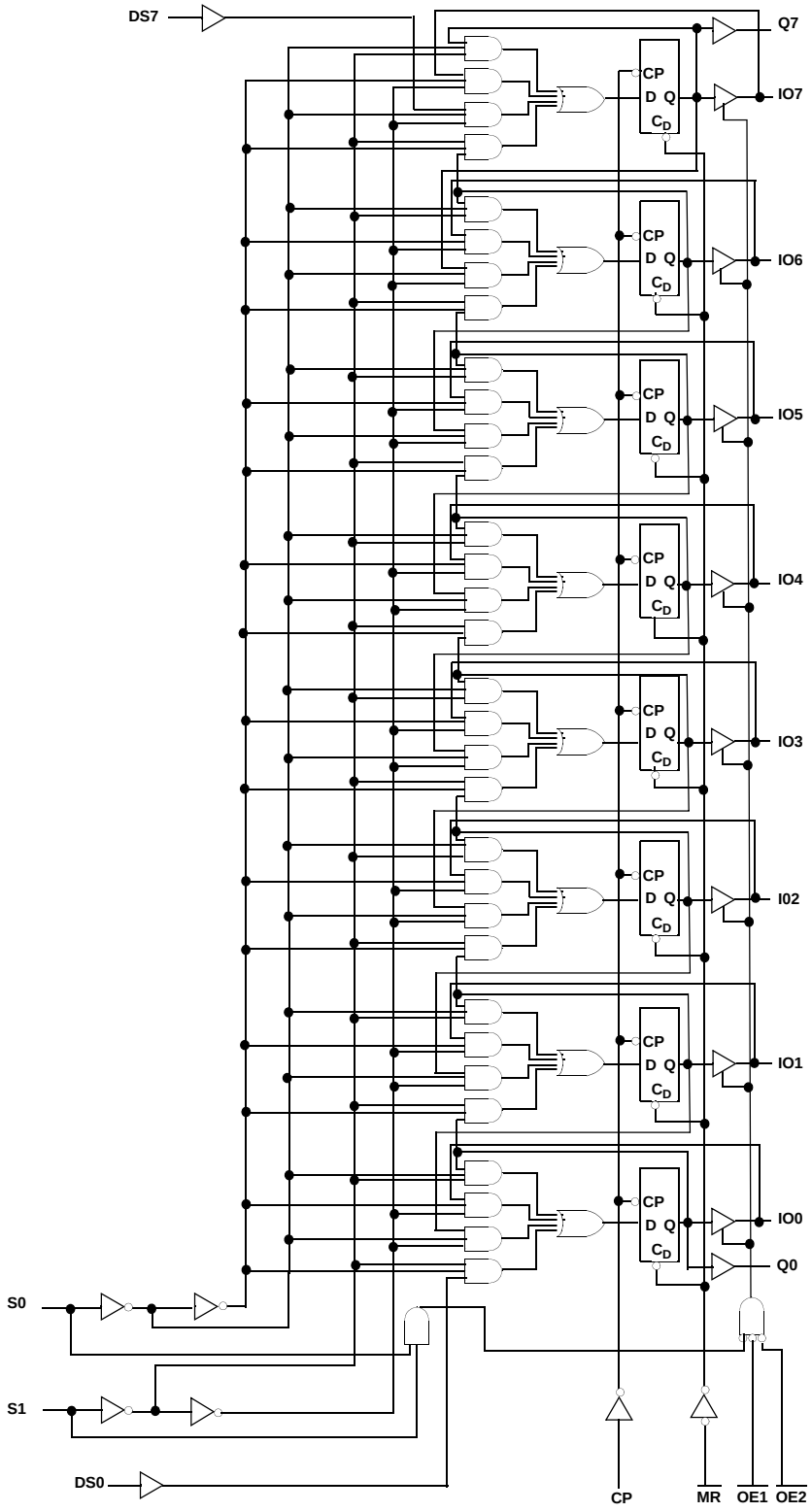
INPUTS						OPERATION
$\overline{MR}$	S1	S0	CP	$\overline{OE1}$	$\overline{OE2}$	
L	X	L	X	L	L	Q0=Q7=Low, Async Reset
L	L	X	X	L	L	Q0=Q7=Low, Async Reset
L	H	H	X	X	X	Q0=Q7=Low, I/O = Hiz, Async Reset
H	H	H	↑	X	X	Parallel Load; IOn > Qn
H	L	H	↑	L	L	Shift Right; DS0 > Q0,Q0 > Q1, etc.
H	H	L	↑	L	L	Shift Left; DS7 > Q7, Q7 > Q6, etc.
H	L	L	X	L	L	Hold

PINOUTS

20-Lead Flatpack
Top View



LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E5	rad(Si)
SEL Immune	>108	MeV-cm^2/mg
SEU Onset LET - 3.0V SEU Onset LET - 4.5V	48 95	MeV-cm^2/mg
SEU Error Rate - 3.0V[2] SEU Error Rate - 4.5V[2]	1.4E-8 8.1E-10	errors/device-day
Neutron Fluence[3]	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Adam's 90% worst case particle environment, geosynchronous orbit, 100 mils aluminum shielding.
3. Not tested, inherent of CMOS technology.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT (Mil only)	UNITS
$V_{I/O}$	Voltage any pin during operation	-.3 to V_{DD} +.3	V
V_{DD}	Supply voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	200	mW

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C
t_{INRISE} t_{INFALL}	Maximum input rise or fall time (V_{IN} transitioning between V_{IL} (max) and V_{IH} (min))	20	ns

DC ELECTRICAL CHARACTERISTICS [1]
(-55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
V_{IL}	Low level input voltage[2]	V_{DD} from 3.0V to 5.5V			0.3 V_{DD}	V
V_{IH}	High level input voltage[2]	V_{DD} from 3.0V to 5.5V		0.7 V_{DD}		V
I_{IN}	Input leakage current	V_{DD} from 3.0V to 5.5V V_{IN} = V_{DD} or V_{SS}		-1	1	µA
I_{OZ}	Three-state output leakage current	V_{DD} from 3.0V to 5.5V V_{IN} = V_{DD} or V_{SS}		-10	10	µA
I_{OS}	Short-circuit output current [4, 5]	V_O = V_{DD} or V_{SS} V_{DD} from 3.0V to 5.5V		-600	600	mA
V_{OL1}	Low-level output voltage [6]	I_{OL} = 12mA I_{OL} = 100µA V_{DD} = 3.0V to 3.6V V_{IN} = 0.7V_{DD} or 0.3V_{DD}			0.4 0.2	V
V_{OL2}	Low-level output voltage [6]	I_{OL}= 24mA	-55°C, 25°C		0.36	V
		I_{OL}= 24mA	+125°C		0.5	
		I_{OL}= 100µA V_{DD} = 4.5V to 5.5V V_{IN} = 0.7V_{DD} or 0.3V_{DD}			0.2	
V_{OL3}	Low-level output voltage[6, 7]	I_{OL}= 50mA	-55°C, 25°C		0.8	V
		V_{DD} = 5.5V	+125°C		1.0	
		V_{IN} = 0.7V_{DD} or 0.3V_{DD}				
V_{OH1}	High-level output voltage[6]	I_{OH} = -12mA I_{OH} = -100µA V_{DD} = 3.0V to 3.6V V_{IN} = 0.7V_{DD} or 0.3V_{DD}		V_{DD} - 0.6 V_{DD} - 0.2		V
V_{OH2}	High-level output voltage[6]	I_{OH}= -24mA	-55°C, 25°C	V_{DD} - 0.64		V
		I_{OH}= -24mA	+125°C	V_{DD} - 0.8		
		I_{OH}= -100µA V_{DD} = 4.5V to 5.5V V_{IN} = 0.7V_{DD} or 0.3V_{DD}		V_{DD} - 0.2		

V_{OH3}	High-level output voltage[6, 7]	I_{OH}= -50mA V_{DD} = 5.5V V_{IN} = 0.7*V_{DD} or 0.3*V_{DD}	-55°C, 25°C +125°C	V_{DD} - 1.1 V_{DD} - 1.25		V
V_{IC}+	Positive input clamp voltage	For input under test, I_{IN} = 18mA V_{DD} = 0.0V		0.4	1.5	V
V_{IC}-	Negative input clamp voltage	For input under test, I_{IN} = -18mA V_{DD} = open		-1.5	-0.4	V
P_{total}	Power dissipation [3, 8, 9]	C_L = 20pF V_{DD} from 3.0V to 5.5V			0.5	mW/ MHz
I_{DDQ}	Standby Supply Current V_{DD} Pre-Rad 25°C Pre-Rad -55°C to +125°C Post-Rad 25°C	V_{IN} = V_{DD} or $V_{SS,}$ V_{DD} = 5.5 $\overline{OE}$n = V_{DD} $\overline{OE}$n = V_{DD} $\overline{OE}$n = V_{DD}			 10 80	 µA µA
C_{IN}	Input capacitance[10]	*f* = 1MHz @ 0V V_{DD} from 3.0V to 5.5V			17	pF
C_{OUT}	Output capacitance[10]	*f* = 1MHz @ 0V V_{DD} from 3.0V to 5.5V			17	pF

Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
3. Guaranteed by characterization.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Supplied as a design limit, but not guaranteed or tested.
6. Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
7. Transmission driving tests are performed at V_{DD} = 5.5V, only one output loaded at a time with a duration not to exceed 2ms. The test is guaranteed, if not tested, for V_{IN}=V_{IH} minimum or V_{IL} maximum.
8. Power does not include power contribution of any CMOS output sink current.
9. Power dissipation specified per switching output.
10. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

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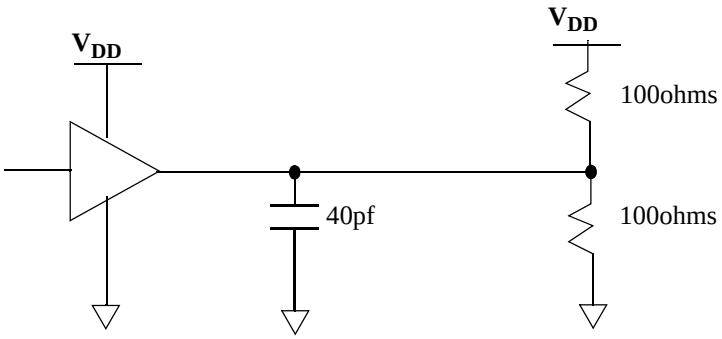
Test Load or Equivalent[1]



Notes:

1. Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

AC ELECTRICAL CHARACTERISTICS[1] (3.3 Volt Operation)

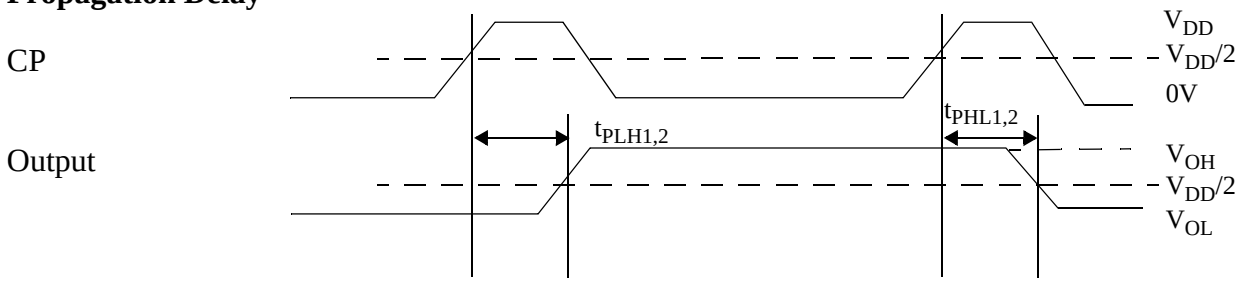
(V_{DD} = 3.3V ±0.3V, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{PLH1}	Propagation delay CP to Q0 or Q7 (shift left or right)	4.5	10.5	ns
t_{PHL1}	Propagation delay CP to Q0 or Q7 (shift left or right)	4.5	10.5	ns
t_{PLH2}	Propagation delay CP to IOn	5	14	ns
t_{PHL2}	Propagation delay CP to IOn	5	14	ns
t_{PHL3}	Propagation delay $\overline{MR}$ to Q0 or Q7	6	11	ns
t_{PHL4}	Propagation delay $\overline{MR}$ to IOn	7	15.5	ns
t_{PZL}	Output enable time $\overline{OE}$ to IOn	4	10.5	ns
t_{PZH}	Output enable time $\overline{OE}$ to IOn	4	10.5	ns
t_{PLZ}	Output disable time $\overline{OE}$ to IOn	3	6.5	ns
t_{PHZ}	Output disable time $\overline{OE}$ to IOn	3	6.5	ns
t_{W1}[2]	Pulse width CP	5.5		ns
t_{W2}[2]	Pulse width $\overline{MR}$	5.5		ns
t_{S1}	Setup time; high or low; Sn to CP	3		ns
t_{H1}	Hold time; high or low; Sn to CP	0.5		ns
t_{S2}	Setup time; high or low; DSn to CP	1		ns
t_{H2}	Hold time; high or low; DSn to CP	0.5		ns
t_{S3}	Setup time; high or low; IOn to CP	1.5		ns
t_{H3}	Hold time; high or low; IOn to CP	0.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	1		ns
f_{MAX}[2]	Maximum frequency CP		70	MHz

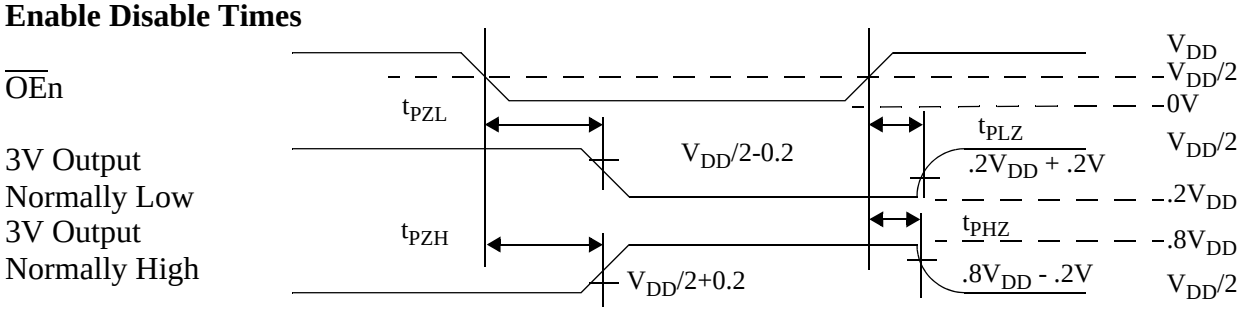
Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Verified by at speed functional test.

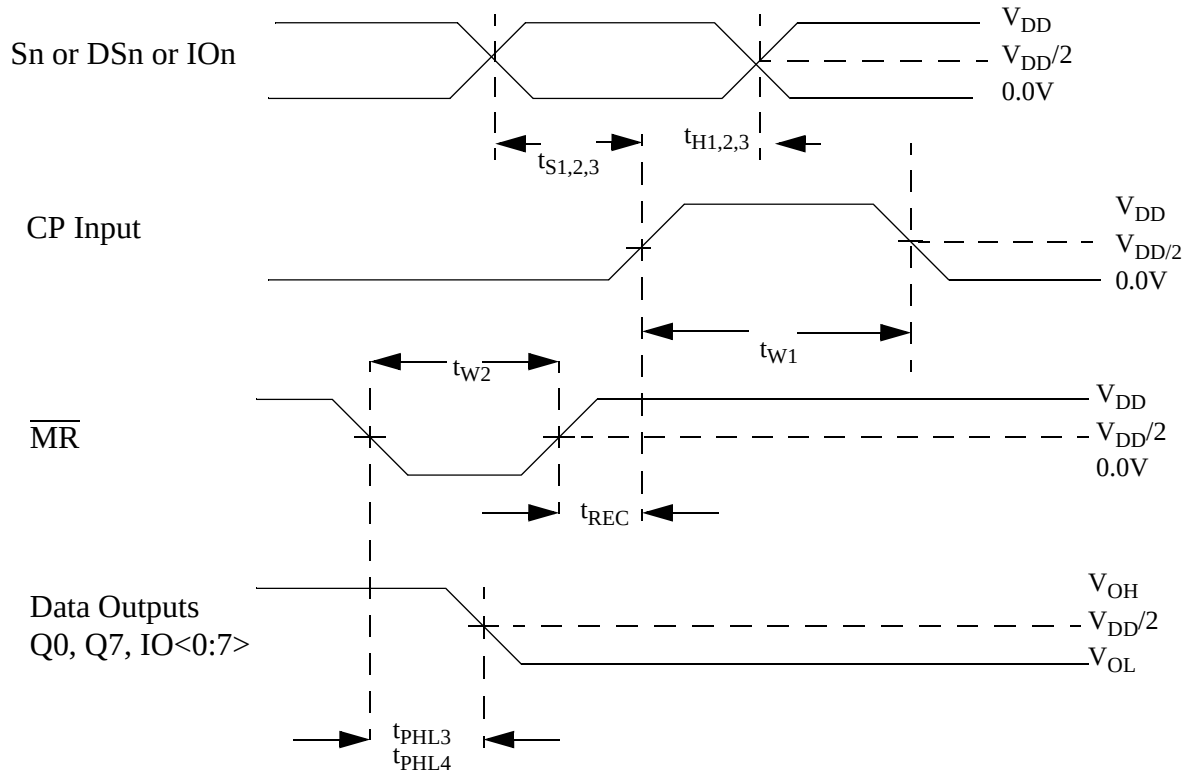
Propagation Delay



Enable Disable Times



Setup and Hold Measurements



AC ELECTRICAL CHARACTERISTICS[1] (5 Volt Operation)

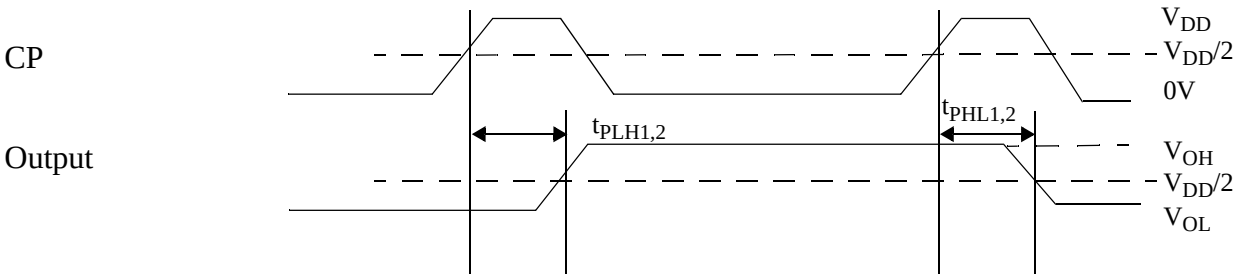
(V_{DD} = 5v ± 10%, -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{PLH1}	Propagation delay CP to Q0 or Q7 (shift left or right)	4	8	ns
t_{PHL1}	Propagation delay CP to Q0 or Q7 (shift left or right)	4	8	ns
t_{PLH2}	Propagation delay CP to IOn	4.5	9	ns
t_{PHL2}	Propagation delay CP to IOn	4.5	9	ns
t_{PHL3}	Propagation delay $\overline{MR}$ to Q0 or $_{Q7}$	5	9	ns
t_{PHL4}	Propagation delay $\overline{MR}$ to IOn	5.5	11	ns
t_{PZL}	Output enable time $\overline{OE}$ to IOn	3	7	ns
t_{PZH}	Output enable time $\overline{OE}$ to IOn	3	7	ns
t_{PLZ}	Output disable time $\overline{OE}$ to IOn	3	6	ns
t_{PHZ}	Output disable time $\overline{OE}$ to IOn	3	6	ns
t_{W1}[2]	Pulse width CP	5		ns
t_{W2}[2]	Pulse width $\overline{MR}$	5		ns
t_{S1}	Setup time; high or low; Sn to CP	2		ns
t_{H1}	Hold time; high or low; Sn to CP	0.5		ns
t_{S2}	Setup time; high or low; DSn to CP	1		ns
t_{H2}	Hold time; high or low; DSn to CP	.5		ns
t_{S3}	Setup time; high or low; IOn to CP	1		ns
t_{H3}	Hold time; high or low; IOn to CP	0.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	0.5		ns
f_{MAX}[2]	Maximum frequency CP		90	MHz

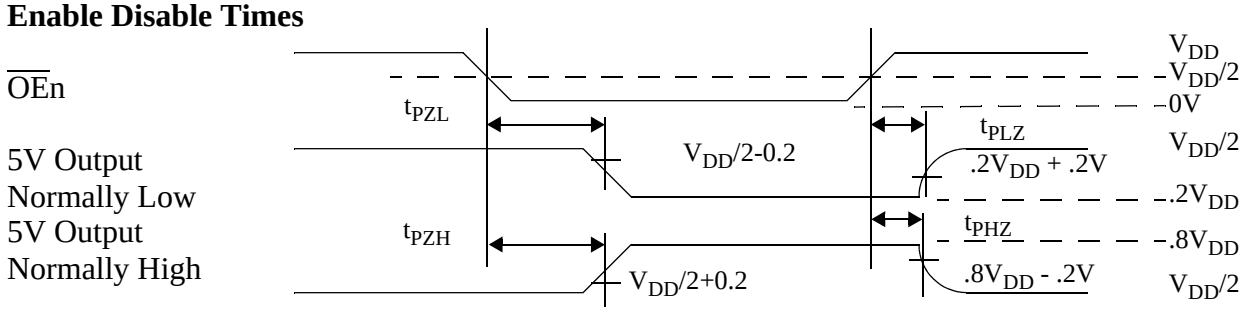
Notes:

1. All specifications valid for radiation dose ≤ 1E5 rad(Si) per MIL-STD-883, Method 1019.
2. Verified by at speed functional test.

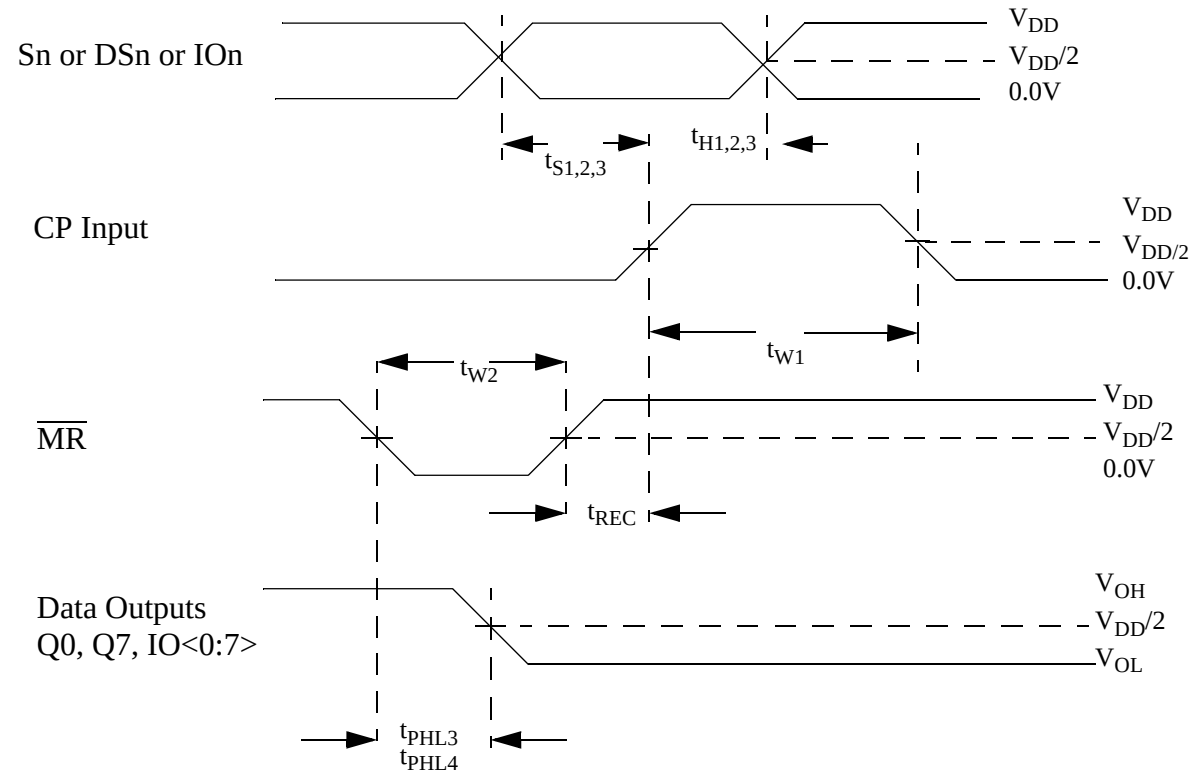
Propagation Delay



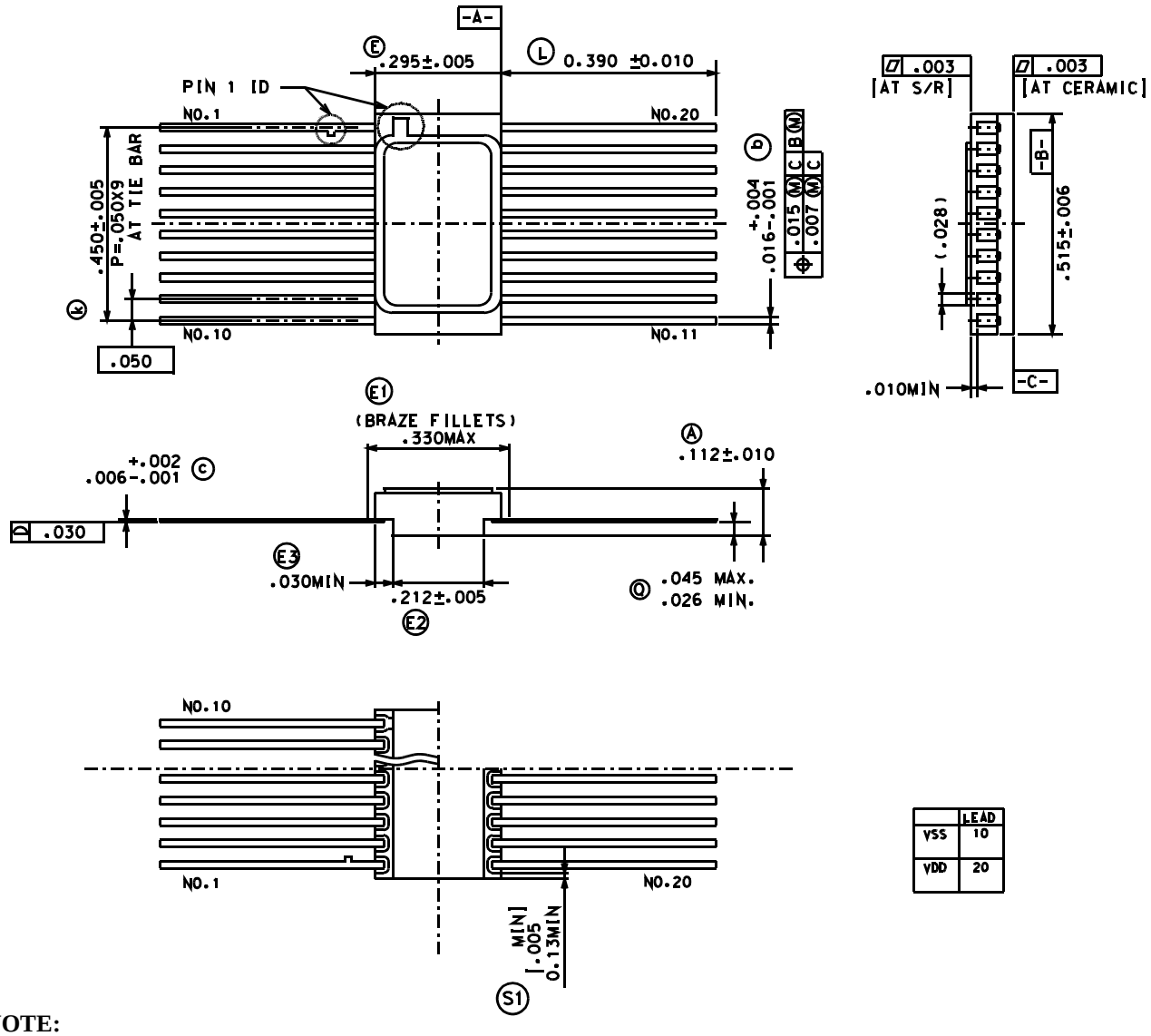
Enable Disable Times



Setup and Hold Measurements



PACKAGE



	LEAD
VSS	10
VDD	20

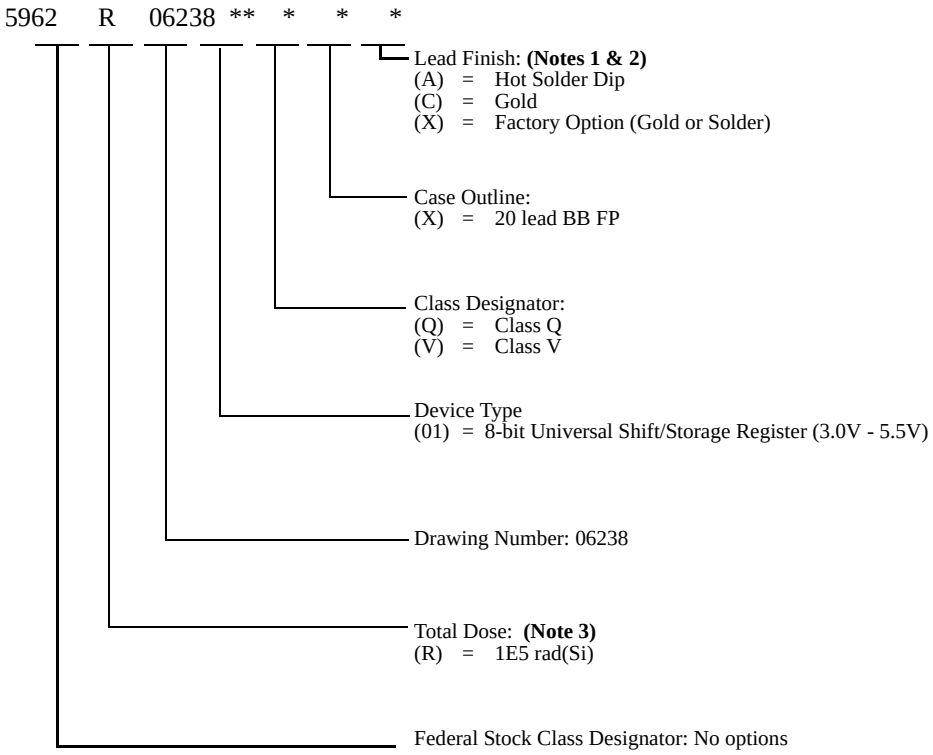
NOTE:

1. Seal ring is connected to V_{SS}.
2. Units are in inches.
3. All exposed metalized areas must be gold plated 100 to 225 microinches thick and all bottom side exposed metalized areas must be gold plated to 60 microinches thick nominal. Both sides shall be over electroplated nickel undercoating 100 to 350 microinches per MIL-PRF-38535.

Figure 1. 20-Lead Flatpack

ORDERING INFORMATION

UT54ACS299E: SMD



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q not available without radiation hardening. QML Q and QML V not available without radiation hardening. For prototyping inquiries, contact factory.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

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