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LC87F5R96B

CMOS IC

FROM 98K byte, RAM 4096 byte on-chip

8-bit 1-chip Microcontroller

Overview

The LC87F5R96B is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 98K-byte flash ROM (onboard programmable), 4096-byte RAM, On-chip debugging function, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO port, two UART ports (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, and a 27-source 10-vector interrupt feature.

Features

■Flash ROM

- Capable of on-board-programing with wide range, 2.7 to 5.5V, of voltage source
- Block-erasable in 128 byte units
- 100352 × 8 bits (Address: 00000H to 17FFFH, 1F800H to 1FFFFH)

■RAM

- 4096 × 9 bits

■Minimum Bus Cycle Time

- 83.3ns (12MHz) $V_{DD}=2.8$ to 5.5V
- 125ns (8MHz) $V_{DD}=2.5$ to 5.5V
- 500ns (2MHz) $V_{DD}=2.2$ to 5.5V

Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)

- 250ns (12MHz) $V_{DD}=2.8$ to 5.5V
- 375ns (8MHz) $V_{DD}=2.5$ to 5.5V
- 1.5 μ s (2MHz) $V_{DD}=2.2$ to 5.5V

■Ports

- Normal withstand voltage I/O ports

| | |
|--|--|
| Ports whose I/O direction can be designated in 1-bit units | 46 (P1n, P2n, P3n, P70 to P73, P80 to P86, PCn, PWM2, PWM3, XT2) |
| Ports whose I/O direction can be designated in 4-bit units | 8 (P0n) |
- Normal withstand voltage input port 1 (XT1)
- Dedicated oscillator ports 2 (CF1, CF2)
- Reset pins 1 (RES)
- Power pins 6 (V_{SS1} to 3, V_{DD1} to 3)

* This product is licensed from Silicon Storage Technology, Inc. (USA).

■ Timers

- Timer 0: 16-bit timer/counter with a capture register
 - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) ×2 channels
 - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
 - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
 - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
 - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
 - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
 - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8-bits)
 - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts programmable in 5 different time schemes.

■ High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 24MHz (at a main clock of 12MHz).
- 2) Can generate output real-time.

■ SIO

- SIO0: 8-bit synchronous serial interface
 - 1) LSB first/MSB first mode selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
 - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
 - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■ UART: 2 channels

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2 bit in continuous data transmission)
- Built-in baudrate generator (with baudrates of 16/3 to 8192/3 tCYC)

■ AD Converter: 8 bits × 11 channels

■ PWM: Multifrequency 12-bit PWM × 2 channels

■ Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- 1) Noise filtering function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
- 2) The noise filtering function is available for the INT3, T0IN, or T0HCP signal at P73. When P73 is read with an instruction, the signal level at that pin is read regardless of the availability of the noise filtering function.

■ Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

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■Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

■Interrupts

- 27 sources, 10 vector addresses

- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level | Interrupt Source |
|-----|----------------|--------|-----------------------------------|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L/INT4 |
| 4 | 0001BH | H or L | INT3/INT5/base timer0/base timer1 |
| 5 | 00023H | H or L | T0H/INT6 |
| 6 | 0002BH | H or L | T1L/T1H/INT7 |
| 7 | 00033H | H or L | SIO0/UART1 receive/UART2 receive |
| 8 | 0003BH | H or L | SIO/UART1 transmit/UART2 transmit |
| 9 | 00043H | H or L | ADC/T6/T7 |
| 10 | 0004BH | H or L | Port 0/T4/T5/PWM2, PWM3 |

- Priority levels $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 2048 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16-bits \times 8-bits (5 tCYC execution time)
- 24-bits \times 16-bits (12 tCYC execution time)
- 16-bits \div 8-bits (8 tCYC execution time)
- 24-bits \div 16-bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal) : For system clock
- CF oscillation circuit : For system clock, with internal Rf
- Crystal oscillation circuit : For low-speed system clock
- Multifrequency RC oscillation circuit (internal) : For system clock

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0 μ s, 2.0 μ s, 4.0 μ s, 8.0 μ s, 16.0 μ s, 32.0 μ s, and 64.0 μ s (at a main clock rate of 12MHz).

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■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC, and crystal oscillators automatically stop operation.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level.
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillators automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are four ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit

■ On-chip Debugger Function

- Permits software debugging with the test device installed on the target board.

■ Package Form

- QIP64E (14 × 14) : “Lead-free type”

■ Development Tools

- Evaluation (EVA) chip : LC87EV690
- Emulator : EVA62S + ECB876600D + SUB875M00 + POD64QFP
ICE-B877300 + SUB875M00 + POD64QFP
- On-chip-debugger : TCB87-TypeB + LC87F5R96B

■ Programming Boards

| Package | Programming boards |
|-----------------|--------------------|
| QIP64E(14 × 14) | W87F50256Q |

■ Flash ROM Programmer

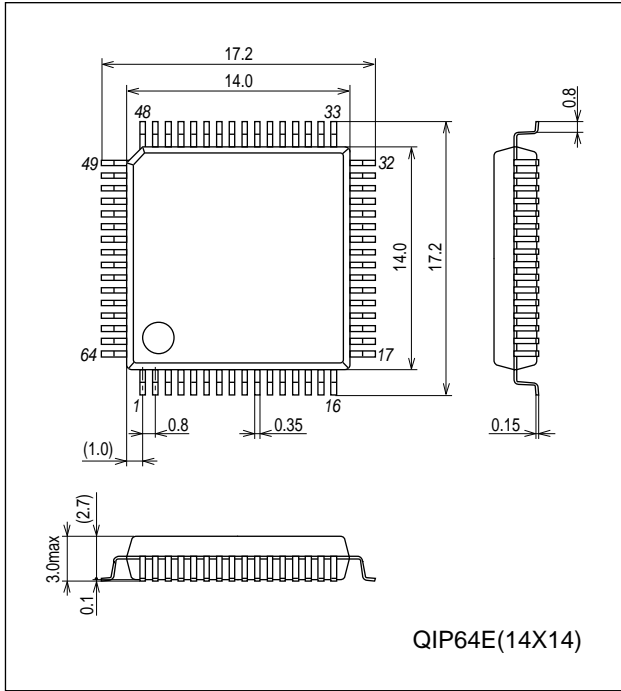
| Maker | Model | Support version(Note) | Device |
|-----------------------------------|---|---|------------|
| Flash Support Group, Inc.(Single) | AF9708/09/09B (including product of Ando Electric Co.,Ltd) | Revision : After Rev.02.73 | LC87F76C8A |
| Flash Support Group, Inc.(Gang) | AF9723(Main body) (including product of Ando Electric Co.,Ltd) | Revision : After Rev.02.29 | LC87F5NC8A |
| | AF9833(Unit) (including product of Ando Electric Co.,Ltd) | Revision : After Rev.01.88 | |
| Our company | SKK/SKK Type-B/SKK DBG Type-B (SANYO FWS) | Application Version: After 1.04 Chip Data Version: After2.11 | LC87F5R96B |

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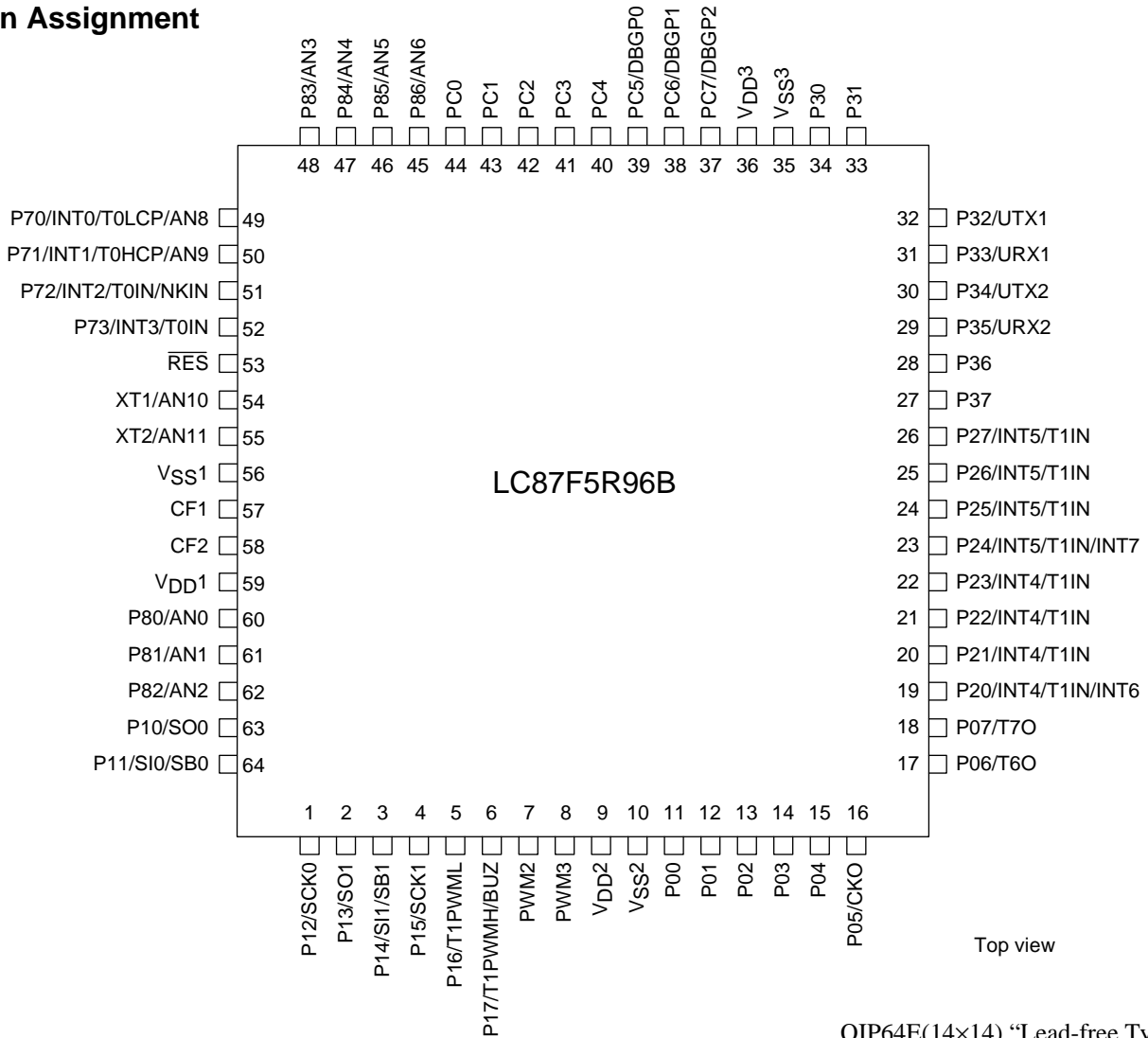
Package Dimensions

unit : mm (typ)

3159A

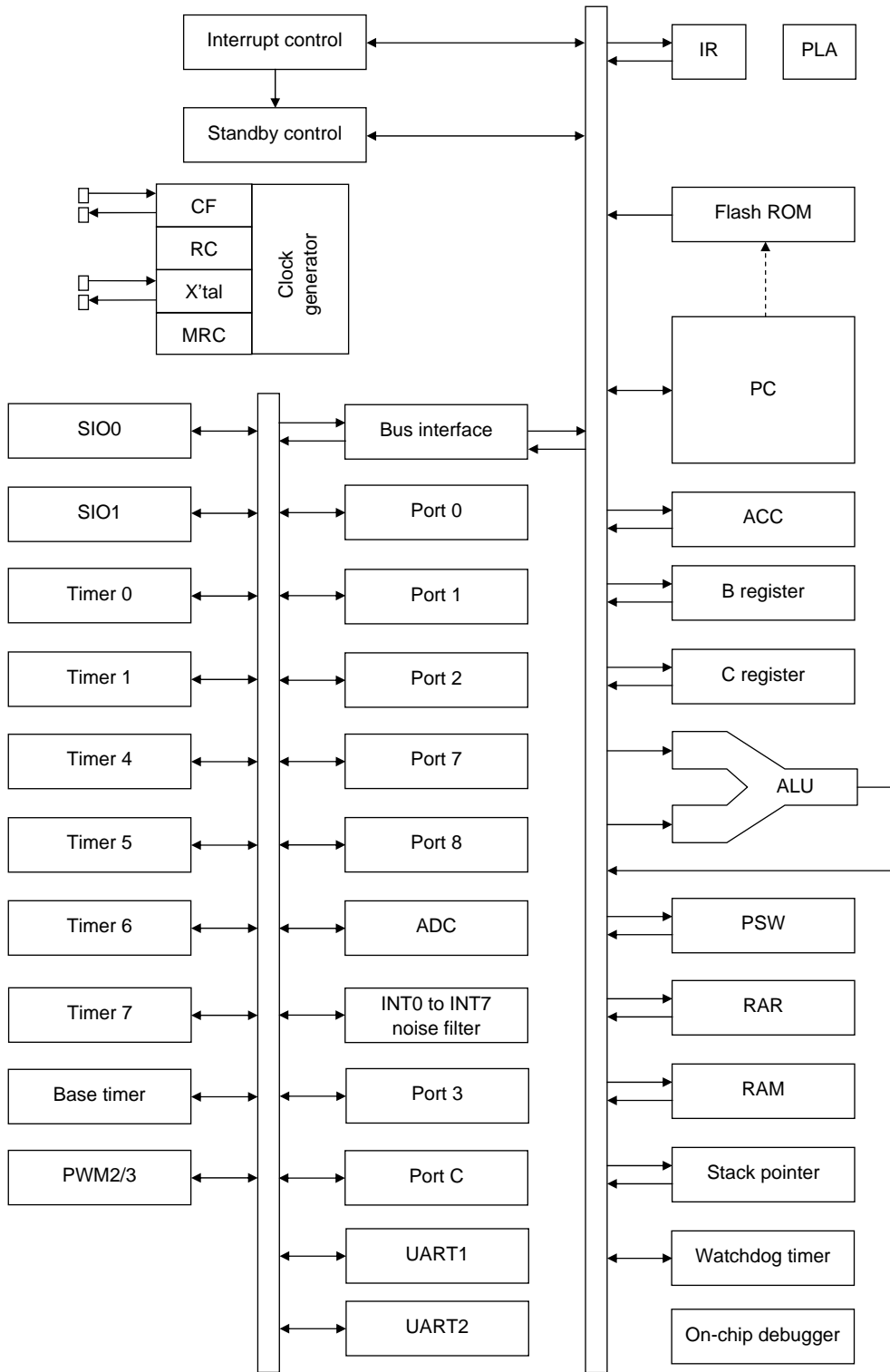


Pin Assignment



QIP64E(14x14) "Lead-free Type"

System Block Diagram



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Pin Description

| Pin Name | I/O | Description | Option | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--------|--|--------------------|---------|---------|--------------------|---------|---------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|-----|
| V _{SS1} , V _{SS2} V _{SS3} | - | - Power supply pin | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V _{DD1} , V _{DD2} V _{DD3} | - | + Power supply pin | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 0 P00 to P07 | I/O | <ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistor can be turned on and off in 4-bit units • HOLD release input • Port 0 interrupt input • Shared Pins <p>P05: Clock output (system clock/can selected from sub clock) P06: Timer 6 toggle output P07: Timer 7 toggle output</p> | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 1 P10 to P17 | I/O | <ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions <p>P10: SIO0 data output P11: SIO0 data input/bus I/O P12: SIO0 clock I/O P13: SIO1 data output P14: SIO1 data input/bus I/O P15: SIO1 clock I/O P16: Timer 1 PWML output P17: Timer 1 PWMH output/beeper output</p> | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 2 P20 to P27 | I/O | <ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Other functions <p>P20: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT6 input/timer 0L capture 1 input P21 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input P24: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT7 input/timer 0H capture 1 input P25 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input</p> <ul style="list-style-type: none"> • Interrupt acknowledge type <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th></th> <th style="text-align: center;">Rising</th> <th style="text-align: center;">Falling</th> <th style="text-align: center;">Rising/ Falling</th> <th style="text-align: center;">H level</th> <th style="text-align: center;">L level</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">INT4</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">disable</td> <td style="text-align: center;">disable</td> </tr> <tr> <td style="text-align: center;">INT5</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">disable</td> <td style="text-align: center;">disable</td> </tr> <tr> <td style="text-align: center;">INT6</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">disable</td> <td style="text-align: center;">disable</td> </tr> <tr> <td style="text-align: center;">INT7</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">enable</td> <td style="text-align: center;">disable</td> <td style="text-align: center;">disable</td> </tr> </tbody> </table> | | Rising | Falling | Rising/ Falling | H level | L level | INT4 | enable | enable | enable | disable | disable | INT5 | enable | enable | enable | disable | disable | INT6 | enable | enable | enable | disable | disable | INT7 | enable | enable | enable | disable | disable | Yes |
| | Rising | Falling | Rising/ Falling | H level | L level | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT4 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT5 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT6 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT7 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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| Pin Name | I/O | Description | Option | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|--------|---|--------------------|---------|---------|--------------------|---------|---------|------|--------|--------|---------|--------|--------|------|--------|--------|---------|--------|--------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|----|
| Port 7 P70 to P73 | I/O | <ul style="list-style-type: none"> • 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Shared Pins P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output P71: INT1 input/HOLD reset input/timer 0H capture input P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/ high speed clock counter input P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input AD converter input port: AN8 (P70), AN9 (P71) <ul style="list-style-type: none"> • Interrupt acknowledge type <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising/ Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> | | Rising | Falling | Rising/ Falling | H level | L level | INT0 | enable | enable | disable | enable | enable | INT1 | enable | enable | disable | enable | enable | INT2 | enable | enable | enable | disable | disable | INT3 | enable | enable | enable | disable | disable | No |
| | Rising | Falling | Rising/ Falling | H level | L level | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT0 | enable | enable | disable | enable | enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT1 | enable | enable | disable | enable | enable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT2 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT3 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 8 P80 to P86 | I/O | <ul style="list-style-type: none"> • 7-bit I/O port • I/O specifiable in 1-bit units • Shared Pins AD converter input port : AN0 (P80) to AN6 (P86) | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PWM2 PWM3 | I/O | <ul style="list-style-type: none"> • PWM2 and PWM3 output ports • General-purpose I/O available | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 3 P30 to P37 | I/O | <ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions P32: UART1 transmit P33: UART1 receive P34: UART2 transmit P35: UART2 receive | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Port C PC0 to PC7 | I/O | <ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions DBG P0 to DBG P2(PC5 to PC7): On-chip Debugger | Yes | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{RES}}$ | Input | Reset pin | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| XT1 | Input | <ul style="list-style-type: none"> • 32.768kHz crystal oscillator input pin • Shared pins General-purpose input port AD converter input port : AN10 Must be connected to V_{DD1} if not to be used. | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| XT2 | I/O | <ul style="list-style-type: none"> • 32.768kHz crystal oscillator input pin • Shared pins General-purpose I/O port AD converter input port : AN11 Must be set for oscillation and kept open if not to be used. | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CF1 | Input | Ceramic resonator input pin | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CF2 | Output | Ceramic resonator output pin | No | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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Port Output Types

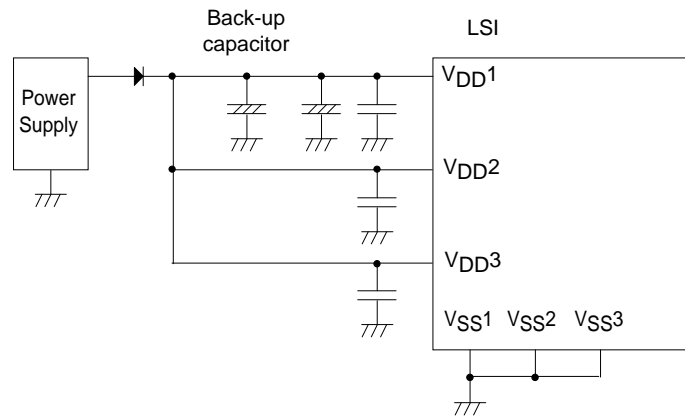
The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

| Port | Options Selected in Units of | Option Type | Output Type | Pull-up Resistor |
|------------|------------------------------|-------------|---|-----------------------|
| P00 to P07 | 1 bit | 1 | CMOS | Programmable (Note 1) |
| | | 2 | Nch-open drain | No |
| P10 to P17 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P20 to P27 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P30 to P37 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P70 | - | No | Nch-open drain | Programmable |
| P71 to P73 | - | No | CMOS | Programmable |
| P80 to P86 | - | No | Nch-open drain | No |
| PWM2, PWM3 | - | No | CMOS | No |
| PC0 to PC7 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| XT1 | - | No | Input for 32.768kHz crystal oscillator (Input only) | No |
| XT2 | - | No | Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode) | No |

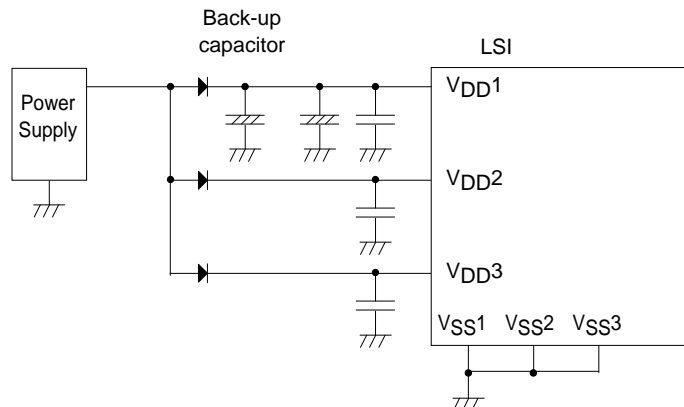
Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

*1: Make the following connection to minimize the noise input to the V_{DD1} pin and prolong the backup time. Be sure to electrically short the V_{SS1}, V_{SS2}, and V_{SS3} pins.

(Example 1) When backup is active in the HOLD mode, the high level of the port outputs is supplied by the backup capacitors.



(Example 2) The high-level output at the ports is unstable when the HOLD mode backup is in effect.



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Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|-------------------------------|-------------------------------|--|--|---|------|------|----------------------|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| Maximum supply voltage | V _{DD} max | V _{DD1} , V _{DD2} , V _{DD3} | V _{DD1} =V _{DD2} =V _{DD3} | | -0.3 | | +6.5 | V |
| Input voltage | V _I (1) | XT1, CF1 | | | -0.3 | | V _{DD} +0.3 | |
| Input/Output voltage | V _{IO} (1) | Ports 0, 1, 2 Ports 7, 8 Ports 3, C PWM0, PWM1, XT2 | | | -0.3 | | V _{DD} +0.3 | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1, 2 Ports 3, C | CMOS output select Per 1 application pin | | -10 | | mA |
| | | IOPH(2) | PWM2, PWM3 | Per 1 application pin. | | -20 | | |
| | | IOPH(3) | P71 to P73 | Per 1 application pin. | | -5 | | |
| | Mean output current (Note1-1) | IOMH(1) | Ports 0, 1, 2 Ports 3, C | CMOS output select Per 1 application pin | | -7.5 | | |
| | | IOMH(2) | PWM2, PWM3 | Per 1 application pin | | -10 | | |
| | | IOMH(3) | P71 to P73 | Per 1 application pin | | -3 | | |
| | Total output current | ΣIOAH(1) | P71 to P73 | Total of all applicable pins | | -10 | | |
| | | ΣIOAH(2) | Port 1 PWM2, PWM3 | Total of all applicable pins | | -25 | | |
| | | ΣIOAH(3) | Ports 0, 2 | Total of all applicable pins | | -25 | | |
| | | ΣIOAH(4) | Ports 0, 1, 2 PWM2, PWM3 | Total of all applicable pins | | -45 | | |
| | | ΣIOAH(5) | Port 3 | Total of all applicable pins | | -25 | | |
| | | ΣIOAH(6) | Port C | Total of all applicable pins | | -25 | | |
| | | ΣIOAH(7) | Ports 3, C | Total of all applicable pins | | -45 | | |
| Low level output current | Peak output current | IOPL(1) | P02 to P07 Ports 1, 2 Ports 3, C PWM2, PWM3 | Per 1 application pin. | | | 20 | |
| | | IOPL(2) | P00, P01 | Per 1 application pin. | | | 30 | |
| | | IOPL(3) | Ports 7, 8, XT2 | Per 1 application pin. | | | 10 | |
| | Mean output current (Note1-1) | IOML(1) | P02 to P07 Ports 1, 2 Ports 3, C PWM2, PWM3 | Per 1 application pin. | | | 15 | |
| | | IOML(2) | P00, P01 | Per 1 application pin. | | | 20 | |
| | | IOML(3) | Ports 7, 8, XT2 | Per 1 application pin. | | | 7.5 | |
| | Total output current | ΣIOAL(1) | Port 7 P83 to P86, XT2 | Total of all applicable pins | | | 15 | |
| | | ΣIOAL(2) | P80 to P82 | Total of all applicable pins | | | 15 | |
| | | ΣIOAL(3) | Ports 7, 8, XT2 | Total of all applicable pins | | | 20 | |
| | | ΣIOAL(4) | Port 1 PWM2, PWM3 | Total of all applicable pins | | | 45 | |
| | | ΣIOAL(5) | Ports 0, 2 | Total of all applicable pins | | | 45 | |
| | | ΣIOAL(6) | Ports 0, 1, 2 PWM2, PWM3 | Total of all applicable pins | | | 80 | |
| | | ΣIOAL(7) | Port 3 | Total of all applicable pins | | | 45 | |
| ΣIOAL(8) | | Port C | Total of all applicable pins | | | 45 | | |
| ΣIOAL(9) | Ports 3, C | Total of all applicable pins | | | 80 | | | |
| Power dissipation | Pd max | QIP64E(14×14) | Ta=-40 to +85°C | | | 300 | mW | |
| Operating ambient temperature | Topr | | | | -40 | | +85 | °C |
| Storage ambient temperature | Tstg | | | | -55 | | +125 | |

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Allowable Operating Conditions at Ta = -40°C to +85°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | unit |
|--|--|---|--|---------------------|----------------------------|----------------------------|-----------------------------|------|
| | | | | V _{DD} [V] | min | typ | max | |
| Operating supply voltage (Note2-1) | V _{DD} (1) | V _{DD1} =V _{DD2} =V _{DD3} | 0.245μs ≤ tCYC ≤ 200μs | | 2.8 | | 5.5 | V |
| | | | 0.367μs ≤ tCYC ≤ 200μs | | 2.5 | | 5.5 | |
| | | | 1.47μs ≤ tCYC ≤ 200μs | | 2.2 | | 5.5 | |
| Memory sustaining supply voltage | V _{HD} | V _{DD1} =V _{DD2} =V _{DD3} | RAM and register contents sustained in HOLD mode | | 2.0 | | 5.5 | |
| High level input voltage | V _{IH} (1) | Ports 1, 2 P71 to P73 P70 port input/ interrupt side | | 2.2 to 5.5 | 0.3V _{DD} +0.7 | | V _{DD} | V |
| | V _{IH} (2) | Ports 0, 8, 3, C PWM2, PWM3 | | 2.2 to 5.5 | 0.3V _{DD} +0.7 | | V _{DD} | |
| | V _{IH} (3) | Port P70 watchdog timer side | | 2.2 to 5.5 | 0.9V _{DD} | | V _{DD} | |
| | V _{IH} (4) | XT1, XT2, CF1, $\overline{\text{RES}}$ | | 2.2 to 5.5 | 0.75V _{DD} | | V _{DD} | |
| Low level input voltage | V _{IL} (1) | Ports 1, 2 P71 to P73 P70 port input/ Interrupt side | | 4.0 to 5.5 | V _{SS} | | 0.1V _{DD} +0.4 | μs |
| | | | | 2.2 to 4.0 | V _{SS} | | 0.2V _{DD} | |
| | V _{IL} (2) | Ports 0, 8, 3, C PWM2, PWM3 | | 4.0 to 5.5 | V _{SS} | | 0.15V _{DD} +0.4 | |
| | | | | 2.2 to 5.5 | V _{SS} | | 0.2V _{DD} | |
| V _{IL} (3) | Port 70 watchdog timer side | | 2.2 to 5.5 | V _{SS} | | 0.8V _{DD} -1.0 | | |
| V _{IL} (4) | XT1, XT2, CF1, $\overline{\text{RES}}$ | | 2.2 to 5.5 | V _{SS} | | 0.25V _{DD} | | |
| Instruction cycle time (Note2-2) | tCYC | | | 2.8 to 5.5 | 0.245 | | 200 | μs |
| | | | | 2.5 to 5.5 | 0.367 | | 200 | |
| | | | | 2.2 to 5.5 | 1.47 | | 200 | |
| External system clock frequency | FEXCF(1) | CF1 | <ul style="list-style-type: none"> • CF2 pin open • System clock frequency division rate=1/1 • External system clock duty=50±5% | 2.8 to 5.5 | 0.1 | | 12 | MHz |
| | | | | 2.5 to 5.5 | 0.1 | | 8 | |
| | | | | 2.2 to 5.5 | 0.1 | | 2 | |
| | | | <ul style="list-style-type: none"> • CF2 pin open • System clock frequency division rate=1/2 | 2.8 to 5.5 | 0.2 | | 24.4 | |
| | | | | 2.5 to 5.5 | 0.1 | | 16 | |
| | | | | 2.2 to 5.5 | 0.1 | | 4 | |
| Oscillation frequency range (Note2-3) | FmCF(1) | CF1, CF2 | 12MHz ceramic oscillation See Fig. 1. | 2.8 to 5.5 | | 12 | | MHz |
| | FmCF(2) | CF1, CF2 | 8MHz ceramic oscillation See Fig. 1. | 2.5 to 5.5 | | 8 | | |
| | FmCF(3) | CF1, CF2 | 4MHz ceramic oscillation See Fig. 1. | 2.2 to 5.5 | | 4 | | |
| | FmRC | | Internal RC oscillation | 2.2 to 5.5 | 0.3 | 1.0 | 2.0 | |
| | FmMRC | | Frequency variable RC oscillation source oscillation | 2.5 to 5.5 | | 16 | | |
| | FsX'tal | XT1, XT2 | 32.768kHz crystal oscillation See Fig. 2. | 2.2 to 5.5 | | 32.768 | | |

Note 2-1: V_{DD} must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

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Electrical Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | unit |
|---------------------------|---------------------|--|---|---------------|----------------------|--------------------|-----|------|
| | | | | VDD[V] | min | typ | max | |
| High level input current | I _{IH} (1) | Ports 0, 1, 2 Ports 7, 8 Ports 3, C $\overline{\text{RES}}$ PWM2, PWM3 | Output disabled Pull-up resistor off V _{IN} =V _{DD} (Including output Tr's off leakage current) | 2.2 to 5.5 | | | 1 | μA |
| | I _{IH} (2) | XT1, XT2 | For input port specification V _{IN} =V _{DD} | 2.2 to 5.5 | | | 1 | |
| | I _{IH} (3) | CF1 | V _{IN} =V _{DD} | 2.2 to 5.5 | | | 15 | |
| Low level input current | I _{IL} (1) | Ports 0, 1, 2 Ports 7, 8 Ports 3, C $\overline{\text{RES}}$ PWM2, PWM3 | Output disabled Pull-up resistor off V _{IN} =V _{SS} (Including output Tr's off leakage current) | 2.2 to 5.5 | -1 | | | μA |
| | I _{IL} (2) | XT1, XT2 | For input port specification V _{IN} =V _{SS} | 2.2 to 5.5 | -1 | | | |
| | I _{IL} (3) | CF1 | V _{IN} =V _{SS} | 2.2 to 5.5 | -15 | | | |
| High level output voltage | V _{OH} (1) | Ports 0, 1, 2 Ports 3, C | I _{OH} =-1mA | 4.5 to 5.5 | V _{DD} -1 | | | V |
| | V _{OH} (2) | | I _{OH} =-0.4mA | 3.0 to 5.5 | V _{DD} -0.4 | | | |
| | V _{OH} (3) | | I _{OH} =-0.2mA | 2.2 to 5.5 | V _{DD} -0.4 | | | |
| | V _{OH} (4) | Ports 71 to 73 | I _{OH} =-0.4mA | 3.0 to 5.5 | V _{DD} -0.4 | | | |
| | V _{OH} (5) | | I _{OH} =-0.2mA | 2.2 to 5.5 | V _{DD} -0.4 | | | |
| | V _{OH} (6) | PWM2, PWM3 | I _{OH} =-10mA | 4.5 to 5.5 | V _{DD} -1.5 | | | |
| | V _{OH} (7) | | I _{OH} =-1.6mA | 3.0 to 5.5 | V _{DD} -0.4 | | | |
| | V _{OH} (8) | | I _{OH} =-1mA | 2.2 to 5.5 | V _{DD} -0.4 | | | |
| Low level output voltage | V _{OL} (1) | Ports 0, 1, 2 Ports 3, C PWM2, PWM3, | I _{OL} =10mA | 4.5 to 5.5 | | | 1.5 | |
| | V _{OL} (2) | | I _{OL} =1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | V _{OL} (3) | | I _{OL} =1mA | 2.2 to 5.5 | | | 0.4 | |
| | V _{OL} (4) | Ports 7, 8 XT2 | I _{OL} =1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | V _{OL} (5) | | I _{OL} =1mA | 2.2 to 5.5 | | | 0.4 | |
| | V _{OL} (6) | P00, P01 | I _{OL} =30mA | 4.5 to 5.5 | | | 1.5 | |
| | V _{OL} (7) | | I _{OL} =5mA | 3.0 to 5.5 | | | 0.4 | |
| | V _{OL} (8) | | I _{OL} =2.5mA | 2.2 to 5.5 | | | 0.4 | |
| Pull-up resistance | R _{pu} (1) | Ports 0, 1, 2, 7 Ports 3, C | V _{OH} =0.9V _{DD} | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | R _{pu} (2) | | | 2.2 to 5.5 | 18 | 35 | 150 | |
| Hysteresis voltage | V _{HYS} | $\overline{\text{RES}}$ Ports 1, 2, 7 | | 2.2 to 5.5 | | 0.1V _{DD} | | V |
| Pin capacitance | CP | All pins | <ul style="list-style-type: none"> • For pins other than that under test: V_{IN}=V_{SS} • f=1MHz • Ta=25°C | 2.2 to 5.5 | | 10 | | pF |

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Serial I/O Characteristics at Ta = -40°C to +85°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

| Parameter | | Symbol | Pins /Remarks | Conditions | V _{DD} [V] | Specification | | | | |
|------------------------|-------------------|------------------------|------------------------|--|---|--------------------|-----------------------------|--------------------|------|--------------------|
| | | | | | | min | typ | max | unit | |
| Serial clock | Input clock | Frequency | tSCK(1) | SCK0(P12) | • See Fig. 6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(1) | | | | 1 | | | |
| | | High level pulse width | tSCKH(1) | | | | 1 | | | |
| | | | tSCKHA(1) | | | | | | | |
| | Output clock | Frequency | tSCK(2) | SCK0(P12) | • CMOS output selected • See Fig. 6. | 2.2 to 5.5 | 4/3 | | | tSCK |
| | | Low level pulse width | tSCKL(2) | | | | 1/2 | | | |
| High level pulse width | | tSCKH(2) | 1/2 | | | | | | | |
| | | tSCKHA(2) | | | | | | | | |
| | | | | • Continuous data transmission/reception mode • CMOS output selected • See Fig. 6. | | tSCKH(2) +2tCYC | tSCKH(2) +(10/3) tCYC | tCYC | | |
| Serial input | Data setup time | tsDI(1) | SB0(P11), SIO(P11) | • Must be specified with respect to rising edge of SIOCLK • See fig. 6. | 2.2 to 5.5 | 0.03 | | | | |
| | Data hold time | thDI(1) | | | | | 2.2 to 5.5 | 0.03 | | |
| Serial output | Output delay time | tdD0(1) | SO0(P10), SB0(P11), | • Continuous data transmission/reception mode • (Note 4-1-3) | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | μs | |
| | | | | • Synchronous 8-bit mode • (Note 4-1-3) | | 2.2 to 5.5 | | | | 1tCYC +0.05 |
| | | | | • (Note 4-1-3) | | 2.2 to 5.5 | | | | (1/3)tCYC +0.15 |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

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2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter | | Symbol | Pins/ Remarks | Conditions | V _{DD} [V] | Specification | | | | |
|---------------|-------------------|------------------------|-----------------------|---|--|---------------|-----|--------------------|------|------|
| | | | | | | min | typ | max | unit | |
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | • See Fig. 6. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • CMOS output selected. • See Fig. 6. | 2.2 to 5.5 | 2 | | | tSCK |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | tsDI(2) | SB1(P14) SI1(P14), | • Must be specified with respect to rising edge of SIOCLK • See fig. 6. | 2.2 to 5.5 | 0.03 | | | μs | |
| | Data hold time | thDI(2) | | | | 0.03 | | | | |
| Serial output | Output delay time | tdD0(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6. | 2.2 to 5.5 | | | (1/3)tCYC +0.05 | μs | |

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

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Pulse Input Conditions at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|----------------------------|--------------------|---|---|---------------------|-----|-----|-----|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| High/low level pulse width | tPIH(1) tPIL(1) | INT0(P70), INT1(P71), INT2(P72) INT4(P20 to P23), INT5(P24 to P27), INT6(P20) INT7(P24) | <ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 or 1 are enabled. | 2.2 to 5.5 | 1 | | | tCYC |
| | tPIH(2) tPIL(2) | INT3(P73) when noise filter time constant is 1/1. | <ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 2 | | | |
| | tPIH(3) tPIL(3) | INT3(P73) when noise filter time constant is 1/32 | <ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 64 | | | |
| | tPIH(4) tPIL(4) | INT3(P73) when noise filter time constant is 1/128 | <ul style="list-style-type: none"> Interrupt source flag can be set. Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 256 | | | |
| | tPIL(5) | $\overline{\text{RES}}$ | Resetting is enabled. | 2.2 to 5.5 | 200 | | | |

AD Converter Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|----------------------------|-------------------|---|---|-----------------------------|-----------------------------|----------------------------|----------------------------|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| Resolution | N | AN0(P80) to | | 3.0 to 5.5 | | 8 | | bit |
| Absolute accuracy | ET | AN6(P86), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2), | (Note 6-1) | 3.0 to 5.5 | | | ±1.5 | LSB |
| Conversion time | TCAD | | AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2) | 4.5 to 5.5 | 11.74 (tCYC= 0.367μs) | | 97.92 (tCYC= 3.06μs) | μs |
| | | | | 3.0 to 5.5 | 23.53 (tCYC= 0.735μs) | | 97.92 (tCYC= 3.06μs) | |
| | | | 4.5 to 5.5 | 15.68 (tCYC= 0.245μs) | | 97.92 (tCYC= 1.53μs) | | |
| | | | | | | | 3.0 to 5.5 | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | V _{SS} | | V _{DD} | V |
| Analog port input current | I _{AINH} | | V _{AIN} =V _{DD} | 3.0 to 5.5 | | | 1 | μA |
| | I _{AINL} | | V _{AIN} =V _{SS} | 3.0 to 5.5 | -1 | | | |

Note 6-1: The quantization error (±1/2 LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

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Consumption Current Characteristics at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = 0V

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|--|--|------------------------|--|---------------|------|-----|------|------|
| | | | | VDD[V] | min | typ | max | unit |
| Normal mode consumption current (Note 7-1) | IDDOP(1) | VDD1 =VDD2 =VDD3 | <ul style="list-style-type: none"> FmCF=12MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 12MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | 4.5 to 5.5 | | 9.1 | 18.5 | mA |
| | | | <ul style="list-style-type: none"> System clock set to 12MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | 2.8 to 4.5 | | 5.3 | 13.5 | |
| | <ul style="list-style-type: none"> FmCF=8MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 8MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | | 4.5 to 5.5 | | 6.7 | 14 | | |
| | <ul style="list-style-type: none"> System clock set to 8MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | | 2.5 to 4.5 | | 3.8 | 10 | | |
| | <ul style="list-style-type: none"> FmCF=4MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 4MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | | 4.5 to 5.5 | | 2.7 | 6 | | |
| | <ul style="list-style-type: none"> System clock set to 4MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | | 2.2 to 4.5 | | 1.45 | 3.8 | | |
| | <ul style="list-style-type: none"> FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode System clock set to internal RC oscillation frequency variable RC oscillation stopped 1/2 frequency division ratio. | | 4.5 to 5.5 | | 0.95 | 4.3 | | |
| | <ul style="list-style-type: none"> System clock set to internal RC oscillation frequency variable RC oscillation stopped 1/2 frequency division ratio. | | 2.2 to 4.5 | | 0.53 | 3.0 | | |
| | <ul style="list-style-type: none"> FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode. System clock set to 1MHz with frequency variable RC oscillation Internal RC oscillation stopped 1/2 frequency division ratio. | | 4.5 to 5.5 | | 1.25 | 5.2 | | |
| | <ul style="list-style-type: none"> System clock set to 1MHz with frequency variable RC oscillation Internal RC oscillation stopped 1/2 frequency division ratio. | | 2.2 to 4.5 | | 0.67 | 4.2 | | |
| | <ul style="list-style-type: none"> FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz by crystal oscillation mode. System clock set to 32.768kHz side. Internal RC oscillation stopped frequency variable RC oscillation stopped 1/2 frequency division ratio. | | 4.5 to 5.5 | | 38 | 112 | μA | |
| <ul style="list-style-type: none"> System clock set to 32.768kHz side. Internal RC oscillation stopped frequency variable RC oscillation stopped 1/2 frequency division ratio. | 2.2 to 4.5 | | 19 | 72 | | | | |
| HALT mode consumption current (Note 7-1) | IDDHALT(1) | VDD1 =VDD2 =VDD3 | <ul style="list-style-type: none"> HALT mode FmCF=12MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 12MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | 4.5 to 5.5 | | 3.2 | 7.5 | mA |
| | | | <ul style="list-style-type: none"> System clock set to 12MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | 2.8 to 5.5 | | 1.8 | 4 | |
| | <ul style="list-style-type: none"> HALT mode FmCF=8MHz ceramic oscillation mode FmX'tal=32.768kHz by crystal oscillation mode System clock set to 8MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | | 4.5 to 5.5 | | 2.4 | 5.3 | | |
| IDDHALT(2) | <ul style="list-style-type: none"> System clock set to 8MHz side Internal RC oscillation stopped frequency variable RC oscillation stopped 1/1 frequency division ratio. | 2.5 to 4.5 | | 12.5 | 2.8 | | | |
| IDDHALT(3) | | | | | | | | |

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

Continued on next page.

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Continued from preceding page.

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|--|--|--|--|---------------------|-----|-------|-----|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| HALT mode consumption current (Note 7-1) | IDDHALT(4) | V _{DD1} =V _{DD2} =V _{DD3} | <ul style="list-style-type: none"> • HALT mode • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode | 4.5 to 5.5 | | 1 | 2.3 | mA |
| | IDDHALT(5) | | <ul style="list-style-type: none"> • System clock set to 4MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio. | 2.2 to 4.5 | | 0.5 | 1.3 | |
| | IDDHALT(6) | | <ul style="list-style-type: none"> • HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode | 4.5 to 5.5 | | 0.33 | 0.9 | |
| | IDDHALT(7) | | <ul style="list-style-type: none"> • System clock set to internal RC oscillation • frequency variable RC oscillation stopped • 1/2 frequency division ratio. | 2.2 to 4.5 | | 0.17 | 0.7 | |
| | IDDHALT(8) | | <ul style="list-style-type: none"> • HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode. | 4.5 to 5.5 | | 1 | 3.8 | |
| | IDDHALT(9) | | <ul style="list-style-type: none"> • System clock set to 1MHz with frequency variable RC oscillation • Internal RC oscillation stopped • 1/2 frequency division ratio. | 2.2 to 4.5 | | 0.5 | 2.7 | |
| | IDDHALT(10) | | <ul style="list-style-type: none"> • HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode. | 4.5 to 5.5 | | 18 | 73 | μA |
| IDDHALT(11) | <ul style="list-style-type: none"> • System clock set to 32.768kHz side. • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio. | 2.2 to 4.5 | | 5 | 65 | | | |
| HOLD mode consumption current | IDDHOLD(1) | V _{DD1} | <ul style="list-style-type: none"> • HOLD mode • CF1=V_{DD} or open (External clock mode) | 4.5 to 5.5 | | 0.035 | 20 | μA |
| | IDDHOLD(2) | | <ul style="list-style-type: none"> • Timer HOLD mode • CF1=V_{DD} or open (External clock mode) | 2.2 to 4.5 | | 0.015 | 16 | |
| Timer HOLD mode consumption current | IDDHOLD(3) | | <ul style="list-style-type: none"> • FmX'tal=32.768kHz by crystal oscillation mode | 4.5 to 5.5 | | 16 | 65 | |
| | IDDHOLD(4) | | <ul style="list-style-type: none"> • FmX'tal=32.768kHz by crystal oscillation mode | 2.2 to 4.5 | | 3.5 | 52 | |

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

F-ROM Programming Characteristics at Ta = +10°C to +55°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|-----------------------------|----------|------------------|---|---------------------|-----|-----|-----|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| Onboard programming current | IDDFW(1) | V _{DD1} | <ul style="list-style-type: none"> • Without CPU current | 2.70 to 5.5 | | 5 | 10 | mA |
| Programming time | tFW(1) | | <ul style="list-style-type: none"> • Erasing | 2.7 to 5.5 | | 20 | 30 | ms |
| | tFW(2) | | <ul style="list-style-type: none"> • programming | 2.7 to 5.5 | | 40 | 60 | μs |

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UART (Full Duplex) Operating Conditions at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

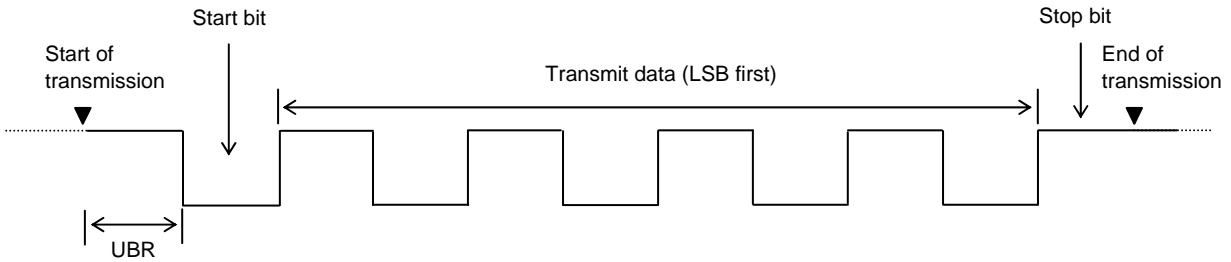
| Parameter | Symbol | Pins/Remarks | Conditions | Specification | | | | |
|---------------|--------|---|------------|--------------------|------|-----|--------|------|
| | | | | $V_{DD}[\text{V}]$ | min | typ | max | unit |
| Transfer rate | UBR | P32 (UTX1), P33 (URX1), P34 (UTX2), P35 (URX2) | | 2.5 to 5.5 | 16/3 | | 8192/3 | tCYC |

Data length : 7/8/9 bits (LSB first)

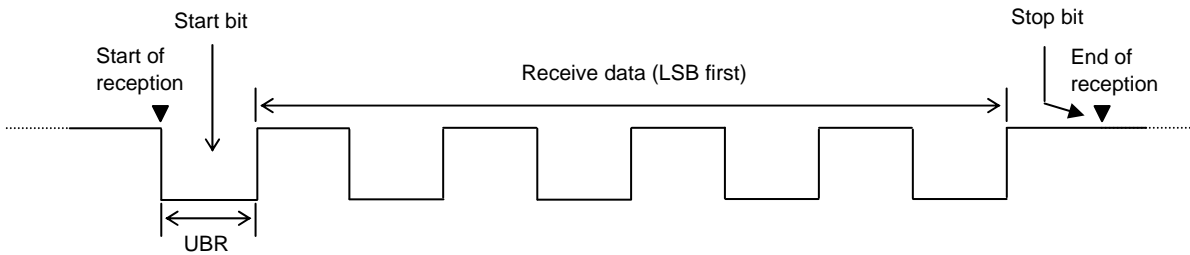
Stop bits : 1-bit (2-bit in continuous data transmission)

Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



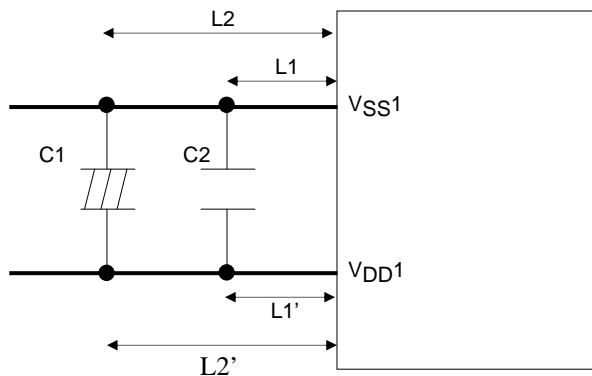
Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



VDD1, VSS1 Terminal Condition

It is necessary to place capacitors between V_{DD1} and V_{SS1} as describe below.

- Place capacitors as close to V_{DD1} and V_{SS1} as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal ($L1 = L1'$, $L2 = L2'$).
- Place high capacitance capacitor $C1$ and low capacitance capacitor $C2$ in parallel.
- Capacitance of $C2$ must be more than $0.1\mu\text{F}$.
- Use thicker pattern for V_{DD1} and V_{SS1} .



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|-------------------|-------------|-----------------|------------------|---------|---------|---------|-----------------------------|--------------------------------|----------|----------------|
| | | | C1 [pF] | C2 [pF] | Rf1 [Ω] | Rd1 [Ω] | | typ [ms] | max [ms] | |
| 12MHz | MURATA | CSTCE12M0G52-R0 | (10) | (10) | Open | 470 | 2.6 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| 10MHz | | CSTCE10M0G52-R0 | (10) | (10) | Open | 470 | 2.4 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| | | CSTLS10M0G53-B0 | (15) | (15) | Open | 680 | 2.6 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| 8MHz | | CSTCE8M00G52-R0 | (10) | (10) | Open | 680 | 2.3 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| | | CSTLS8M00G53-B0 | (15) | (15) | Open | 1k | 2.5 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| 4MHz | | CSTCR4M00G53-R0 | (15) | (15) | Open | 1.5k | 2.2 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |
| | | CSTLS4M00G53-B0 | (15) | (15) | Open | 1.5k | 2.2 to 5.5 | 0.03 | 0.5 | Internal C1,C2 |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Fig. 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

| Nominal Frequency | Vendor Name | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|-------------------|---------------|-----------------|------------------|---------|---------|---------|-----------------------------|--------------------------------|---------|-------------------------------|
| | | | C3 [pF] | C4 [pF] | Rf2 [Ω] | Rd2 [Ω] | | typ [s] | max [s] | |
| 32.768kHz | SEIKO TOYOCOM | MC-306 | 18 | 18 | Open | 560k | 2.2 to 5.5 | 1.2 | 3.0 | Applicable CL value=12.5pF |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure. 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

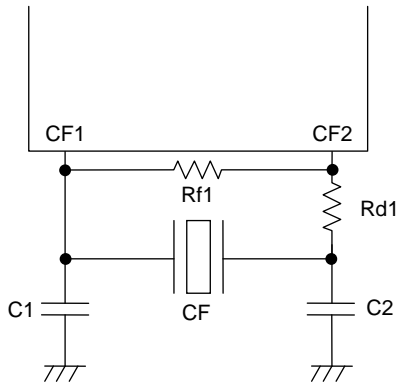


Figure 1 CF Oscillator Circuit

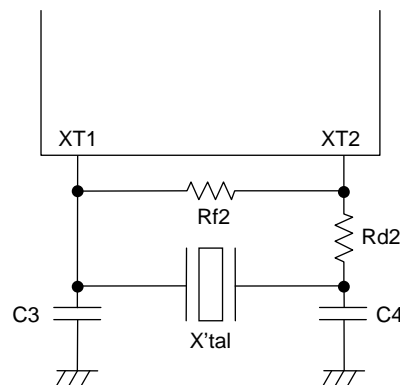


Figure 2 XT Oscillator Circuit

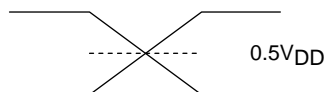
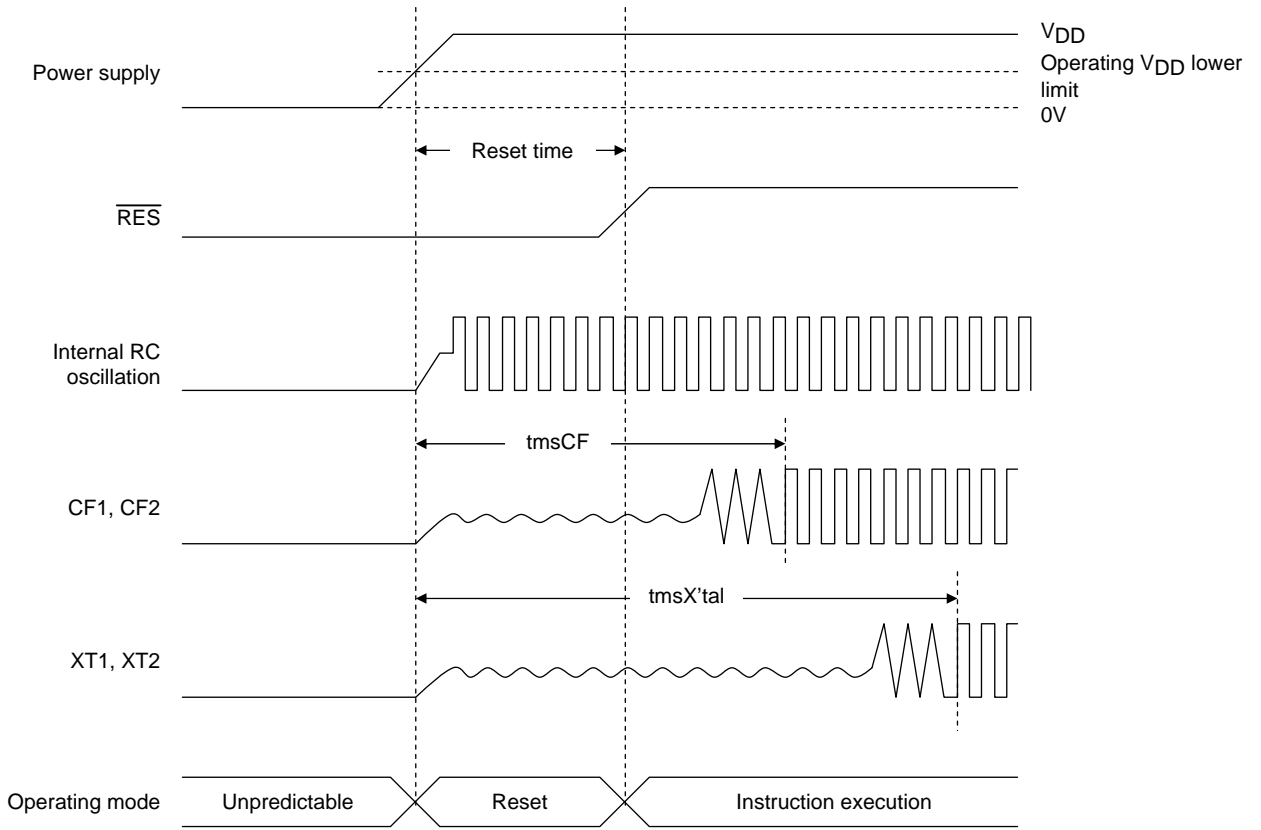
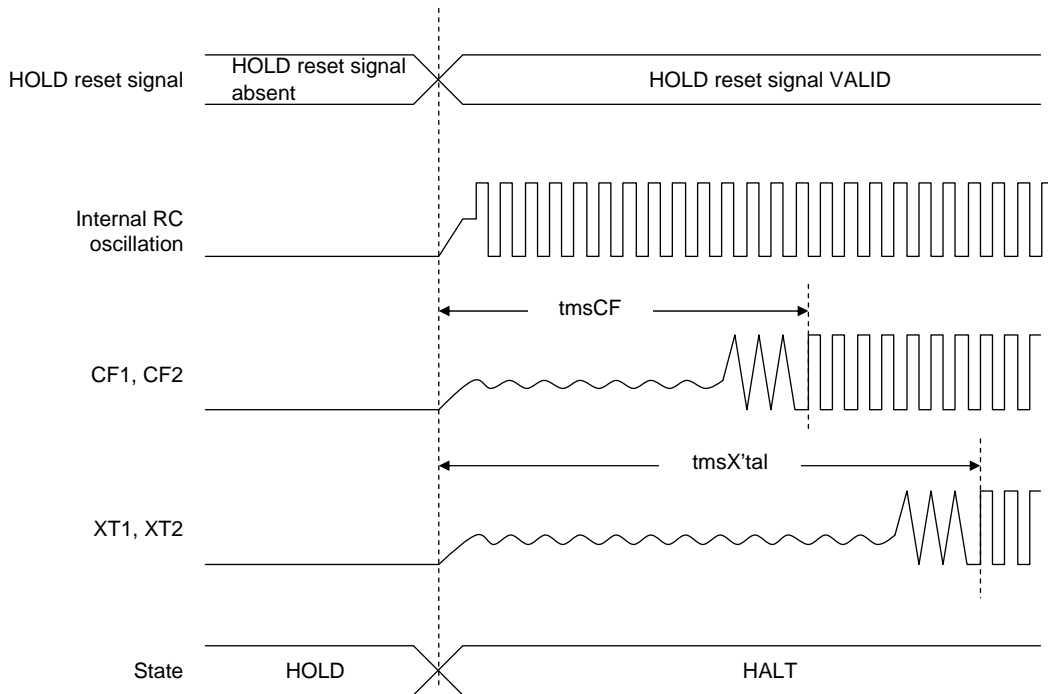


Figure 3 AC Timing Measurement Point

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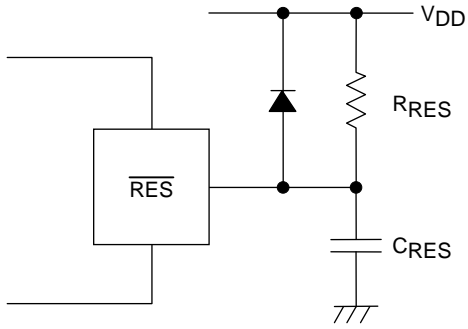


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200 μ s after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

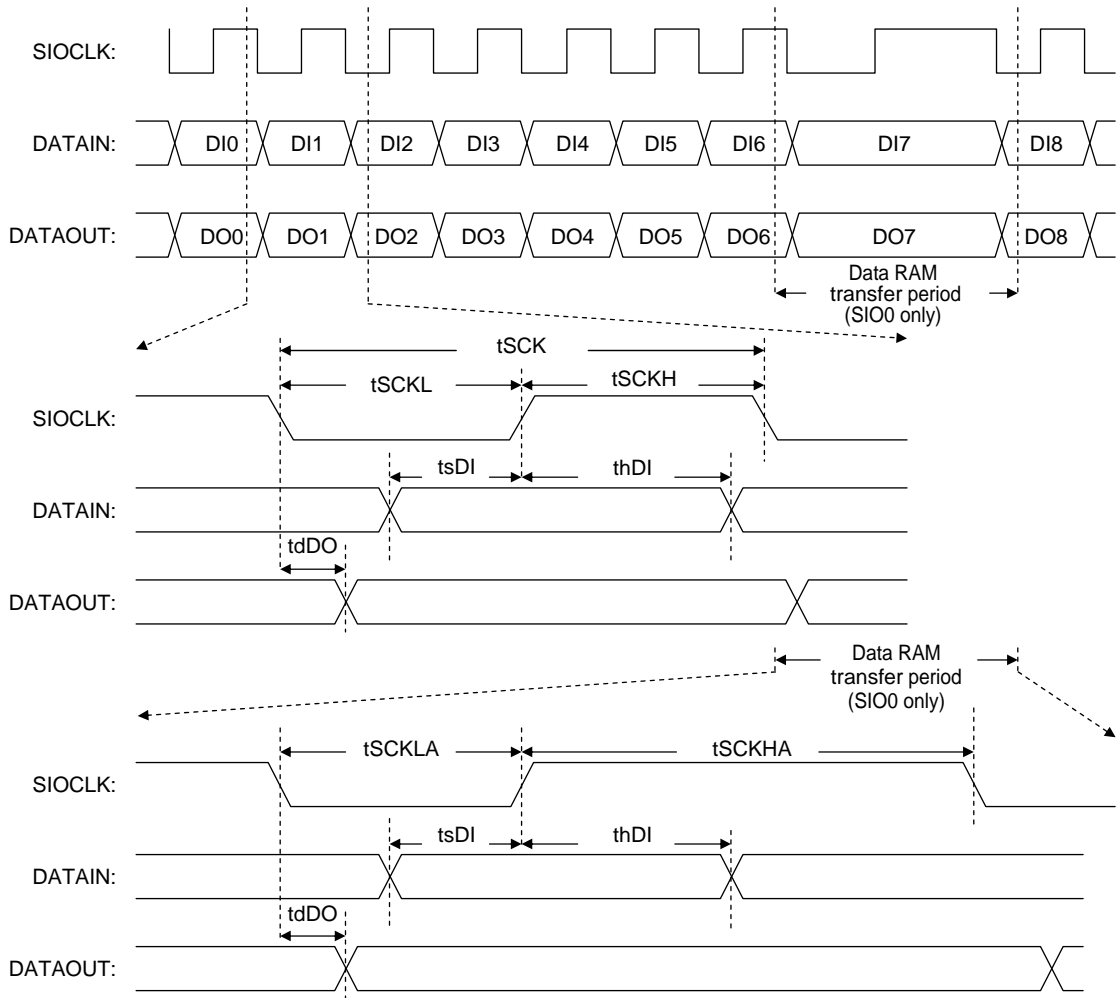


Figure 6 Serial I/O Waveforms

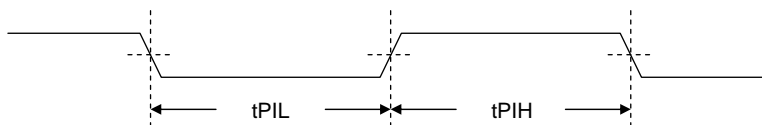


Figure 7 Pulse Input Timing Signal Waveform

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