IFX25401

Low Dropout Linear Voltage Regulator

IFX25401TBV
IFX25401TEV
IFX25401TBV50
IFX25401TEV50

Data Sheet

Rev. 1.02, 2012-08-24

Standard Power

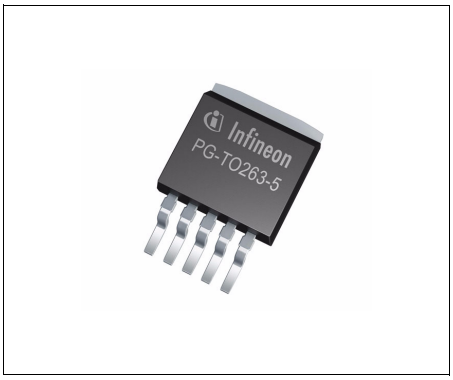
Low Dropout Linear Voltage Regulator

IFX25401

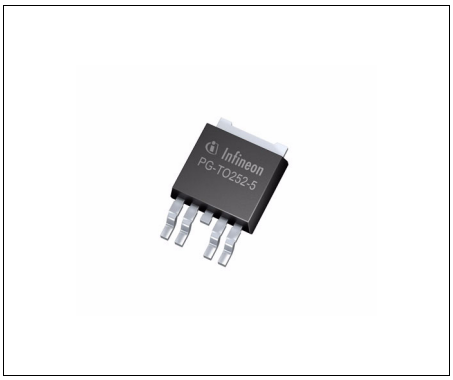
RoHS

Features

- Output Voltage Versions: 5V and Adjustable
- Very Low Current Consumption
- 400 mA Output Current Capability
- Enable Input
- Very Low Dropout Voltage
- Output Current Limitation
- Overtemperature Shutdown
- Reverse Polarity Protection
- Wide Temperature Range; -40 °C to 125 °C
- Green Product (RoHS compliant)



PG-TO263-5



PG-TO252-5

Applications

- Manufacturing and Automation
- Medical Equipment
- Building Management
- Industrial White Goods
- Security Systems

IFX25401 is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications. For automotive applications please refer to the Infineon TLx (TLE, TLS, TLF.....) voltage regulator products.

Description

The IFX25401 is a monolithic integrated low dropout voltage regulator for load currents up to 400 mA. An input voltage up to 40 V is regulated to an adjustable voltage with a precision of ±2%. The device is designed for harsh environments. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The adustable output can be configured to regulate between 2.5 V and 20 V.

Due to its very low quiescent current the IFX25401 is dedicated for use in applications permanently connected to a battery. In addition the device can be switched off via the Enable input which reduces the current consumption to less than 10 µA.

Type	Package	Marking
IFX25401TBV	PG-TO263-5	25401V
IFX25401TEV	PG-TO252-5	25401V
IFX25401TBV50	PG-TO263-5	25401V50
IFX25401TEV50	PG-TO252-5	2540150

1 Block Diagram

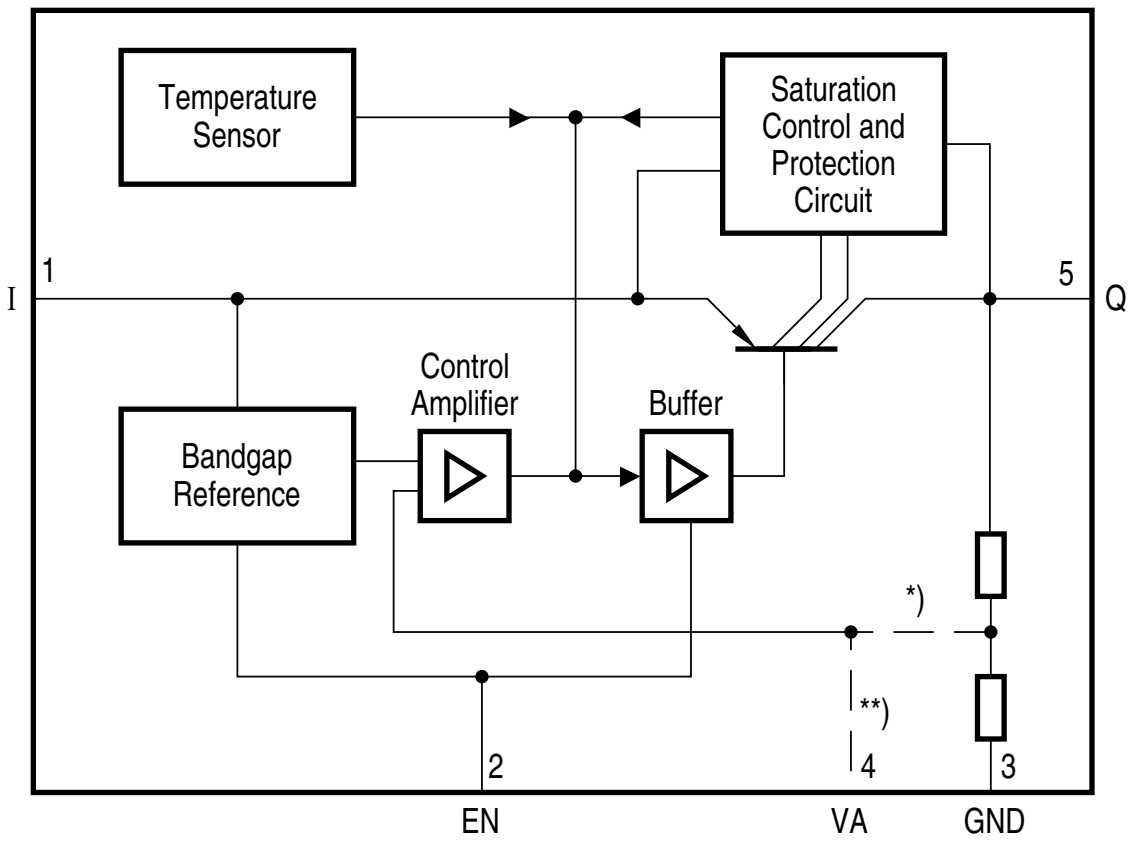


Figure 1 Block Diagram

2 Pin Configuration

2.1 Pin Assignment PG-TO263-5, PG-TO252-5

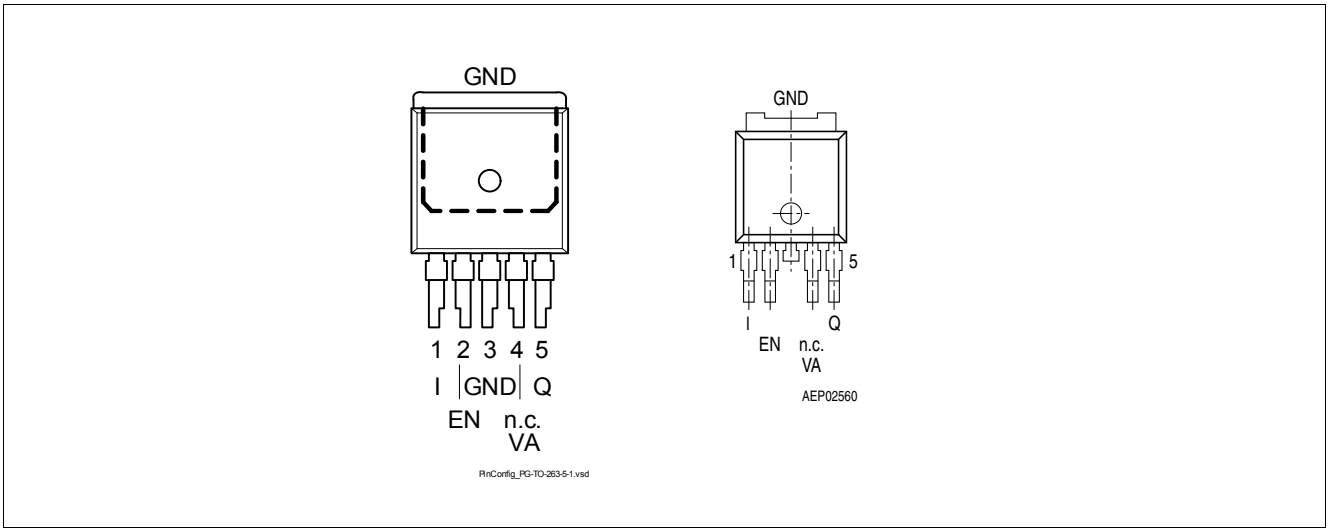


Figure 2 Pin Configuration (top view)

2.2 Pin Definitions and Functions PG-TO263-5, PG-TO252-5

Pin No.	Symbol	Function
1	I	**Input** block to ground directly at the IC with a ceramic capacitor
2	EN	**Enable** high level input signal enables the IC; low level input signal disables the IC; integrated pull-down resistor
3	GND	**Ground** internally connected to heat slug
4	N.C. VA	**Not Connected** for IFX25401TBV50, IFX25401TEV50 can be open or connected to GND **Voltage Adjust** for IFX25401TBV, IFX25401TEV connect external voltage divider to configure the output voltage
5	Q	**Output** Connect a capacitor between Q and GND close to the IC pins and respect the values specified for apacitance and ESR in **“Functional Range” on Page 6**
Heat Slug	–	**Heat Slug** internally connected to GND; connect to PCB/System GND and heatsink area

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]
T_j = -40 °C to 150 °C; all voltages with respect to ground, (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Condition
			Min.	Max.		
Input I						
3.1.1	Voltage	V_I	-42	45	V	–
Enable EN						
3.1.2	Voltage	V_{EN}	-42	45	V	–
Voltage Adjust Input VA						
3.1.3	Voltage	V_{VA}	-0.3	10	V	–
Output Q						
3.1.4	Voltage	V_Q	-1	40	V	–
Temperature						
3.1.5	Junction temperature	T_j	-40	150	°C	–
3.1.6	Storage temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
3.1.7	ESD Absorption	$V_{ESD,HBM}$	-2	2	kV	Human Body Model (HBM)[2)]
3.1.8		$V_{ESD,CDM}$	-500	500	V	Charge Device Model (CDM)[3)]
3.1.9			-750	750	V	Charge Device Model (CDM) at corner pins[3)]

1) not subject to production test, specified by design
2) ESD susceptibility Human Body Model “HBM” according to JESD22-A114
3) ESD susceptibility Charged Device Model “CDM” according to ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
3.2.10	Input voltage	V_I	V_Q + 0.5	40	V	IFX25401TBV, IFX25401TEV; IFX25401TBV50, IFX25401TEV50 V_Q > 4 V
3.2.11	Input voltage	V_I	4.5	40	V	IFX25401TBV, IFX25401TEV; V_Q < 4 V
3.2.12	Output Capacitor's Requirements for Stability	C_Q	22	–	µF	1)
3.2.13		$ESR(C_Q)$	–	3	Ω	2)
3.2.14	Junction temperature	T_j	-40	125	°C	–

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
IFX25401TBV, IFX25401TBV50 (PG-TO263-5)							
3.3.1	Junction to Case[1)]	R_{thJC}	–	4	–	K/W	measured to heat slug
3.3.2	Junction to Ambient[1)]	R_{thJA}	–	22	–	K/W	2)
3.3.3			–	74	–	K/W	footprint only[3)]
3.3.4			–	42	–	K/W	300 mm² heatsink area[3)]
3.3.5			–	34	–	K/W	600 mm² heatsink area[3)]
IFX25401TEV, IFX25401TEV50 (PG-TO252-5)							
3.3.6	Junction to Case[1)]	R_{thJC}	–	4	–	K/W	measured to heat slug
3.3.7	Junction to Ambient[1)]	R_{thJA}	–	27	–	K/W	2)
3.3.8			–	115	–	K/W	footprint only[3)]
3.3.9			–	52	–	K/W	300 mm² heatsink area[3)]
3.3.10			–	40	–	K/W	600 mm² heatsink area[3)]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

4 Electrical Characteristics

4.1 Electrical Characteristics Voltage Regulator

Electrical Characteristics
V_I=13.5 V; T_j = -40 °C to 125 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Measuring Condition
			Min.	Typ.	Max.		
Output Q							
4.1.1	Output Voltage Accuracy[1)]	ΔV_Q	-2	–	2	%	IFX25401TBV, IFX25401TEV R_2 < 50 kΩ; V_Q + 1 V ≤ V_I ≤ 40V; V_I > 4.5 V; 5 mA ≤ I_Q ≤ 400 mA
4.1.2	Output Voltage	V_Q	4.9	5.0	5.1	V	IFX25401TBV50 IFX25401TEV50 6 V ≤ V_I ≤ 28 V; 5 mA ≤ I_Q ≤ 400 mA
4.1.3	Output Voltage Adjustable Range[3)]	$V_{Q,range}$	2.5	–	20	V	IFX25401TBV, IFX25401TEV; Refer to **Page 13**
4.1.4	Dropout Voltage	V_{dr}	–	250	500	mV	I_Q = 250 mA V_I > 4.5 V; V_{dr} = V_I – V_Q[2)]
4.1.5	Load Regulation	$\Delta V_{Q, lo}$	–	5	35	mV	I_Q = 5 mA to 400 mA V_I = 4.5 V
4.1.6	Line Regulation	$\Delta V_{Q, li}$	–	15	25	mV	V_I = 12 V to 32 V I_Q = 5 mA
4.1.7	Output Current Limitation	I_Q	400	600	1100	mA	[2)]
4.1.8	Power Supply Ripple Rejection[3)]	$PSRR$	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
4.1.9	Temperature Output Voltage Drift[3)]	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–

Electrical Characteristics

V_I=13.5 V; T_j = -40 °C to 125 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Measuring Condition
			Min.	Typ.	Max.		
Current Consumption							
4.1.10	Current Consumption, Regulator Disabled	I_q	–	–	10	µA	V_{EN} = 0 V $T_j \leq$ 100 °C
4.1.11	Quiescent Current $I_q = I_I - I_Q$	I_q	–	100	220	µA	I_Q = 1 mA; V_{EN} = 5 V
4.1.12	Current Consumption $I_q = I_I - I_Q$	I_q	–	5	10	mA	I_Q = 250 mA; V_{EN} = 5 V
4.1.13	Current Consumption $I_q = I_I - I_Q$	I_q	–	15	25	mA	I_Q = 400 mA; V_{EN} = 5 V

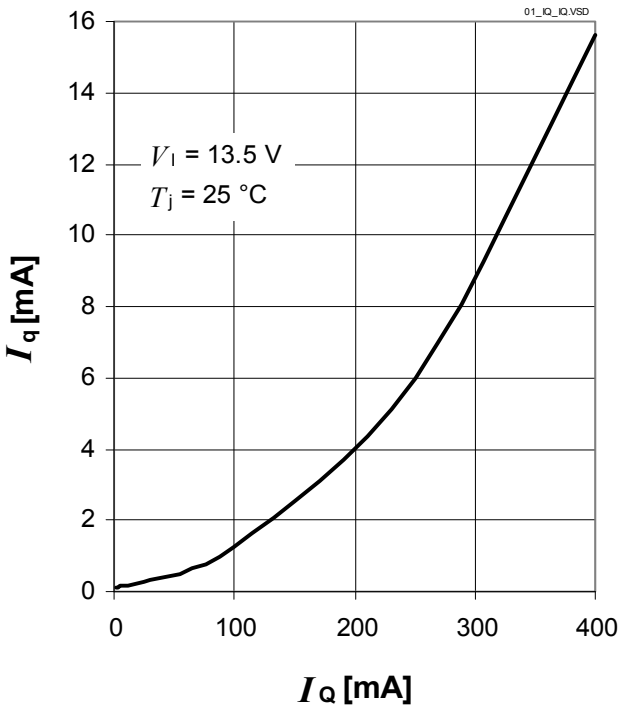
1) influence of resistor divider on accuracy neglected

2) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

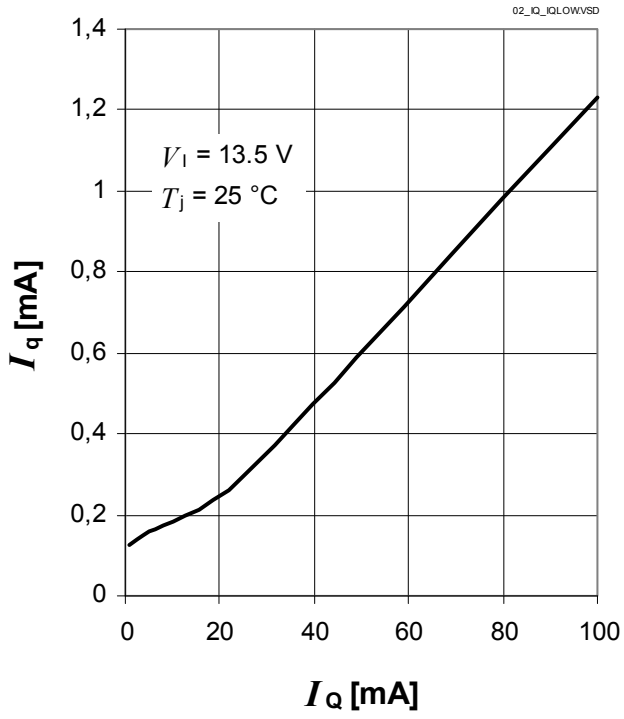
3) not subject to production test, specified by design

4.2 Typical Performance Characteristics Voltage Regulator

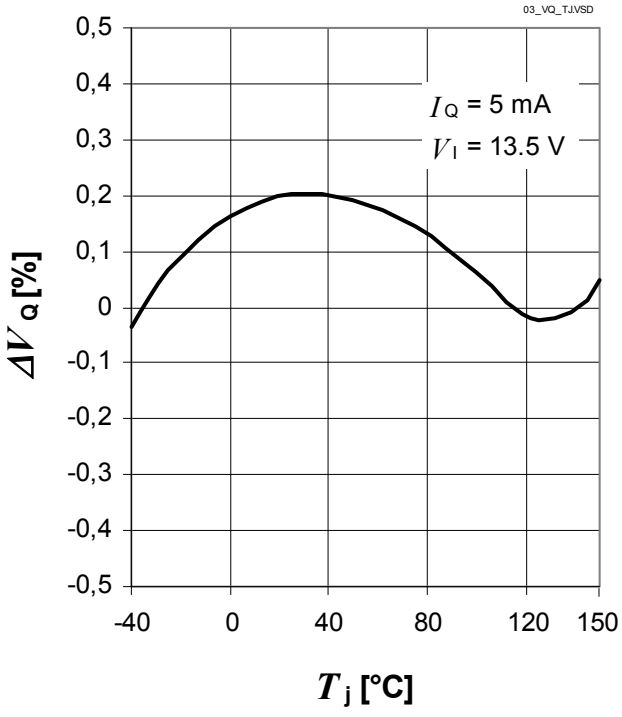
Current Consumption I_q versus Output Current I_Q



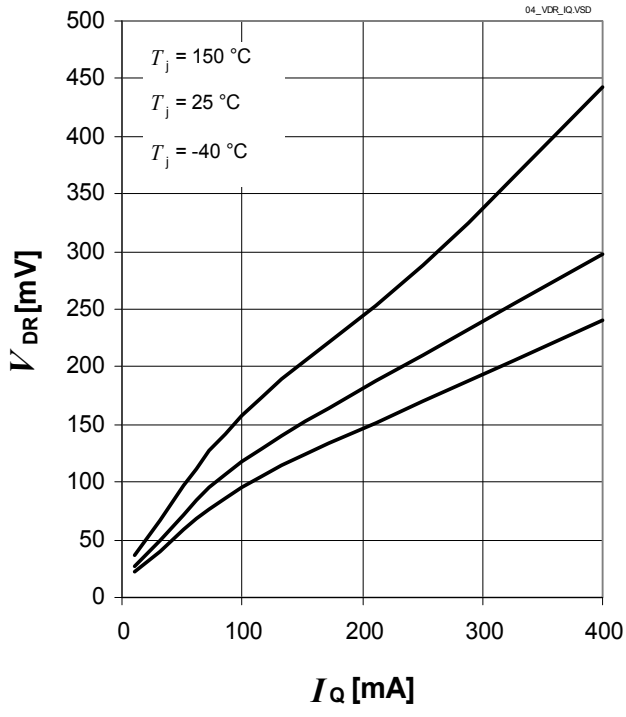
Current Consumption I_q versus Low Output Current I_Q



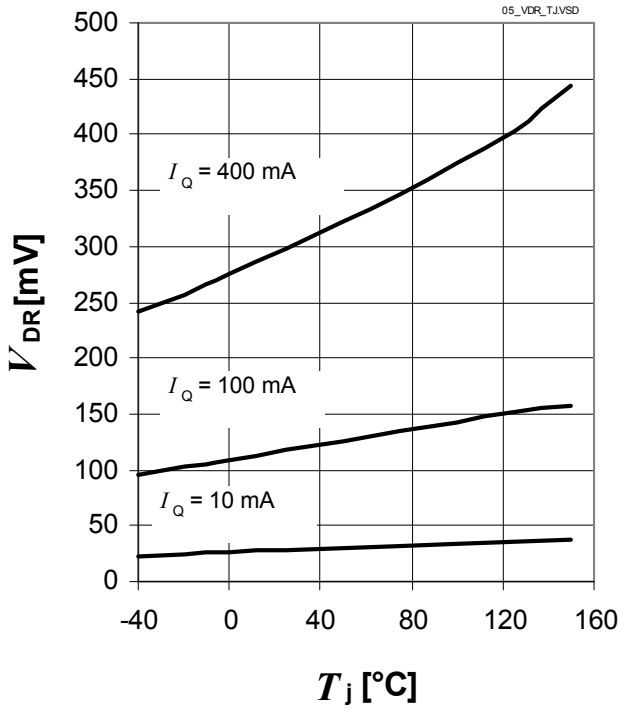
Output Voltage V_Q versus Junction Temperature T_J



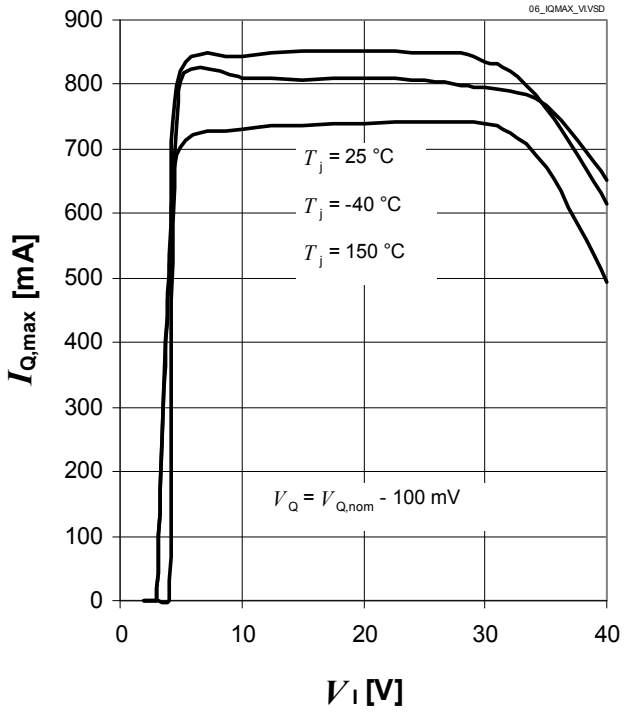
Dropout Voltage V_{dr} versus Output Current I_Q



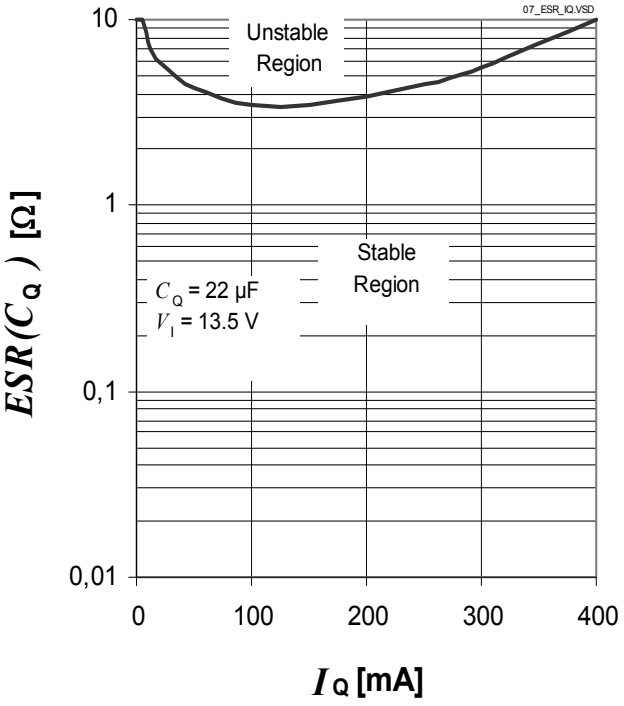
Dropout Voltage V_{dr} versus Junction Temperature



Maximum Output Current I_Q versus Input Voltage V_I



Region Of Stability: Output Capacitor's ESR $ESR(C_Q)$ versus Output Current I_Q



4.3 Electrical Characteristics Enable Function

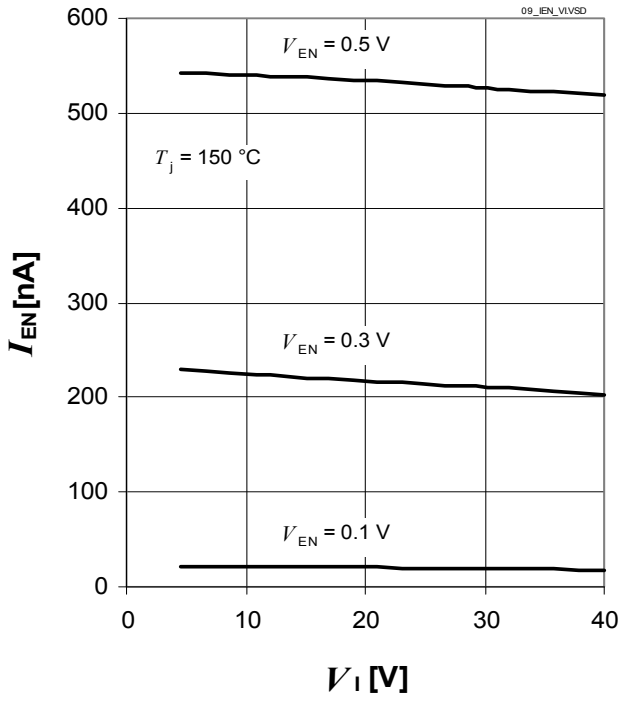
The Enable Function allows disabling/enabling the regulator via the input pin EN. The regulator is turned on in case the pin EN is connected to a voltage higher than $V_{EN,H}$. This can be e.g. the battery voltage, whereby no additional pull-up resistor is needed. The regulator can be turned off by connecting the pin EN to a voltage less than $V_{EN,L}$, e.g. GND.

Electrical Characteristics Enable
V_I=13.5 V; T_j = -40 °C to 125 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

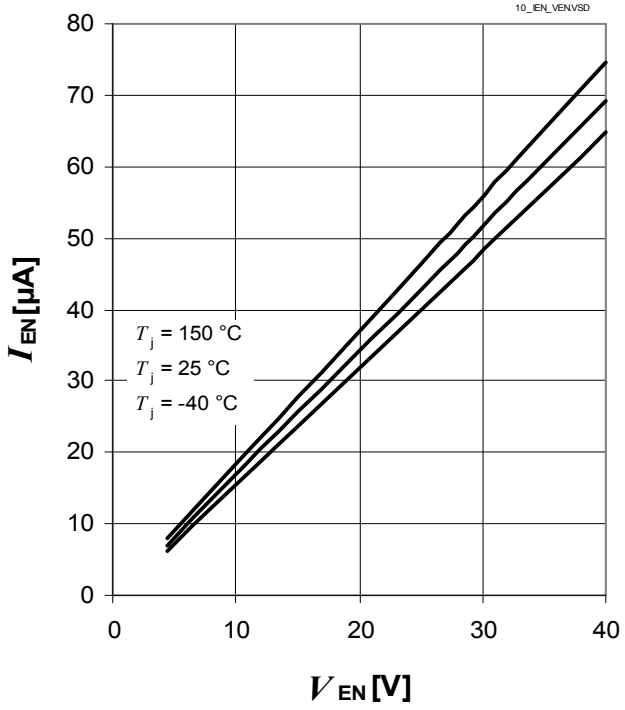
Pos.	Parameter	Symbol	Limit Values			Unit	Measuring Condition
			Min.	Typ.	Max.		
4.3.14	High Level Input Voltage	$V_{EN,H}$	3.5	–	–	V	$V_Q \geq$4.9 V
4.3.15	Low Level Input Voltage	$V_{EN,L}$	–	–	0.5	V	$V_Q \leq$0.1 V
4.3.16	High Level Input Current	$I_{EN,H}$	5	10	20	µA	V_{EN} = 5 V

4.4 Typical Performance Characteristics Enable Function

Enabled Input Current I_{EN} versus Input Voltage V_I, (Device OFF)



Enabled Input Current I_{EN} versus Enabled Input Voltage V_{EN} (Device ON)



5 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

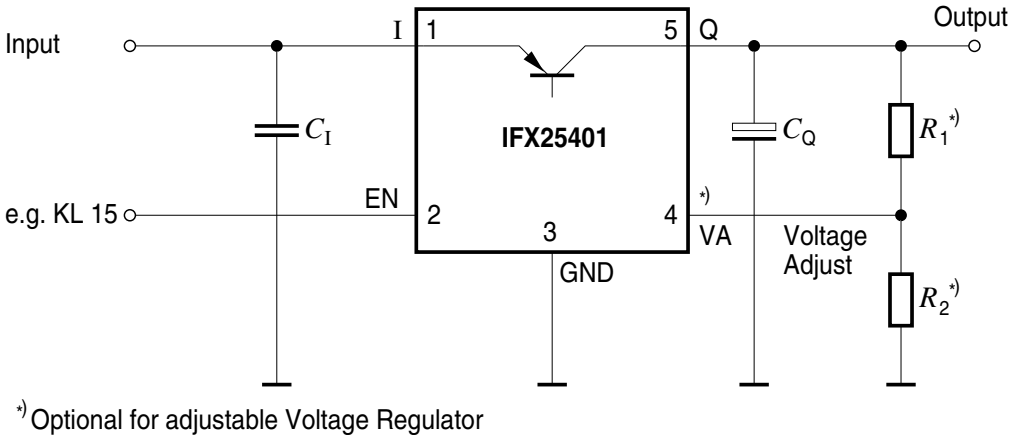


Figure 3 Application Diagram

A typical application circuit of the IFX25401 is shown in **Figure 3**. It shows a generic configuration of the voltage regulator with a recommended minimum number of components. The small input capacitor is not required but recommended for high frequency noise filtering. For a normal operation the fixed output voltage regulator only requires an output capacitor for stability. The adjustable output regulator requires an additional resistor network to configure the output voltage. Depending on the application conditons, additional components such as an input buffer capacitor or a reverse polarity protection diode can be considered as well.

Input Filter Capacitor

A small ceramic capacitor (e.g. 100nF in **Figure 3**) at the device's input helps filtering high frequency noise. To reach the best filter effect, this capacitor should be placed as close as possible to the device's input pin. The input filter capacitor does not have an influence on the stability of the device's regulation loop.

Output Capacitor C_Q

The output capacitor is the only external component that is required because it is part of the regulation loop. To maintain stability of this regulation loop, the IFX25401 requires an output capacitor respecting the values given in **"Functional Range" on Page 6**.

Adjusting the Output Voltage of Variable Output Regulators IFX25401TBV, IFX25401TEV

The output voltage of the IFX25401TBV and the IFX25401TEV can be adjusted between 2.5 V and 20 V by an external resistor divider connected to the voltage adjust pin VA.

The VA pin is connected to the internal error amplifier comparing the voltage at this pin with the internal reference voltage (i.e. 2.5 V).

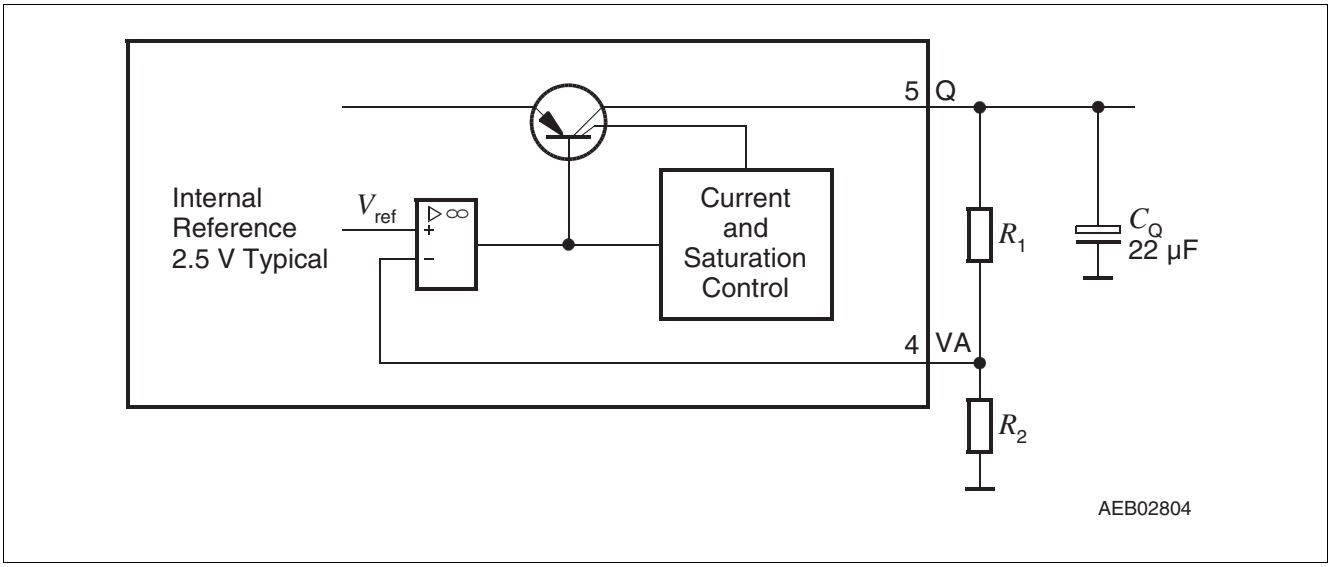


Figure 4 External Components at Output for Variable Voltage Regulator

The output voltage can be easily calculated, neglecting the current flowing into the VA pin:

$$V_Q = \frac{R_1 + R_2}{R_2} \times V_{ref}$$

where

$R_2 < 50\ k\Omega$ to neglect the current flowing into the VA pin,

with:

- V_{ref}: internal reference voltage, typically 2.5V
- R_1: resistor between regulator output Q and voltage adjust pin VA
- R_2: resistor between voltage adjust pin VA and GND

For a 2.5 V output voltage the output pin Q has to be directly connected to the adjust pin VA.

Take into consideration, that the accuracy of the resistors R_1 and R_2 adds an additional error to the output voltage tolerance.

6 Package Outlines

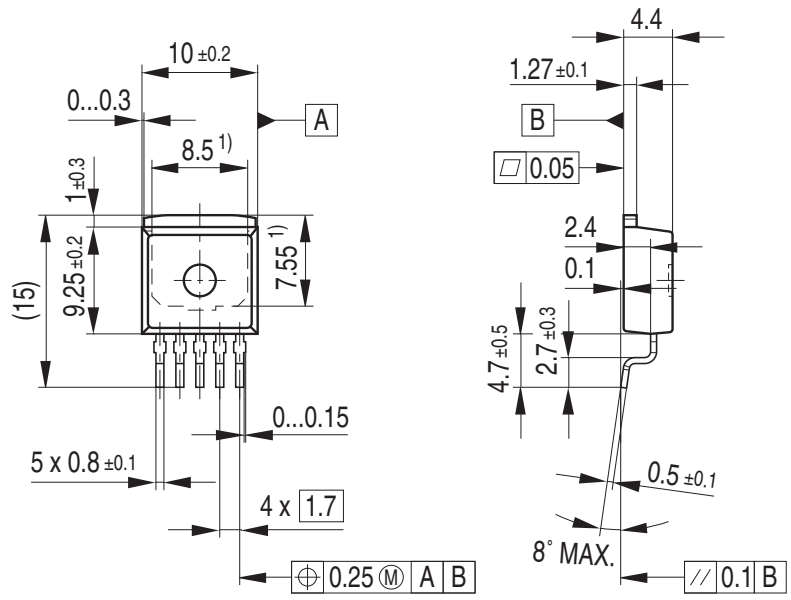
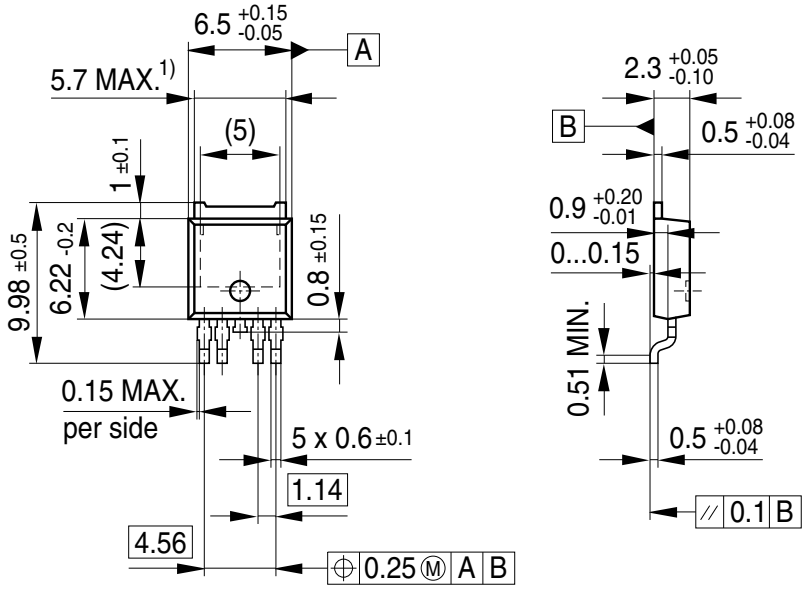


Figure 5 PG-TO263-5



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

Figure 6 PG-TO252-5

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

7 Revision History

Revision	Date	Changes
1.02	2012-08-24	Coverpage changed, Additional information about the ENABLE pin added, Disclaimer Updated
1.01	2009-10-19	Coverpage changed Overview page: Inserted reference statement to TLE/TLF series.
1.0	2009-04-28	Initial Release

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