

# MC74HC132A

## Quad 2-Input NAND Gate with Schmitt-Trigger Inputs

### High-Performance Silicon-Gate CMOS

The MC74HC132A is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

The HC132A can be used to enhance noise immunity or to square up slowly changing waveforms.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

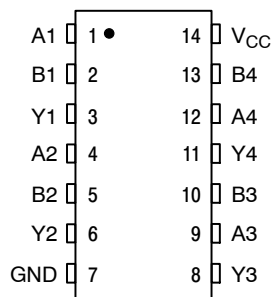


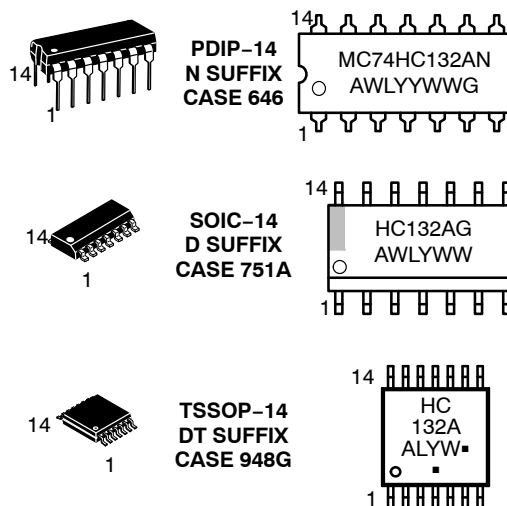
Figure 1. Pin Assignment



ON Semiconductor®

<http://onsemi.com>

#### MARKING DIAGRAMS



A = Assembly Location  
 L, WL = Wafer Lot  
 Y, YY = Year  
 W, WW = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## MC74HC132A

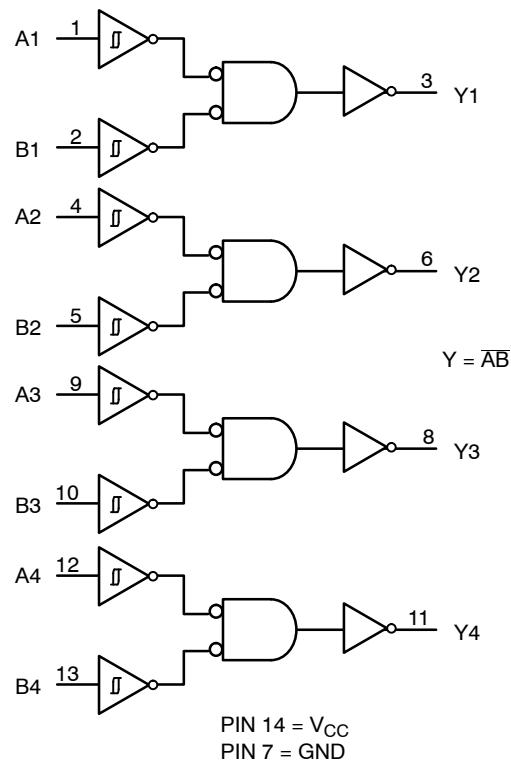


Figure 2. Logic Diagram

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74HC132ANG	PDIP-14 (Pb-Free)	25 / Tape & Ammo Box
MC74HC132ADG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74HC132ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74HC132ADTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74HC132ADTR2G	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC132ADG*	SOIC-14 (Pb-Free)	55 Units / Rail
NLV74HC132ADR2G*	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NLV74HC132ADTG*	TSSOP-14 (Pb-Free)	96 Units / Rail
NLV74HC132ADTR2G*	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

# MC74HC132A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage	- 0.5 to + 7.0	V
$V_{IN}$	Digital Input Voltage	- 0.5 to + 7.0	V
$V_{OUT}$	DC Output Voltage Output in 3-State High or Low State	- 0.5 to + 7.0 - 0.5 to $V_{CC}$ + 0.5	V
$I_{IK}$	Input Diode Current	- 20	mA
$I_{OK}$	Output Diode Current	± 20	mA
$I_{OUT}$	DC Output Current, per Pin	± 25	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	± 75	mA
$I_{GND}$	DC Ground Current per Ground Pin	± 75	mA
$T_{STG}$	Storage Temperature Range	- 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
$T_J$	Junction Temperature Under Bias	+ 150	°C
$\theta_{JA}$	Thermal Resistance 14-PDIP 14-SOIC 14-TSSOP	78 125 170	°C/W
$P_D$	Power Dissipation in Still Air at 85°C PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 30% - 35%	UL 94 V0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 100 > 500	V
$I_{Latch-Up}$	Latch-Up Performance Above $V_{CC}$ and Below GND at 85°C (Note 4)	± 300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 3)	-	No Limit (Note 5)	ns

5. When  $V_{IN} \sim 0.5 V_{CC}$ ,  $I_{CC} \gg$  quiescent current.
6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

# MC74HC132A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55°C to 25°C	≤ 85°C	≤ 125°C	
V <sub>T+</sub> max	Maximum Positive-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>T+</sub> min	Minimum Positive-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.0	0.95	0.95	V
			4.5	2.3	2.25	2.25	
			6.0	3.0	2.95	2.95	
V <sub>T-</sub> max	Maximum Negative-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.9	0.95	0.95	V
			4.5	2.0	2.05	2.05	
			6.0	2.6	2.65	2.65	
V <sub>T-</sub> min	Minimum Negative-Going Input Threshold Voltage (Figure 5)	V <sub>OUT</sub> = V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>H</sub> max (Note 7)	Maximum Hysteresis Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.2	1.2	1.2	V
			4.5	2.25	2.25	2.25	
			6.0	3.0	3.0	3.0	
V <sub>H</sub> min (Note 7)	Minimum Hysteresis Voltage (Figure 5)	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.2	0.2	0.2	V
			4.5	0.4	0.4	0.4	
			6.0	0.5	0.5	0.5	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> ≤ V <sub>T-</sub> min or V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>IN</sub> ≤ -V <sub>T-</sub> min or V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> ≥ V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>IN</sub> ≥ V <sub>T+</sub> max  I <sub>OUT</sub>   ≤ 4.0 mA  I <sub>OUT</sub>   ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0	1.0	10	40	μA

7. V<sub>H</sub>min > (V<sub>T+</sub>min) - (V<sub>T-</sub>max); V<sub>H</sub>max = (V<sub>T+</sub>max) + (V<sub>T-</sub>min).

# MC74HC132A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$-55^\circ\text{C}$ to $25^\circ\text{C}$	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 3 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF
$C_{PD}$	Power Dissipation Capacitance (per Gate) (Note 8)	Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$			pF	
		24				

8. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

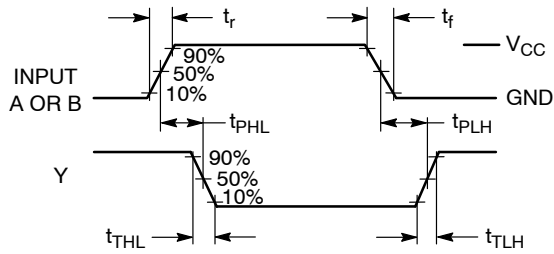
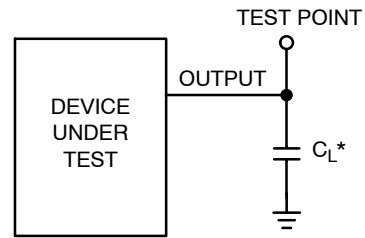


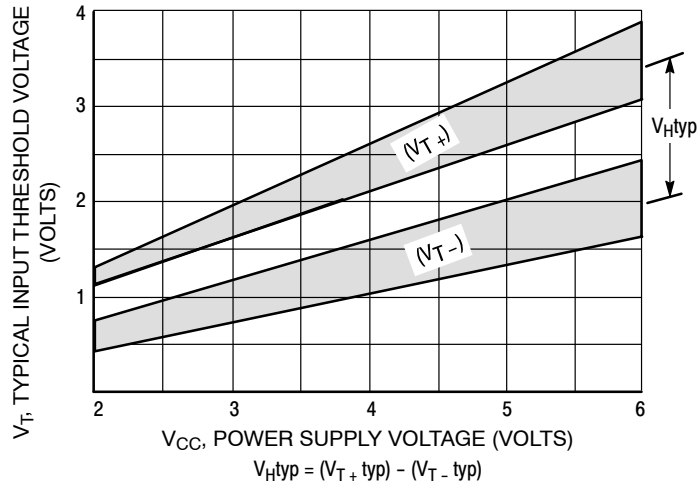
Figure 3. Switching Waveforms



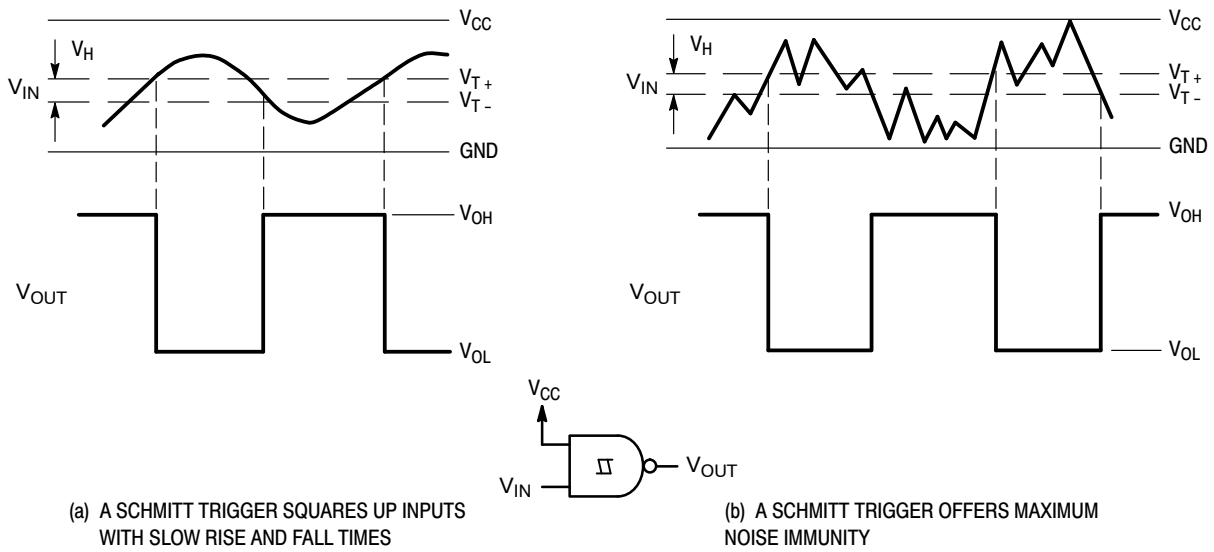
\*Includes all probe and jig capacitance

Figure 4. Test Circuit

# MC74HC132A



**Figure 5. Typical Input Threshold,  $V_{T+}$ ,  $V_{T-}$  Versus Power Supply Voltage**

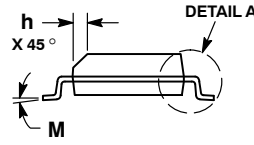
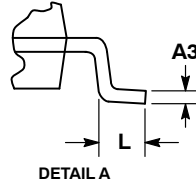
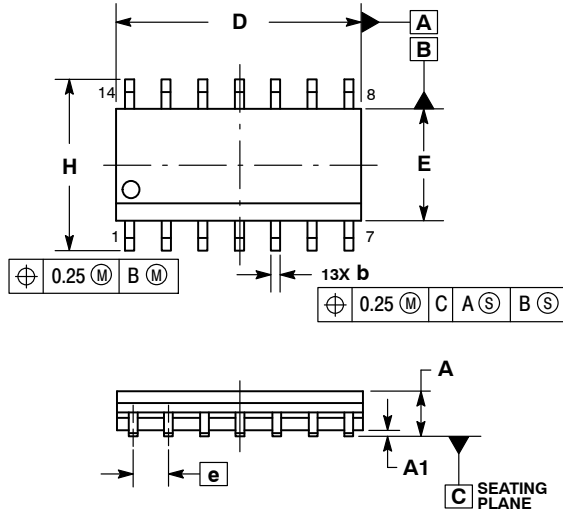


**Figure 6. Typical Schmitt-Trigger Applications**

# MC74HC132A

## PACKAGE DIMENSIONS

SOIC-14 NB  
CASE 751A-03  
ISSUE K

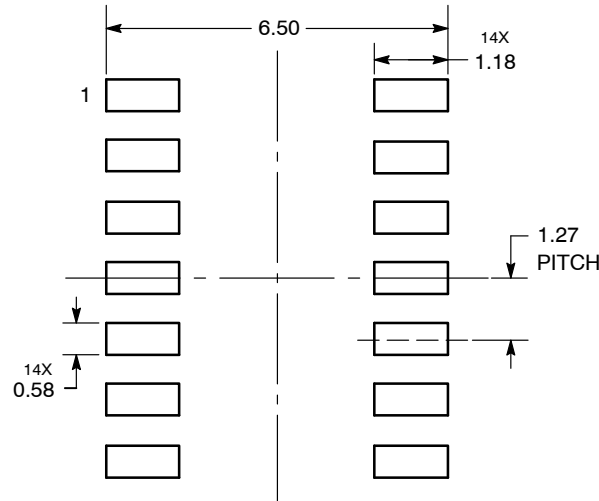


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

### SOLDERING FOOTPRINT\*



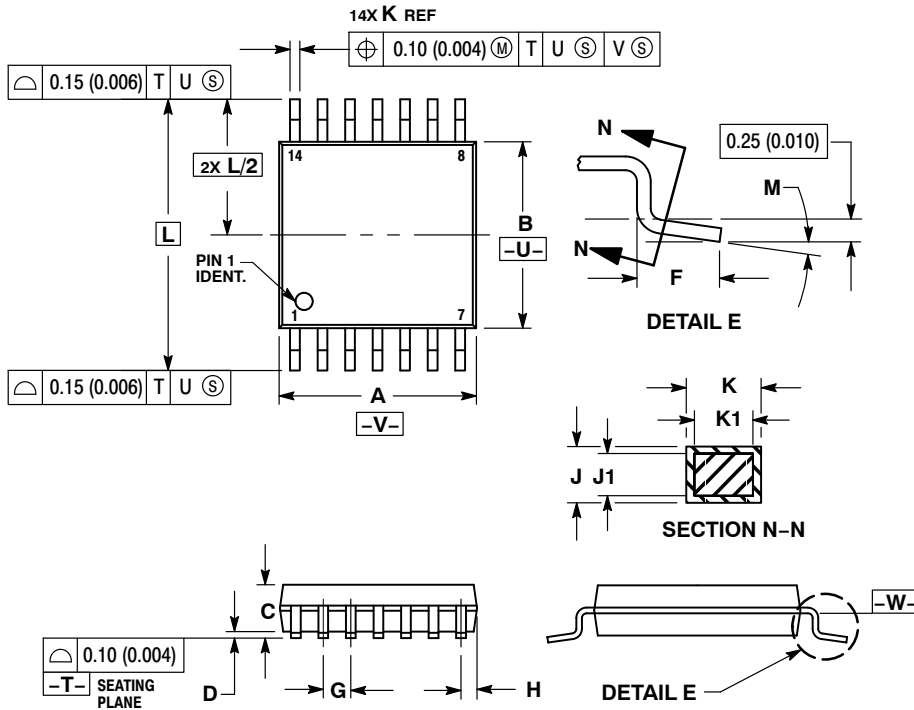
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC132A

## PACKAGE DIMENSIONS

TSSOP-14  
DT SUFFIX  
CASE 948G-01  
ISSUE B

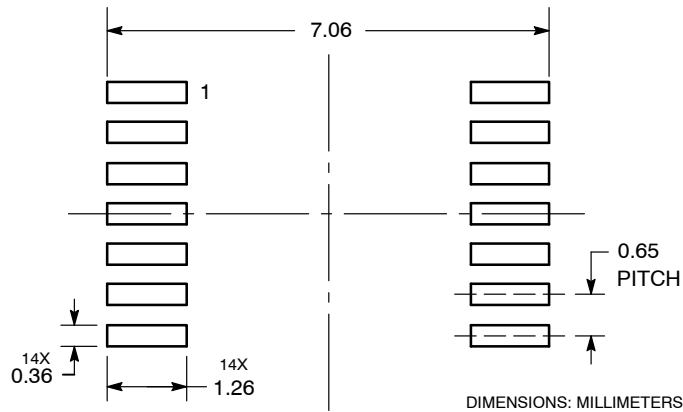


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
M	0°	8°	0°	8°

### SOLDERING FOOTPRINT\*



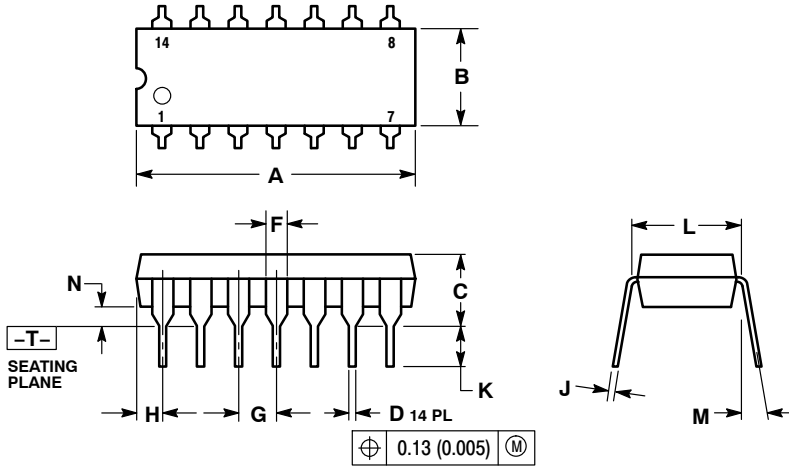
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



# MC74HC132A

## PACKAGE DIMENSIONS

**PDIP-14**  
**N SUFFIX**  
 CASE 646-06  
 ISSUE P



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marketing.pdf](http://www.onsemi.com/site/pdf/Patent-Marketing.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
 USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
 Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
 Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative