

**N-Channel Logic Level Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

V _{DSS}	I _D	R _{DS(ON)} (mΩ) Typ
100V	35A	30 @ V _{GS} =10V

FEATURES

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- TO-220 package.

**ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Drain Current-Continuous ^a	T _C =25°C	35
		T _C =70°C	29.3
I _{DM}	-Pulsed ^a	103	A
P _D	Maximum Power Dissipation	T _C =25°C	75
		T _C =70°C	52.5
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 175	°C

THERMAL CHARACTERISTICS

R _{θ JC}	Thermal Resistance, Junction-to-Case	2	°C/W
R _{θ JA}	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body leakage current	V _{GS} = ±20V , V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1.5	2.5	3.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V , I _D =17.5A		30	36	m ohm
g _{FS}	Forward Transconductance	V _{DS} =10V , I _D =17.5A		12		S
DYNAMIC CHARACTERISTICS ^b						
C _{ISS}	Input Capacitance	V _{DS} =25V, V _{GS} =0V f=1.0MHz		1490		pF
C _{OSS}	Output Capacitance			155		pF
C _{RSS}	Reverse Transfer Capacitance			100		pF
SWITCHING CHARACTERISTICS ^b						
t _{D(ON)}	Turn-On DelayTime	V _{DD} =50V I _D =1A		36		ns
t _r	Rise Time			41		ns
t _{D(OFF)}	Turn-Off DelayTime	V _{GS} =10V R _{GEN} = 6 ohm		39		ns
t _f	Fall Time			22		ns
Q _g	Total Gate Charge	V _{DS} =50V, I _D =17.5A, V _{GS} =10V		19		nC
Q _{gs}	Gate-Source Charge	V _{DS} =50V, I _D =17.5A, V _{GS} =10V		2.6		nC
Q _{gd}	Gate-Drain Charge			10		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =5A		0.8	1.3	V
Notes a. Drain current limited by maximum junction temperature. b. Guaranteed by design, not subject to production testing.						

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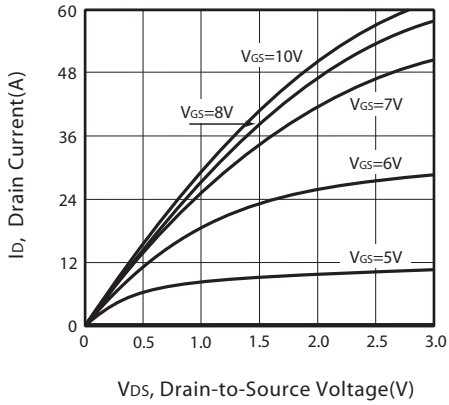


Figure 1. Output Characteristics

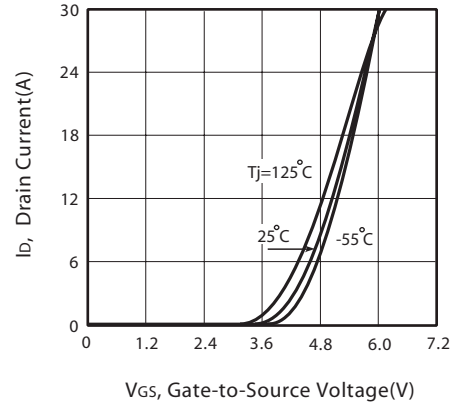


Figure 2. Transfer Characteristics

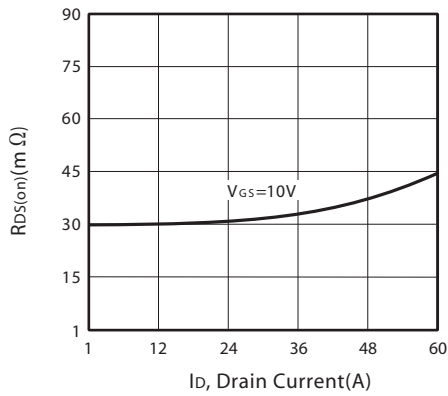


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

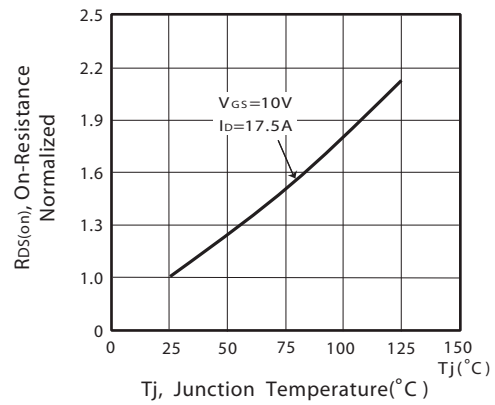


Figure 4. On-Resistance Variation with Drain Current and Temperature

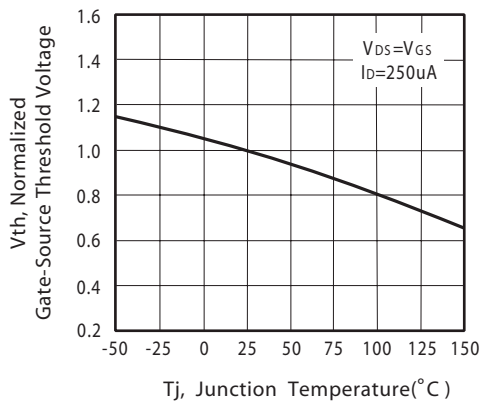


Figure 5. Gate Threshold Variation with Temperature

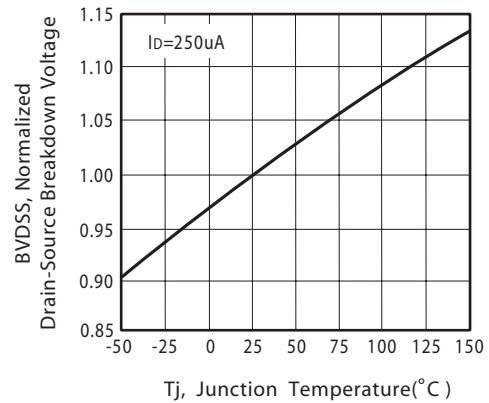


Figure 6. Breakdown Voltage Variation with Temperature

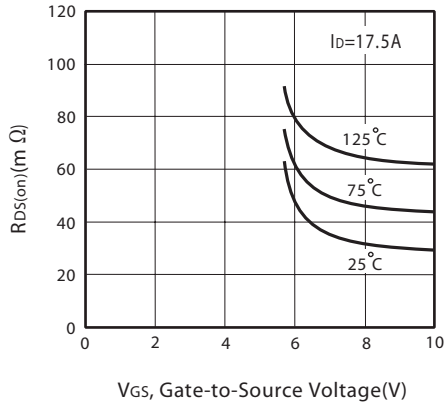


Figure 7. On-Resistance vs. Gate-Source Voltage

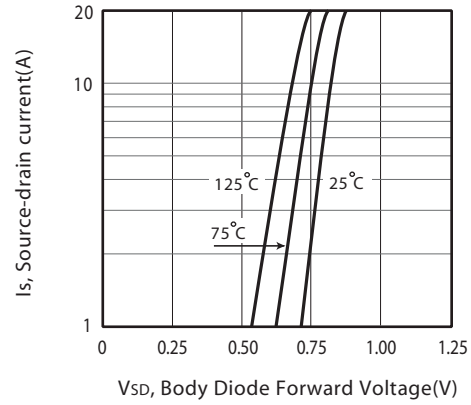


Figure 8. Body Diode Forward Voltage Variation with Source Current

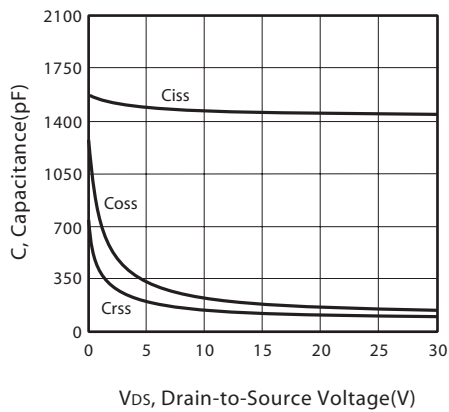


Figure 9. Capacitance

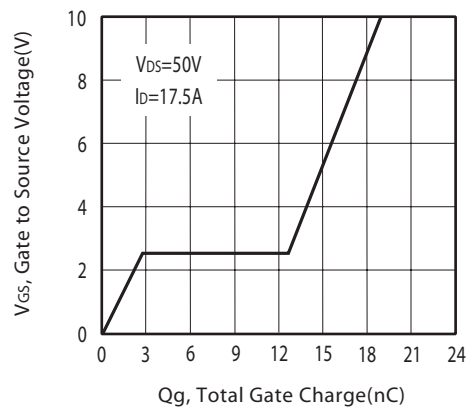


Figure 10. Gate Charge

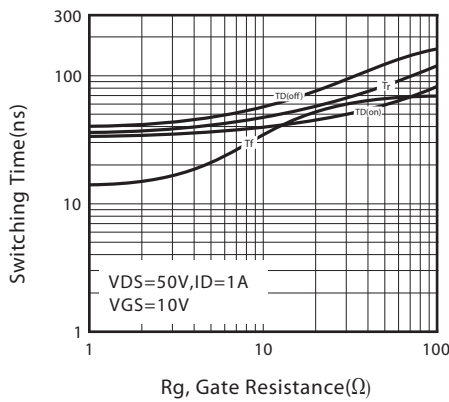


Figure 11. switching characteristics

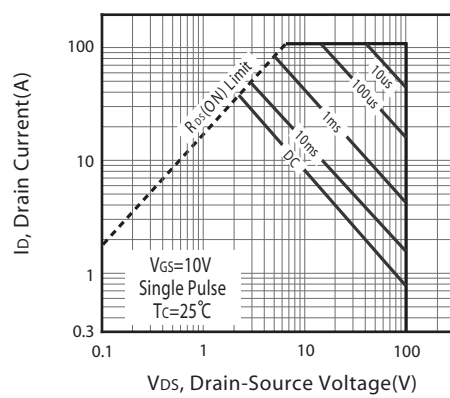
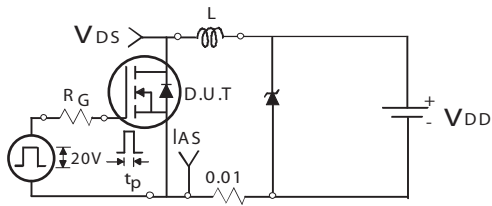


Figure 12. Maximum Safe Operating Area

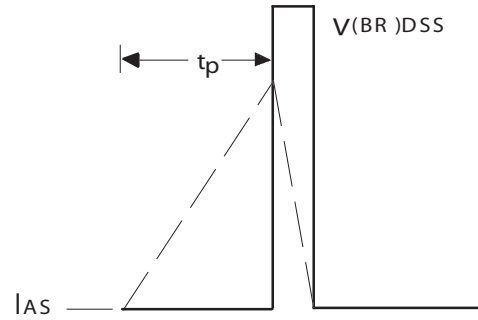
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Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

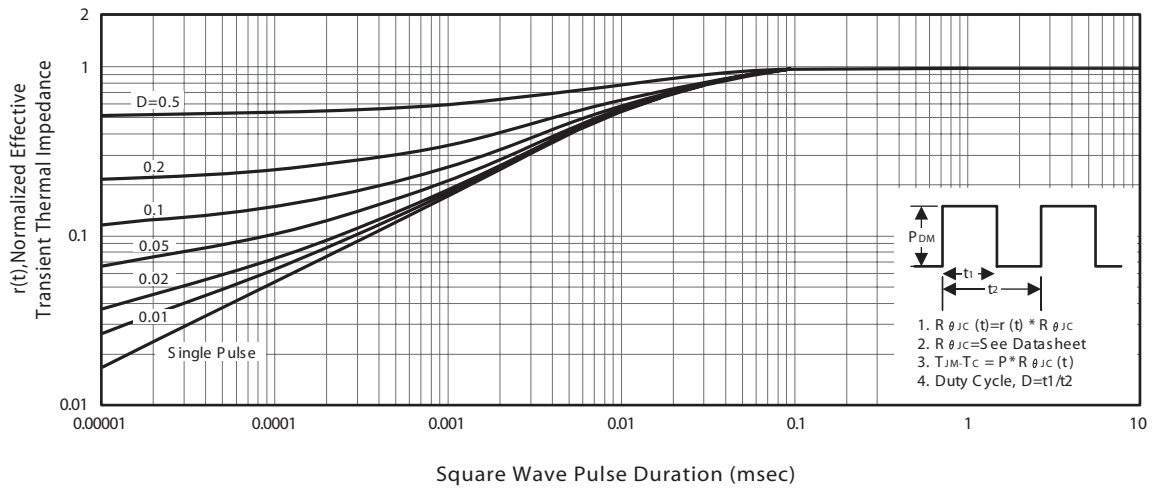


Figure 14. Normalized Thermal Transient Impedance Curve

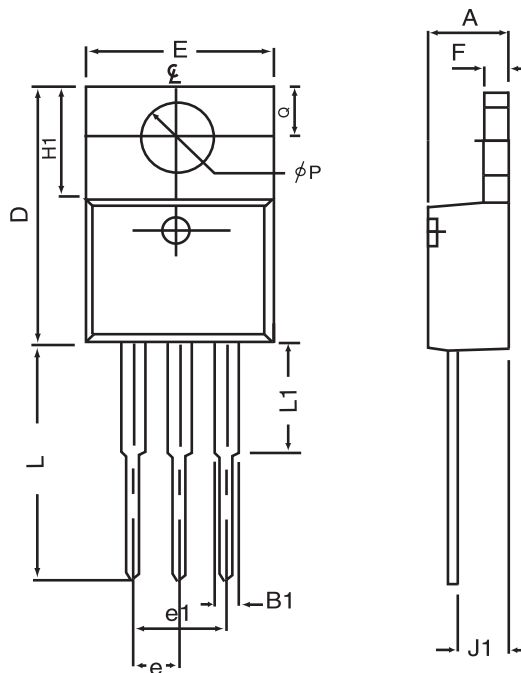
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PACKAGE OUTLINE DIMENSIONS

TO-220

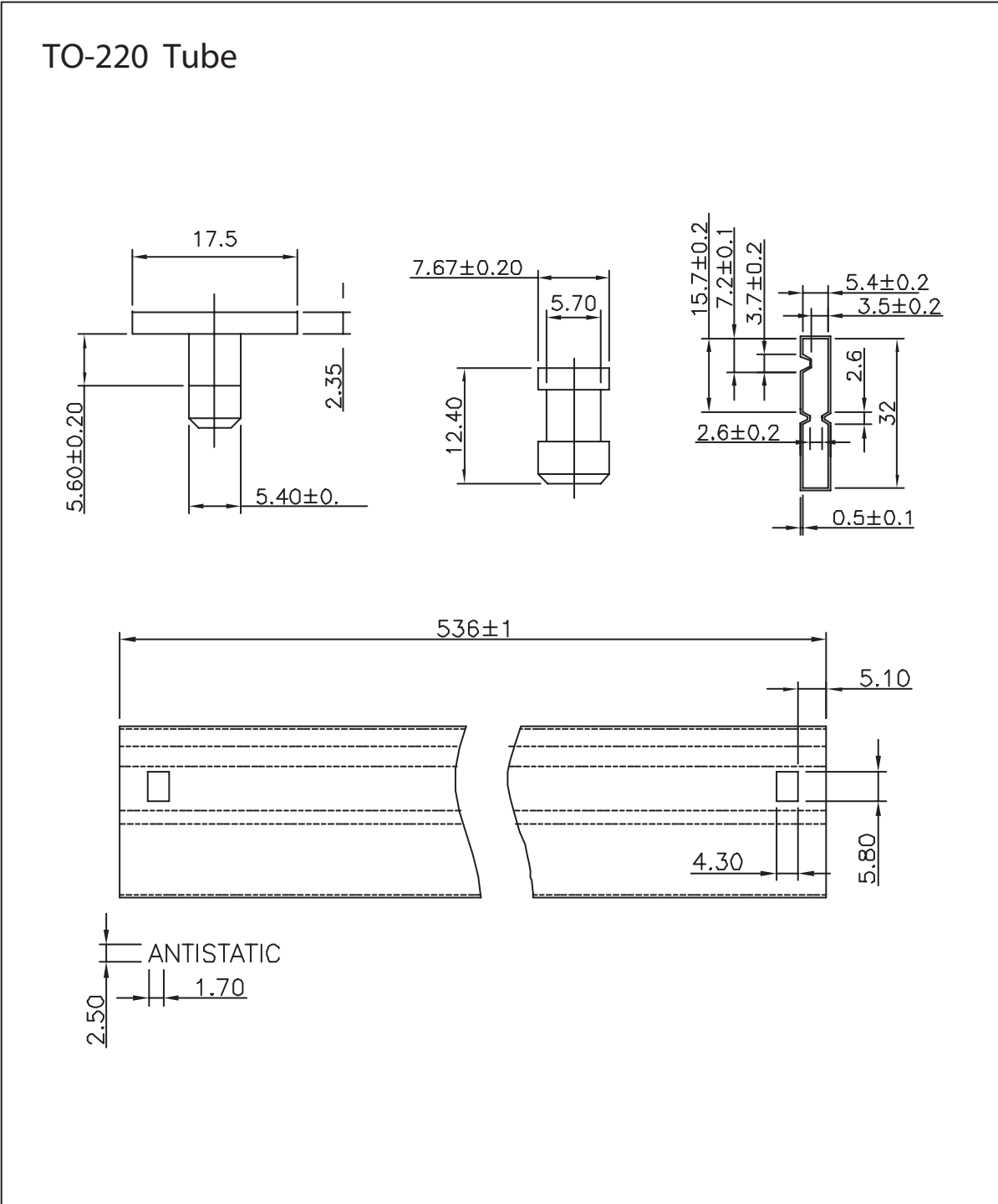


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
phi P	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120

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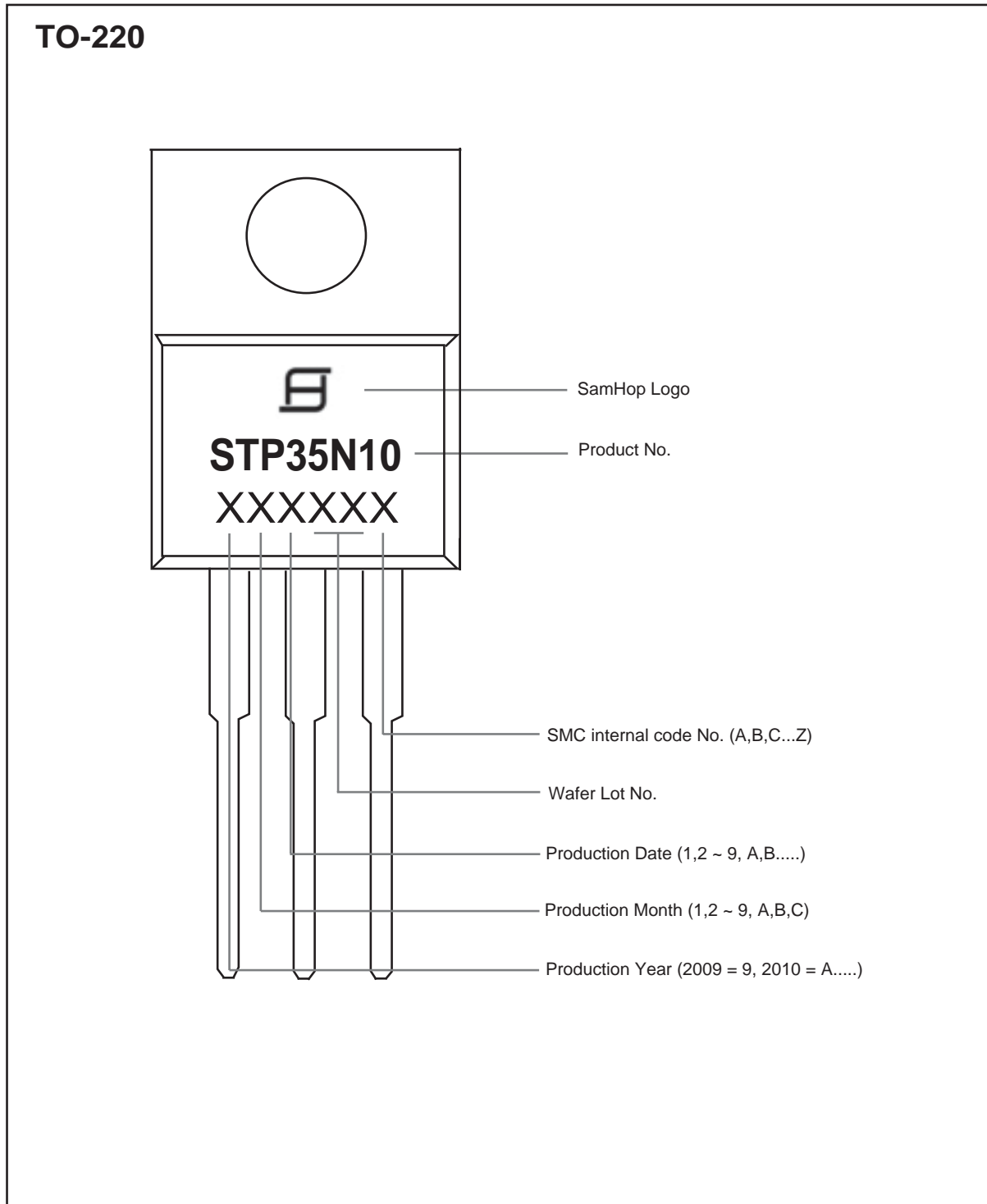


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TOP MARKING DEFINITION



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