DATA SHEET

SKYA21052: 0.7 to 2.7 GHz SP12T MIPI® Antenna Switch Module

Applications

- 2G/3G/4G/4G LTE, 4G LTE-A
- Embedded cellular telematics modules
- OBD-II cellular modems

Features

- High isolation and linearity
- Broadband frequency range: 0.7 to 2.7 GHz
- Dedicated Band 7 TRX ports: 0.8 dB insertion loss @ 2.7 GHz
- Integrated low-band and high-band GSM harmonic filters
- Integrated MIPI interface
- Automotive Level-3 PPAP available upon request
- IMDS material declaration available at production release
- Extended production life to support automotive requirements
- Independent BOM management to minimize PCN risk
- Extended operating temperature: –40 °C to +105 °C Tc
- Small MCM (20-pin, 2.5 x 2.5 x 0.8 mm) package (MSL3, 260 °C per JEDEC J–STD–020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

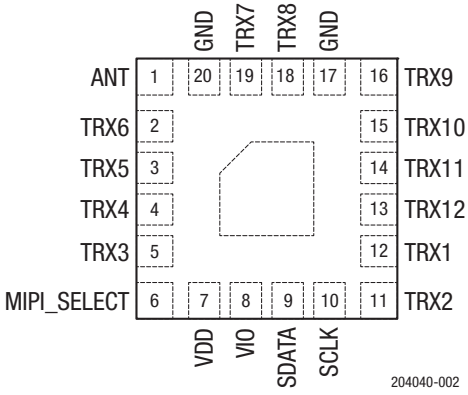


Figure 2. SKYA21052 Pinout (Top View)

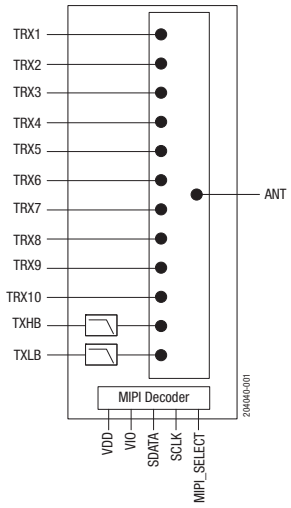


Figure 1. SKYA21052 Block Diagram

Description

The SKYA21052 is a single-pole, twelve-throw (SP12T) antenna switch with an integrated Mobile Industry Processor Interface (MIPI) controller. Using an advanced switching technology, the SKYA21052 maintains low insertion and high isolation, which makes it an ideal choice for UMTS, CDMA2000, EDGE, GSM, and LTE applications.

The design features two dedicated GSM transmit ports and three dedicated ultra low-loss TRX ports. The switch also has an excellent triple beat ratio and second/third order intermodulation distortion (IMD2/IMD3) performance.

Switching is controlled by the MIPI decoder. There is an external MIPI select pin that enables how the switch responds to power mode triggers. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch responds to individual power mode triggers.

No external DC blocking capacitors are required on the RF paths as long as no DC voltage is applied.

The SKYA21052 is manufactured in a compact, 2.5 x 2.5 x 0.8 mm, 20-pin surface-mount Multi-Chip Module (MCM) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Table 1. SKYA21052 Signal Descriptions[1]

Pin	Name	Description	Pin	Name	Description
1	ANT	Antenna port	11	TRX2	Ultra low-loss 3G WCDMA transmit/receive port 2. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
2	TRX6	3G WCDMA transmit/receive port 6. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	12	TRX1	Ultra low-loss 3G WCDMA transmit/receive port 1. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
3	TRX5	3G WCDMA transmit/receive port 5. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	13	TRX10	3G WCDMA transmit/receive port 10. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
4	TRX4	Ultra low-loss 3G WCDMA transmit/receive port 4. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	14	TRX9	3G WCDMA transmit/receive port 9. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
5	TRX3	Ultra low-loss 3G WCDMA transmit/receive port 3. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	15	TRX8	3G WCDMA transmit/receive port 8. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
6	MIPI_SELECT	MIPI interface select. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch is RFFE MIPI compliant and responds to individual power mode triggers.	16	TRX7	3G WCDMA transmit/receive port 7. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
7	VDD	DC power supply	17	GND	Ground
8	VIO	MIPI decoder enable/reference voltage	18	TXHB	GSM transmit high band. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
9	SDATA	Data input/output	19	TXLB	GSM transmit low band. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
10	SCLK	Clock signal	20	GND	Ground

[1] Bottom ground paddles must be connected to ground.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKYA21052 are provided in Table 2. Table 3 provides the recommended operating conditions. Electrical specifications are provided in Table 4.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 5 and 6, respectively.

Triple beat ratio (TBR) test conditions for bands 2 and 5 are listed in Table 7.

Figure 3 shows a timing diagram. Figure 4 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm continuous wave (CW) signal, f_{FUND}, is sequentially applied to the TRX1 through TRX10 ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting third order intermodulation distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKYA21052 exhibits exceptional performance for all TRXx ports.

Table 8 shows the isolation matrix for "On" arms to "Off" arms. Table 9 shows the isolation matrix for "Ant" to "Off" arms. Table 10 provides the matrix of insertion loss and return loss information. Table 11 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front–End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figures 5 and 6 provide the timing diagrams for register write commands and read commands, respectively.

Table 12 provides the Register_0 logic. Table 13 describes the register parameters and bit values.

Table 2. SKYA21052 Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V_{DD}	2.5		6.0	V
MIPI decoder enable/reference voltage	VIO			2	V
Clock signal voltage	SCLK			VIO	V
Data signal voltage	SDATA			VIO	V
RF input power:	P_{IN}				
LTX pin				+36	dBm
HTX pin				+34	dBm
All TRXx pins				+31	dBm
Ambient temperature ranges:					
Operating	T_A[2]	–40	+25	+95	°C
Storage	T_{STG}	–40		+150	°C
Electrostatic discharge:	ESD				
Charged Device Model (CDM), Class C4				1000	V
Human Body Model (HBM), Class 1C				1500	V

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

2 In all cases, ambient operating temperature (T_A) is specified relative to case temperature (T_C) and assumes $T_A = (T_C – 10\ °C)$. Case temperature (T_C) refers to the temperature of the ground pad at the underside of the package.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. SKYA21052 Recommended Operating Conditions[1]
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply voltage	V_{DD}		2.50	2.85	5.50	V
Supply current, active mode	I_{DD}			50	100	µA
Supply current, low power mode	I_{DD_L}			10		µA
Interface supply voltage	VIO		1.65	1.80	1.95	V
Interface signal: High Low	SDATA		 0.8 × VIO		 0.2 × VIO	 V V
Control current: High Low				 1 1	 5 5	 µA µA
Ambient operating temperature[1,2]	T_{RANGE}		–40	+25	+80	°C
	$T_{EXTENDED}$		–40		+95	°C

1 Performance is guaranteed only under the conditions listed in this table.

2 In all cases, ambient operating temperature (T_A) is specified relative to case temperature (T_C) and assumes $T_A = (T_C – 10\ °C)$. Case temperature (T_C) refers to the temperature of the ground pad at the underside of the package.

Table 4. SKYA21052 RF Electrical Specifications[1] (1 of 2)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Operating frequency	f		0.7		2.7	GHz
Insertion loss	I_L	TXLB, 824 to 915MHz		1.25	1.45	dB
		TXHB,1710 to 1910 MHz		1.25	1.4	dB
		TRX1 to TRX10 ports: 700 to 824MHz 824 to 960 MHz 1710 to 1990 MHz		 0.6 0.62 0.75	 0.8 0.85 0.9	 dB dB dB
		TRX4 to TRX10 ports: 2110 to 2170 MHz		 0.8	 0.95	 dB
		TRX4 to TRX10 ports (except TRX6): 2300 to 2690 MHz		 0.95	 1.25	 dB
		TRX6 port: 2300 to 2690 MHz		 1.1	 1.4	 dB
		TRX1 to TRX3 ports: 2110 to 2170 MHz 2300 to 2690 MHz		 0.8 0.9	 1.05 1.05	 dB dB
GSM LB TX: 2f0 attenuation 3f0 attenuation 4f0 attenuation	 H2LB H3LB H4LB	 2f0 attenuation 1830 MHz 3f0 attenuation 2745 MHz 4f0 attenuation 3660 MHz	 20 20	 23 28 25		 dB dB dB
GSM HB TX: 2f0 attenuation 3f0 attenuation	 H2HB H3HB	 2f0 attenuation 3820 MHz 3f0 attenuation 5730 MHz	 20 15	 22.5 17		 dB dB

Table 4. SKYA21052 RF Electrical Specifications[1] (2 of 2)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Isolation	ISO	TRx 1, 2, 7, 8, 9, 10 ports to TRx 3, 4, 5, 6 ports: 824 to 1910 MHz 1910 to 2690 MHz	 32 25	 35 30		 dB dB
		Tx LB to any TRx/Rx ports: 824 to 960 MHz	 35	 36		 dB
		Tx HB to any TRx/Rx ports: 1710 to 1910 MHz	 30	 32		 dB
		Any adjacent ports: 824 to1910 MHz 1910 to 2690 MHz	 20 17	 23 19		 dB dB
		Any non-adjacent ports: 824 to1910 MHz 1910 to 2690MHz	 25 20	 28 23		 dB dB
		Antenna to any TRx ports: 824 to1910 MHz 1910 to 2690 MHz	 30 23	 31.5 26		 dB dB
		Tx LB to Tx HB when TX HB is on: 1648 to 1830 MHz	 27	 28.5		 dB
Return loss	|S11|	0.7 to 2.7 GHz	14	18		dB
GSM harmonics: High band Low band	2fo, 3fo	 P_{IN} = +33 dBm, 50 Ω P_{IN} = +33 dBm, 3:1 VSWR P_{IN} = +35 dBm, 50 Ω P_{IN} = +35 dBm, 3:1 VSWR		 –53 –41 –50 –36	 –40 –45 	 dBm dBm dBm dBm
TRXx harmonics	2fo, 3fo	P_{IN} = +27 dBm, 50 Ω, f = 704 to 2700 MHz P_{IN} = +27 dBm, 5:1 VSWR, f = 704 to 2700 MHz		–68 –58	–62 –50	dBm dBm
TRX1 through TRX10, band 13 2nd harmonics	2fo	P_{IN} = +25 dBm f = 787 MHz		 –81		 dBm
Second order intermodulation distortion	IMD2	See test conditions in Table 5		–110	–105	dBm
Third order intermodulation distortion	IMD3	See test conditions in Table 6		–110	–105	dBm
Triple Beat Ratio: 650 to 900 MHz 1710 to 2155 MHz	TBR	See test conditions in Table 7	 +81 +81			 dBc dBc
Turn-on time	t_{ON}	From application of V_{DD} and VIO			20	µs
Switching speed	t_S	Port to port		2	5	µs

[1] Performance is guaranteed only under the conditions listed in this table.

Table 5. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 6. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 7. Triple Beat Ratio Test Conditions

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker @ ANT (MHz)	Power Blocker (dBm)	TBR Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	–30	1960.0 ± 1
5	836.5		881.5		881.5		881.5 ± 1

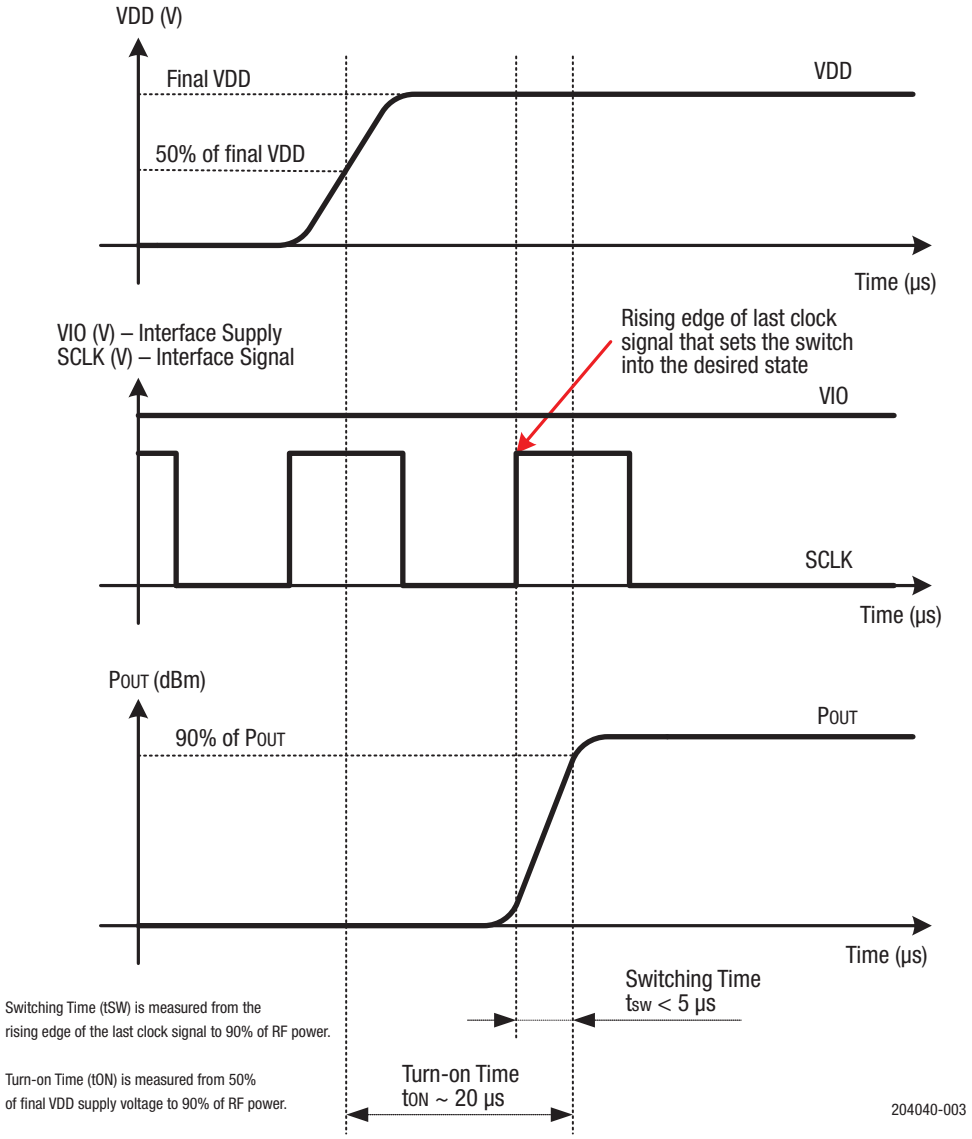


Figure 3. SKYA21052 Timing Diagram

Table 8. SKYA21052: Isolation Matrix: Isolation "On" Arms to "Off" Arms

		Isolation (dB)											
ON_Throw	freq (GHz)	TXLB	TXHB	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
TXLB	0.915		–32	–50	–54	–52	–47	–45	–45	–47	–49	–50	–51
TXLB	1.91		–28	–48	–49	–45	–46	–43	–46	–40	–40	–43	–47
TXLB	2.69		–19	–46	–48	–44	–44	–42	–46	–38	–39	–42	–46
TXHB	0.915	–35		–47	–52	–56	–55	–50	–49	–39	–41	–45	–43
TXHB	1.91	–24		–39	–43	–43	–43	–41	–39	–33	–36	–38	–35
TXHB	2.69	–19		–49	–41	–50	–50	–48	–44	–41	–40	–45	–39
TRX1	0.915	–36	–46		–36	–52	–56	–53	–50	–49	–45	–42	–35
TRX1	1.91	–35	–33		–28	–41	–43	–42	–39	–40	–39	–35	–28
TRX1	2.69	–32	–29		–24	–37	–38	–38	–33	–35	–35	–32	–24
TRX2	0.915	–37	–52	–36		–49	–55	–54	–49	–50	–47	–44	–38
TRX2	1.91	–35	–35	–28		–40	–42	–42	–39	–41	–40	–37	–31
TRX2	2.69	–32	–30	–24		–36	–37	–37	–33	–36	–36	–33	–27
TRX3	0.915	–32	–48	–49	–46		–29	–36	–38	–53	–55	–54	–52
TRX3	1.91	–31	–36	–41	–38		–23	–30	–31	–43	–46	–45	–44
TRX3	2.69	–30	–32	–37	–34		–20	–25	–26	–37	–41	–41	–40
TRX4	0.915	–33	–46	–50	–47	–35		–30	–36	–53	–55	–54	–52
TRX4	1.91	–32	–36	–41	–39	–28		–23	–28	–42	–45	–45	–44
TRX4	2.69	–31	–33	–37	–34	–24		–20	–24	–37	–40	–40	–40
TRX5	0.915	–34	–45	–50	–48	–39	–35		–30	–52	–54	–53	–52
TRX5	1.91	–34	–36	–40	–39	–32	–28		–23	–42	–45	–44	–43
TRX5	2.69	–33	–34	–36	–34	–28	–24		–19	–36	–40	–39	–39
TRX6	0.915	–36	–43	–49	–49	–41	–40	–36		–51	–52	–51	–51
TRX6	1.91	–39	–36	–40	–39	–33	–32	–28		–41	–43	–43	–43
TRX6	2.69	–35	–36	–35	–34	–28	–28	–24		–36	–38	–38	–38
TRX7	0.915	–36	–44	–44	–48	–56	–57	–52	–50		–30	–35	–41
TRX7	1.91	–50	–34	–36	–39	–43	–44	–42	–39		–24	–29	–35
TRX7	2.69	–37	–41	–32	–34	–38	–39	–38	–34		–21	–26	–32
TRX8	0.915	–36	–45	–42	–47	–56	–57	–52	–50	–37		–29	–38
TRX8	1.91	–41	–35	–35	–39	–43	–44	–42	–39	–29		–24	–32
TRX8	2.69	–36	–37	–31	–34	–38	–39	–38	–34	–25		–21	–29
TRX9	0.915	–35	–45	–38	–45	–55	–57	–52	–50	–40	–35		–31
TRX9	1.91	–38	–34	–32	–38	–43	–44	–42	–39	–33	–28		–25
TRX9	2.69	–35	–32	–28	–33	–38	–39	–38	–33	–28	–25		–22
TRX10	0.915	–36	–46	–29	–38	–54	–57	–52	–50	–47	–42	–37	
TRX10	1.91	–36	–34	–23	–31	–42	–43	–42	–39	–39	–36	–31	
TRX10	2.69	–33	–30	–19	–26	–38	–39	–38	–33	–34	–32	–27	

Table 9. SKYA21052: Isolation Matrix "ANT" to "Off" Arms

		Isolation (dB)											
ON_Throw	freq (GHz)	TXLB	TXHB	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
ANT	0.915		–35	–46	–46	–43	–41	–39	–36	–44	–45	–46	–47
ANT	1.91		–47	–49	–48	–38	–34	–32	–32	–45	–46	–48	–50
ANT	2.69		–37	–45	–44	–39	–34	–32	–34	–45	–46	–47	–48
ANT	0.915	–46		–46	–43	–45	–43	–41	–39	–46	–49	–47	–51
ANT	1.91	–24		–37	–36	–38	–37	–34	–32	–33	–35	–36	–37
ANT	2.69	–25		–37	–37	–36	–34	–32	–32	–32	–34	–34	–34
ANT	0.915	–39	–36		–43	–48	–45	–42	–40	–48	–54	–53	–46
ANT	1.91	–35	–32		–32	–41	–39	–37	–33	–40	–43	–41	–34
ANT	2.69	–33	–34		–27	–37	–36	–34	–29	–35	–38	–36	–28
ANT	0.915	–38	–35	–44		–50	–46	–43	–40	–47	–51	–54	–49
ANT	1.91	–35	–31	–34		–42	–40	–37	–33	–39	–42	–42	–37
ANT	2.69	–33	–35	–28		–37	–36	–33	–29	–35	–38	–37	–31
ANT	0.915	–38	–37	–48	–51		–36	–46	–39	–46	–46	–47	–48
ANT	1.91	–32	–32	–37	–39		–28	–33	–30	–39	–40	–40	–40
ANT	2.69	–31	–38	–33	–34		–25	–28	–26	–35	–37	–37	–37
ANT	0.915	–39	–37	–48	–50	–44		–38	–41	–46	–47	–47	–48
ANT	1.91	–32	–33	–38	–39	–32		–28	–30	–39	–40	–40	–41
ANT	2.69	–31	–40	–34	–34	–27		–25	–26	–35	–37	–37	–37
ANT	0.915	–41	–38	–48	–49	–46	–45		–39	–46	–47	–47	–48
ANT	1.91	–34	–34	–39	–39	–35	–33		–27	–39	–40	–41	–41
ANT	2.69	–31	–43	–34	–34	–30	–27		–23	–35	–37	–37	–37
ANT	0.915	–42	–39	–48	–48	–43	–44	–42		–47	–48	–48	–49
ANT	1.91	–39	–34	–39	–39	–34	–35	–32		–39	–41	–41	–41
ANT	2.69	–32	–44	–34	–34	–29	–30	–26		–34	–37	–37	–37
ANT	0.915	–43	–34	–53	–48	–46	–44	–42	–39		–37	–48	–52
ANT	1.91	–43	–29	–41	–38	–40	–38	–36	–33		–29	–36	–42
ANT	2.69	–33	–30	–36	–33	–36	–35	–33	–29		–26	–31	–37
ANT	0.915	–42	–35	–52	–49	–46	–44	–41	–39	–41		–37	–44
ANT	1.91	–41	–32	–41	–38	–40	–38	–36	–33	–32		–29	–37
ANT	2.69	–34	–39	–36	–33	–36	–35	–33	–29	–26		–27	–35
ANT	0.915	–41	–36	–45	–48	–47	–44	–42	–39	–44	–48		–35
ANT	1.91	–38	–33	–38	–37	–40	–38	–36	–33	–35	–35		–29
ANT	2.69	–34	–42	–34	–32	–36	–35	–33	–29	–29	–29		–27
ANT	0.915	–40	–36	–38	–42	–47	–45	–42	–40	–49	–54	–49	
ANT	1.91	–36	–33	–29	–30	–41	–39	–36	–33	–39	–41	–37	
ANT	2.69	–33	–36	–25	–25	–37	–35	–33	–29	–34	–36	–31	

Table 10. SKYA21052: Insertion Loss and Return Loss Matrix

ON_Throw	freq (GHz)	IL (dB)	RL_pole (dB)	RL_throw (dB)
LB	0.915	–1.1	–20.5	–21.9
HB	1.91	–1.1	–37.3	–25.0
TRX1	0.915	–0.5	–29.1	–26.2
TRX1	0.91	–0.8	–16.2	–14.6
TRX1	2.69	–0.8	–23.6	–21.4
TRX2	0.915	–0.5	–28.7	–26.9
TRX2	0.91	–0.9	–15.3	–14.0
TRX2	2.69	–0.8	–26.2	–21.8
TRX3	0.915	–0.5	–25.1	–24.8
TRX3	0.91	–0.8	–20.6	–17.9
TRX3	2.69	–0.8	–21.5	–31.3
TRX4	0.915	–0.6	–22.9	–23.4
TRX4	0.91	–0.7	–24.4	–20.3
TRX4	2.69	–0.9	–18.3	–22.7
TRX5	0.915	–0.6	–21.2	–21.3
TRX5	0.91	–0.7	–31.7	–22.4
TRX5	2.69	–0.9	–15.8	–18.4
TRX6	0.915	–0.6	–19.4	–19.9
TRX6	0.91	–0.7	–32.7	–25.7
TRX6	2.69	–1.0	–13.2	–14.8
TRX7	0.915	–0.5	–25.9	–24.9
TRX7	0.91	–0.8	–18.3	–16.3
TRX7	2.69	–0.8	–27.2	–27.0
TRX8	0.915	–0.5	–25.5	–24.6
TRX8	0.91	–0.7	–19.4	–16.9
TRX8	2.69	–0.7	–21.6	–22.7
TRX9	0.915	–0.5	–25.7	–24.4
TRX9	0.91	–0.7	–18.7	–16.2
TRX9	2.69	–0.7	–23.7	–24.4
TRX10	0.915	–0.5	–27.4	–25.9
TRX10	0.91	–0.8	–17.3	–15.4
TRX10	2.69	–0.8	–24.2	–23.0

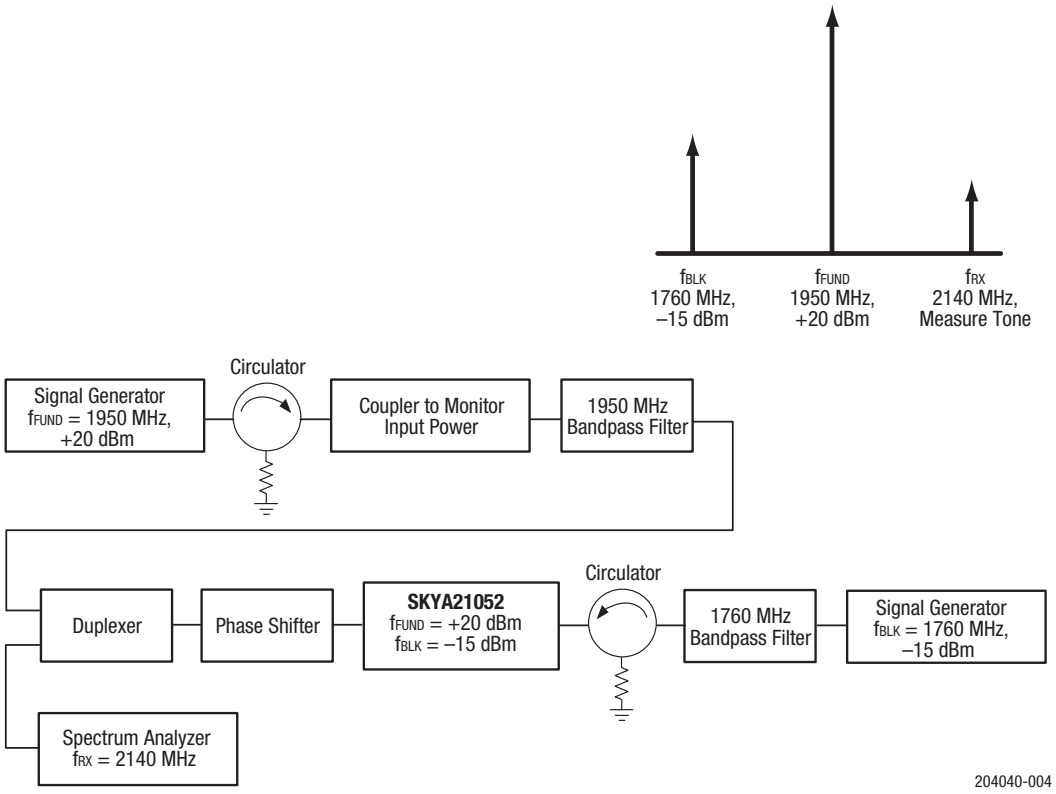


Figure 4. Third Order Intermodulation Test Setup

Table 11. Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1) - DA0(1)	Parity Bits	BPC	DA7(n) - DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	–	–	–	–	–	–
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	–	–	–	Y	Y

Legend:
SSC = Sequence start command
C = Command frame bits
DA = Data/address frame bits
BPC = Bus park cycle
BC = Byte count (# of consecutive addresses)

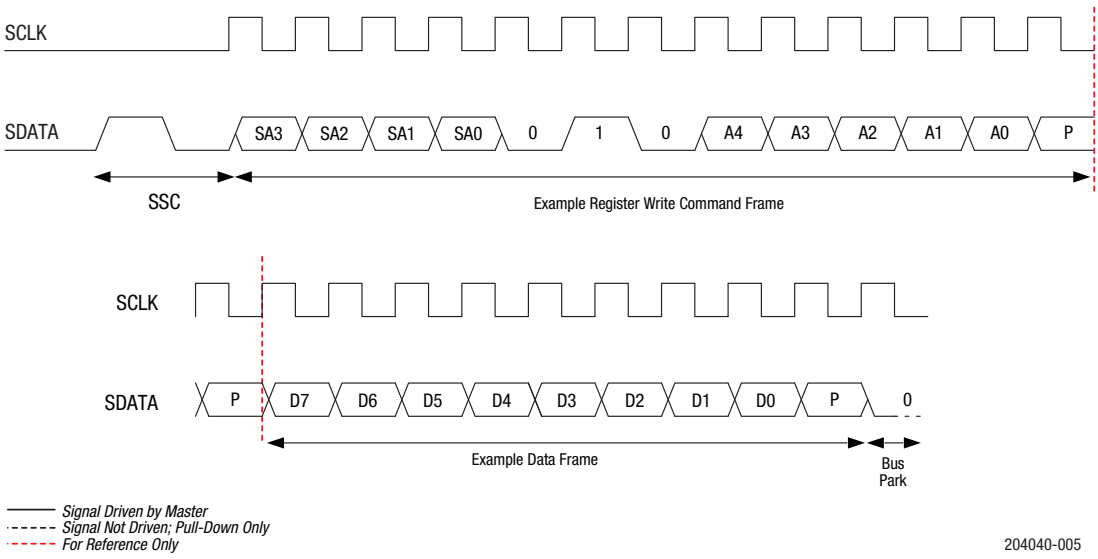


Figure 5. Register Write Command Timing Diagram

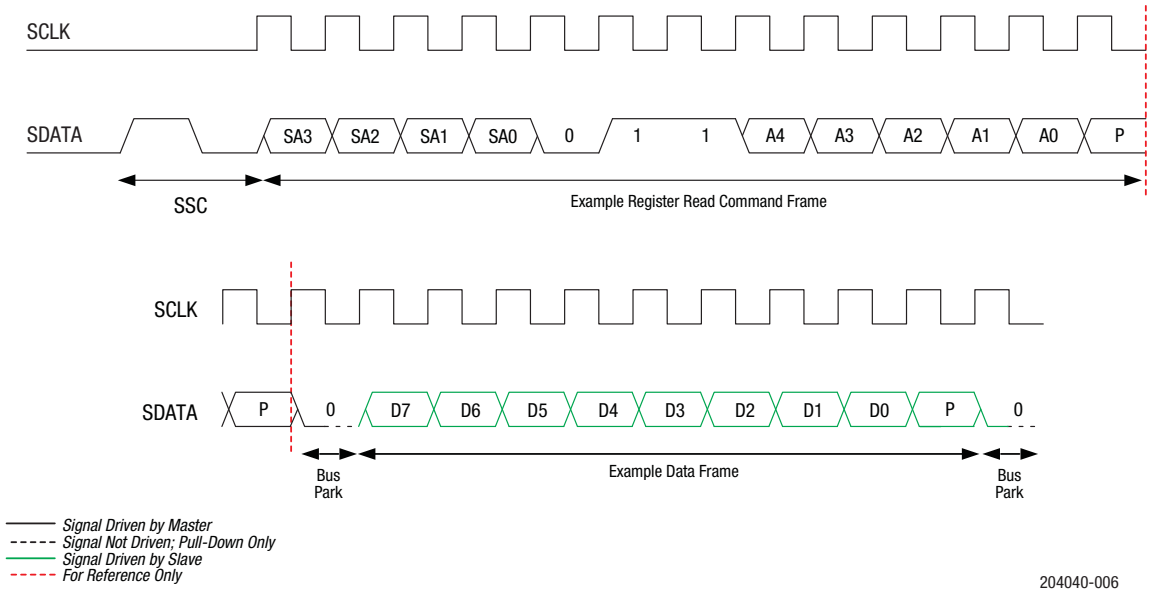


Figure 6. Register Read Command Timing Diagram

Table 12. Register_0 Truth Table

Antenna Path	Register_0 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Sleep mode (standby)	X	0	0	0	0	0	0	0
2G transmit low band	X	0	0	0	1	0	1	0
2G transmit high band	X	0	0	0	1	0	0	0
TRX1	X	0	0	0	0	1	0	0
TRX2	X	0	0	0	0	1	0	1
TRX3	X	0	0	0	0	1	1	0
TRX4	X	0	0	0	0	1	1	1
TRX5	X	0	0	0	1	0	0	1
TRX6	X	0	0	0	1	0	1	1
TRX7	X	0	0	0	1	1	0	0
TRX8	X	0	0	0	0	0	0	1
TRX9	X	0	0	0	0	0	1	0
TRX10	X	0	0	0	0	0	1	1
Isolation mode (warm–up)	X	1	1	1	1	1	1	1

Table 13. Register Description and Programming (1 of 3)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
Register_0	0000	MODE_CTRL	Bits[7:0]: Switch control. See Table 8 for logic	–
RFFE_STATUS	001A	SOFTWARE RESET	Bit[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation 1 = Software reset	0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error =1.	0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the *MIPI Alliance Specification*) or GSID.	0

Table 13. Register Description and Programming (2 of 3)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
GROUP_SID	001B	Reserved	Bits[7:4]: Reserved	0000
		GSID	Bits[3:0]: Group slave ID	0000
PM_TRIG[1]	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	01
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers (unsupported).	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers (unsupported).	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read–only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	01011111

Table 13. Register Description and Programming (3 of 3)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
MANUFACTURER_ID	001E	MANUFACTURER_ID	Bits[7:0]: Read–only register	10100101
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID	Bits[5:4]: Read–only register	01
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1011

[1] Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Evaluation Board Description

The SKYA21052 Evaluation Board is used to test the performance of the SKYA21052 SP12T Switch. An Evaluation Board schematic diagram is provided in Figure 7. A recommended ESD protection circuit diagram is provided in Figure 8. An assembly drawing for the Evaluation Board is shown in Figure 9.

Package Dimensions

The PCB layout footprint for the SKYA21052 is provided in Figure 10. Typical part markings are shown in Figure 11. Package dimensions are shown in Figure 12, and tape and reel dimensions are provided in Figure 13.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKYA21052 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead–free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM–L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

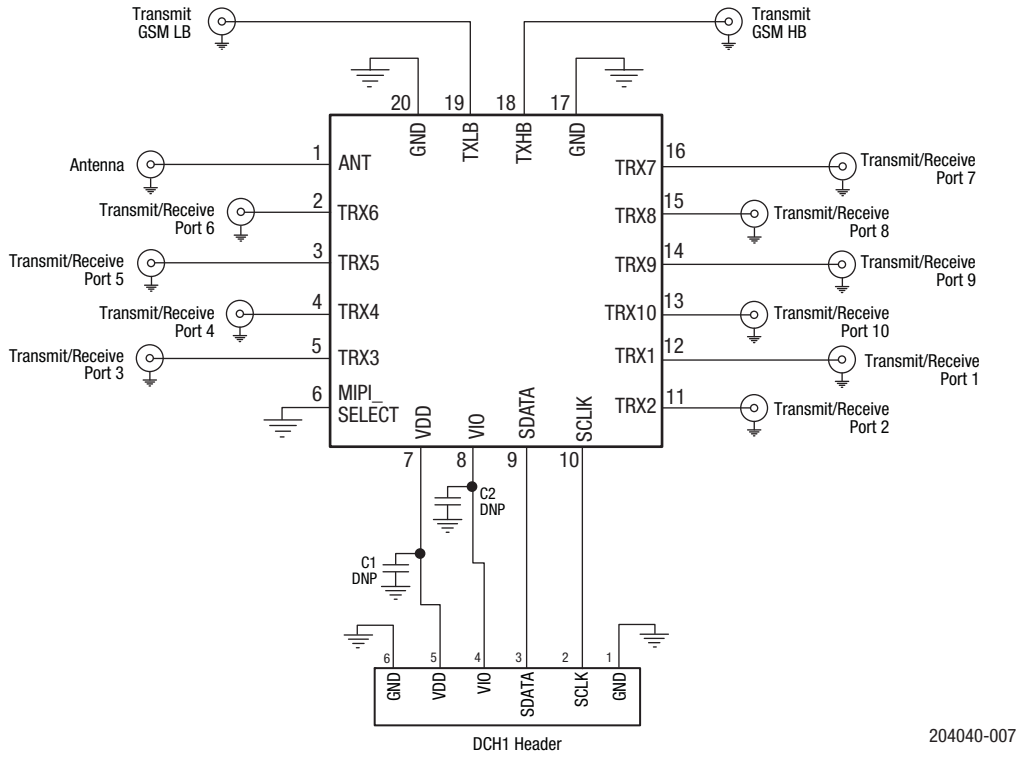
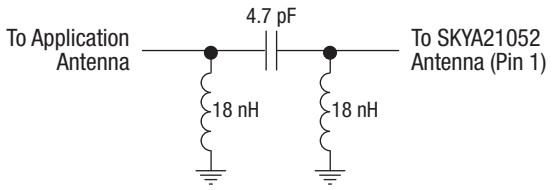
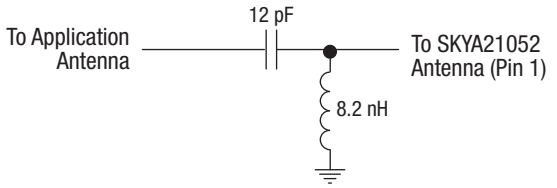


Figure 7. SKYA21052 Evaluation Board Schematic



ESD Circuit 1



ESD Circuit 2

204040-008

Figure 8. SKYA21052 Recommended ESD Protection Circuits

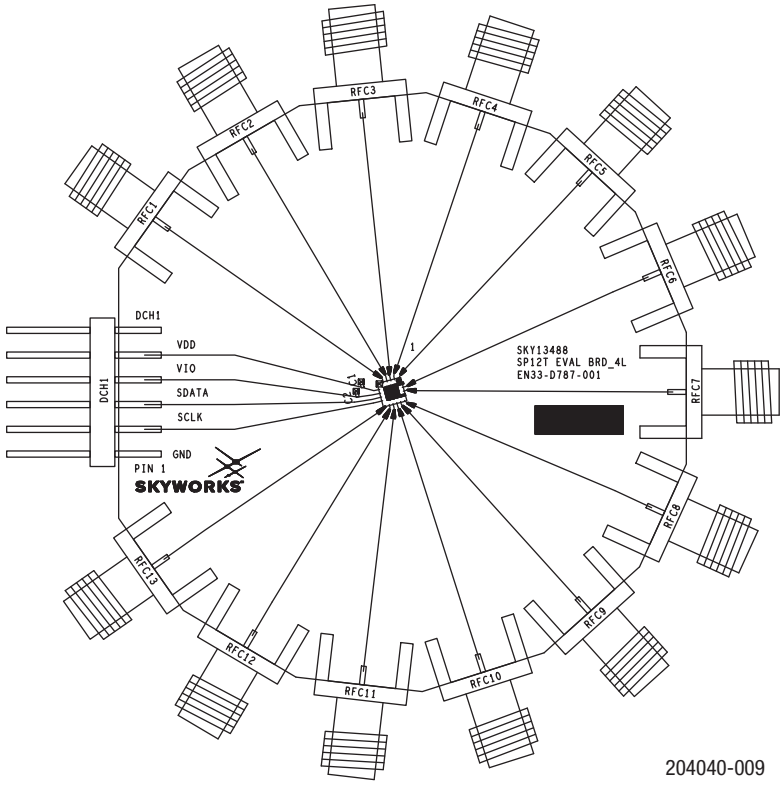
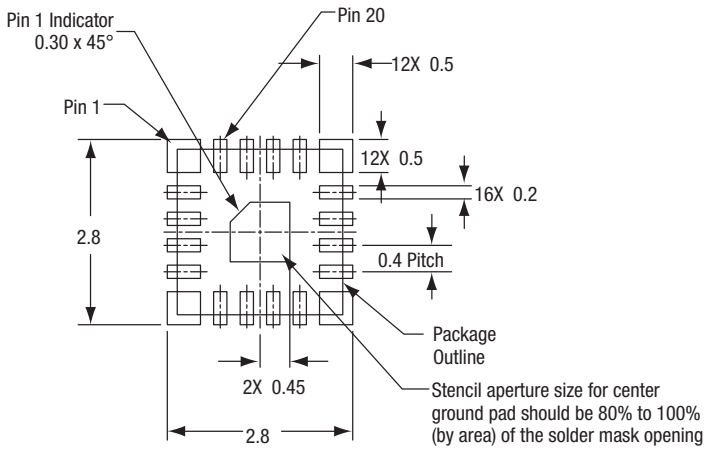
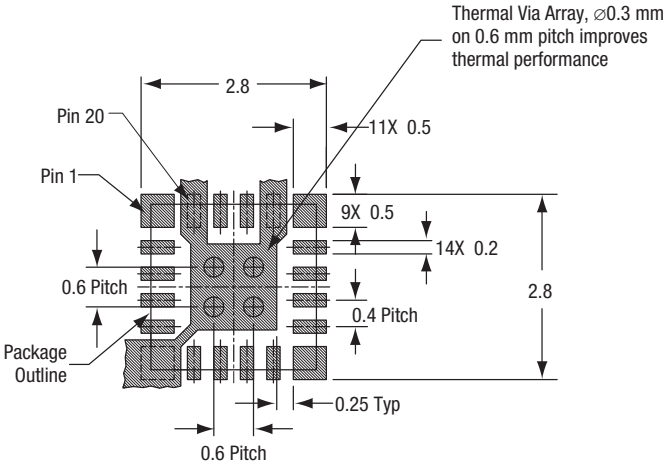


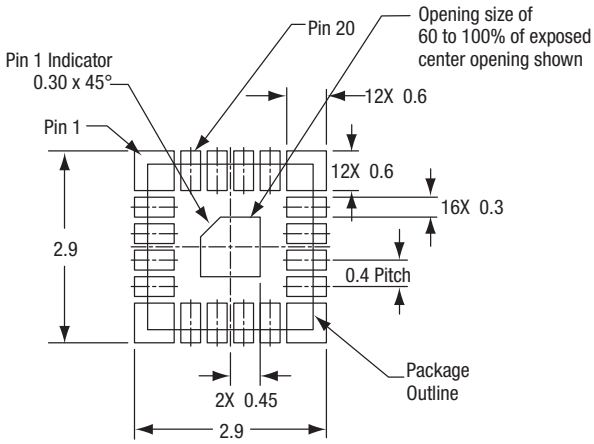
Figure 9. SKYA21052 Evaluation Board Assembly Diagram



Stencil Aperture
Top View



Metallization
Top View



Solder Mask Opening
Top View

Notes:

1. *All dimensions are in millimeters*
2. *Thermal vias should be resin filled and capped according to IPC-4761, Type VII vias.*
3. *Recommended Cu thickness is 30 to 35 mm.*

204040-010

Figure 10. SKYA21052 PCB Layout Footprint (Top View)

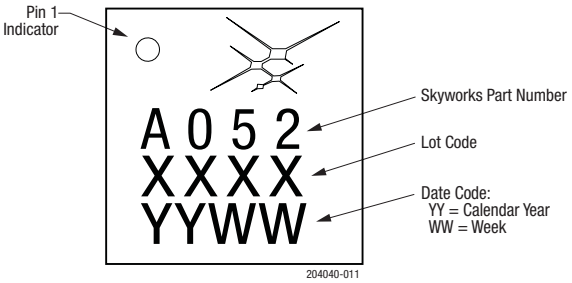
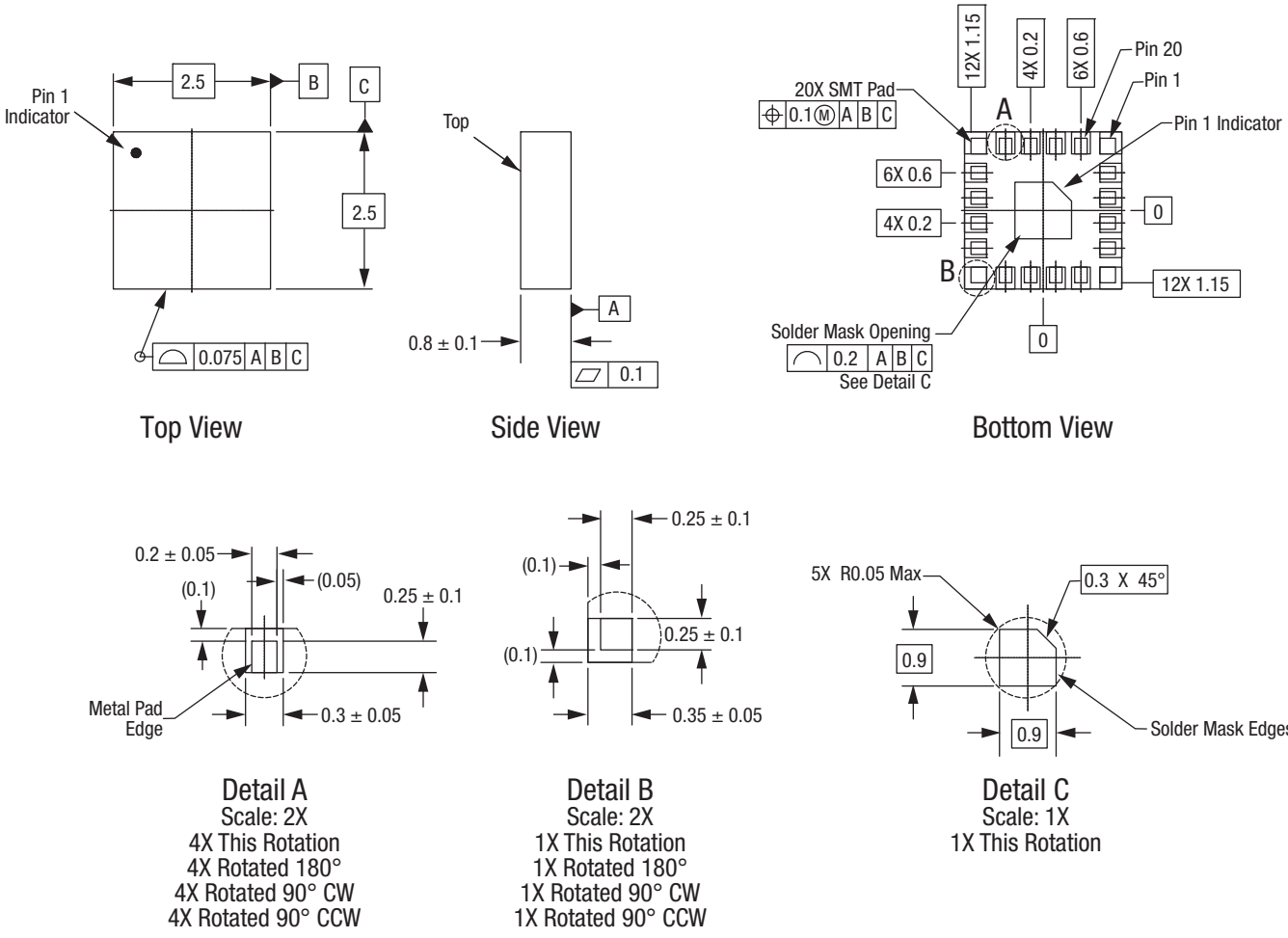


Figure 11. Typical Part Markings (Top View)

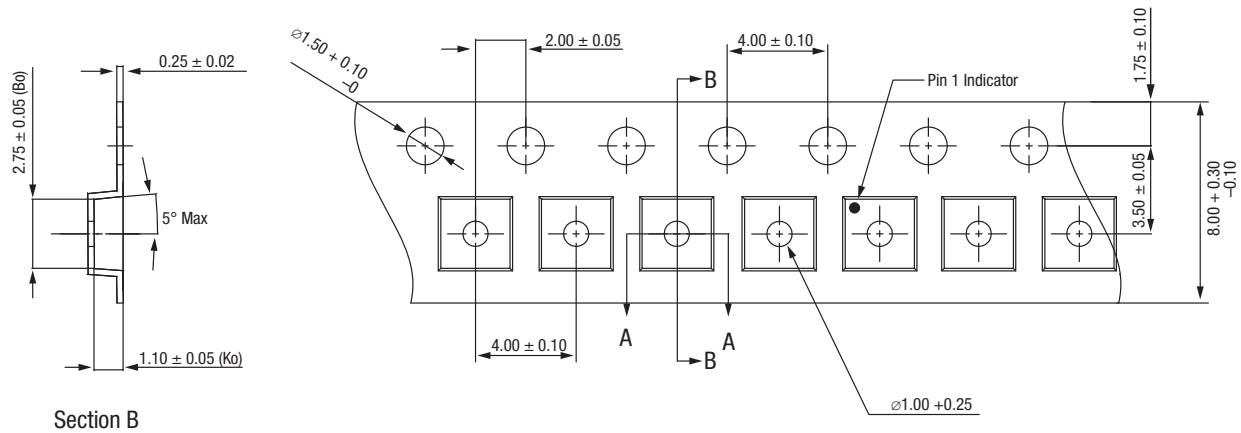


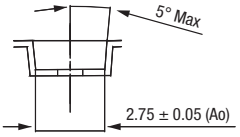
Notes:

1. *Dimensions and tolerances according to ASME Y14.5M-1994.*
2. *All measurements are in millimeters.*

204040-012

Figure 12. SKYA21052 Package Dimensions





Notes:

1. *Carrier tape: black conductive polycarbonate or polystyrene.*
2. *Cover tape material: transparent conductive.*
3. *ESD-surface resistivity shall be ≤ 1 x 10^{10} Ω/square per EIA, JEDEC TNR Specification.*
4. *10-sprocket hole pitch cumulative tolerance: ±0.20 mm.*
5. *Ao and Bo measurement point to be 0.30 mm from bottom pocket.*
6. *All dimensions are in millimeters.*

204040-013

Figure 13. SKYA21052 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKYA21052: 0.7 to 2.7 GHz SP12T Antenna Switch with MIPI Interface	SKYA21052	SKYA21052-EVB