MP3430

90V Step-Up Converter with APD Current Monitor

DESCRIPTION

The MP3430 is a monolithic step-up converter that integrates a power switch and a biased avalanche photodiode (APD) current monitor. The device can double the output voltage through the APD optical receivers. The MP3430 can provide up to 90V output.

The MP3430 uses a current-mode, fixed-frequency architecture to regulate the output voltage, which provides a fast transient response and cycle-by-cycle current limiting. The MP3430 features two accurate APD current monitoring outputs with 1:10 and 1:2 ratios, respectively. Resistor-adjustable current limiting protects the APD from optical power transients.

The MP3430 includes over-current and thermal-overload protection to prevent damage in the event of an output overload.

The MP3430 is available in a small 3mm×3mm QFN16 package.

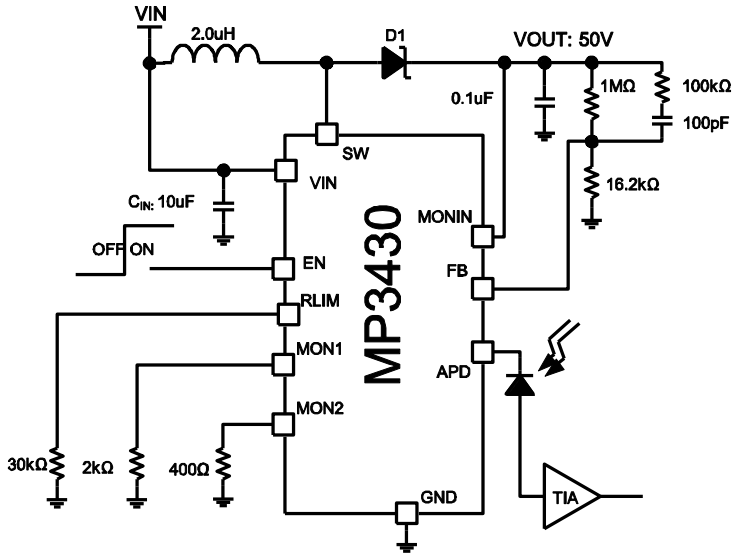
FEATURES

- 2.7V-to-5.5V Input Voltage
- 100V/1Ω NFET with 0.9A Limit
- Up to 90V Output Voltage
- 50ns APD Current Monitoring Response Speed
- 1.3MHz Fixed Switching Frequency
- Internal Compensation and Soft-Start
- High-Side APD Current Monitor with less than ±5% Tolerance.
- 1:10 and 1:2 Ratio Outputs for APD Current Monitoring
- Thermal-Shutdown Protection
- Programmable APD Over-Current Limit and Protection
- 3×3mm QFN16 Package

APPLICATIONS

- APD Biasing
- PIN Diode Biasing
- Optical Receivers and Modules
- Fiber-Optic–Network Equipment

TYPICAL APPLICATION

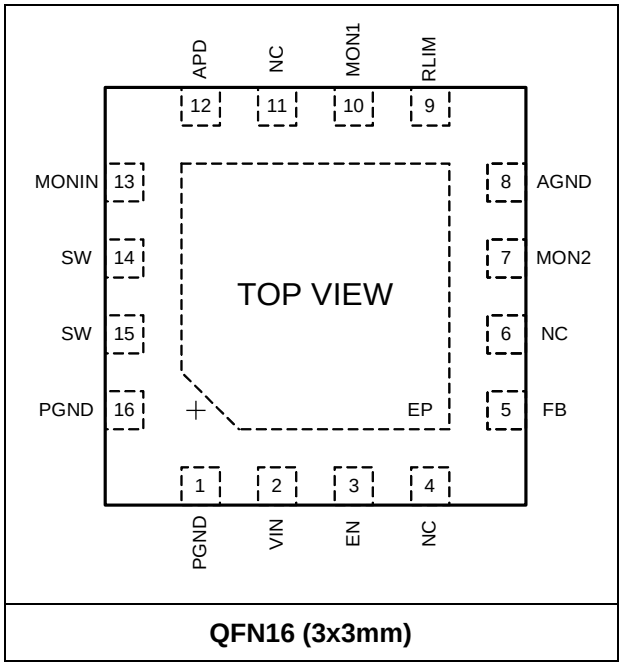


**ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3430GQ	QFN16 (3x3mm)	ACBY
MP3430HQ	QFN16 (3x3mm)	ACBY

* For Tape & Reel, add suffix –Z (e.g. MP3430GQ–Z).
For Tape & Reel, add suffix –Z (e.g. MP3430HQ–Z).
For RoHS Compliant Packaging, add suffix –LF (e.g. MP3430HQ–LF–Z)
**MPS is offering two different order codes, for this device we recommend MP3430HQ for our customers, both devices completely meet specifications

PACKAGE REFERENCE



QFN16 (3x3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage ..... -0.3V to 6.5V
MONIN, SW, APD Voltage..... -0.3V to 100V
EN, FB, RLIM ..... -0.3V to 6.5V
MON1, MON2..... -0.3V to4.5V
Continuous Power Dissipation (T_A = +25°C) (2)
.....2.1W

Recommended Operating Conditions (3)

Input Voltage ..... 2.7V to 5.5V
MON1, MON2..... 2.2V
MONIN, SW, APD Voltage..... 2.7V to 90V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN16 (3x3mm).....60 .....12 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

Parameters	Symbol	Condition	Min	Typ	Max	Units
Minimum Operating Voltage	$V_{IN\ MIN}$		2.7			V
Maximum Operating Voltage	$V_{IN\ MAX}$				5.5	V
Under-Voltage Lockout Threshold	V_{UVLO}		2.4	2.6	2.7	V
Under-Voltage Lockout Hysteresis	V_{UVLOH}			185		mV
EN Threshold		EN Rising	0.8		1.6	V
EN Hysteresis				150		mV
Feedback Voltage	V_{FB}		0.77	0.8	0.824	V
Feedback Line Regulator	R_{FBL}			0.043	0.12	%/V
FB-Pin Bias Current	I_{FBB}	V_{FB}=0.8V		30	100	nA
Supply Current	I_S	FB=1V, Not switching		0.3	1.0	mA
		V_{EN}=0		0.1	0.5	μA
Switching Frequency	f_S		1.0	1.3	1.55	MHz
Maximum Duty Cycle	D_{MAX}		76		97	%
Switch Current Limit	I_{SLMT}		0.6	0.9	1.3	A
Switch R_{DSon}	V_{CESAT}	I_{SW}=150mA	0.58	0.98	1.3	Ω
Switch Leakage Current	I_{SL}	SW=90V, EN=0			1.0	μA
EN Pin Pull-Down Current	I_{ENP}	EN=0V			0.2	μA
APD-Current–Monitor Output1 Gain	G_{CM1}	I_{APD}=250nA 10V≤MONIN≤90V	0.09	0.10	0.12	mA/mA
		I_{APD}=2.5mA 10V≤MONIN≤90V	0.095	0.10	0.105	
APD-Current–Monitor Output2 Gain	G_{CM2}	I_{APD}=250nA, 10V≤MONIN≤90V	0.45	0.5	0.6	mA/mA
		I_{APD}=2.5mA, 10V≤MONIN≤90V	0.475	0.5	0.53	
Monitor-Output1–Voltage Clamp	V_{MOC}	250nA<I_{APD}<2.5mA	2.2		3.5	V
Monitor-Output2–Voltage Clamp	V_{MOC}	250nA<I_{APD}<2.5mA	2.2		3.5	V
APD-Monitor–Voltage Drop	V_{ADP}	MONIN – ADP at I_{APD}=1mA, MONIN=40V	1.0	1.32	2.0	V
APD-Monitor-Current–Response Speed	t_{delay1}	10μA to 1mA step APD current input		50		ns
	t_{delay2}	250nA to 10μA step APD current input		7		μs
APD-Pin Current Limit	$I_{MONINLMT}$	APD=0V, MONIN=40V, R_{LIM}=16.9kΩ	2.5		4.3	mA
APD Current-Limit–Adjustment Range		R_{LIM}=27.2kΩ,, MONIN=10V,	2.25		3	mA
		R_{LIM}=137kΩ ,MONIN=10V	0.375		0.625	
		R_{LIM}=27.2kΩ,, MONIN=90V,	1.85		3	mA
		R_{LIM}=137kΩ ,MONIN=90V	0.36		0.72	mA
Thermal Shutdown				160		°C
Thermal Shutdown Hysteresis				10		°C

Notes:

5) The * denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A =+25°C. V_{IN}=3.3V, V_{EN}=3.3V unless otherwise noted.

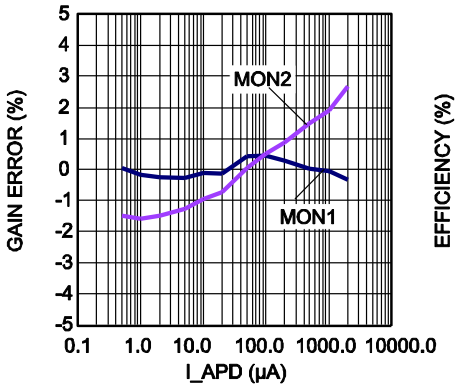
PIN FUNCTIONS

Pin #	Name	Description
1, 16	PGND	Power Ground. Pins connected internally. For best performance, connect both pins to board ground.
2	V_{IN}	Input Supply. Locally bypass this pin.
3	EN	Shutdown. Tie to 1.6V or higher to enable device; 0.6V or less to disable device.
4, 6, 11	NC	Not Connected.
5	FB	Feedback. Connect to the output-resistor–divider tap.
7	MON2	Current-Monitor Output. It sources a current equal to 50% of the APD current and converts to a reference voltage through an external resistor.
8	AGND	Analog Ground.
9	RLIM	Current-Limit Resistor. Connect a resistor from RLIM to GND to program the APD current-limit threshold.
10	MON1	Current-Monitor Output. It sources a current equal to 10% of the APD current and converts to a reference voltage through an external resistor.
12	APD	Connect to APD Cathode.
13	MONIN	Current-Monitor Power Supply. Connect an external low-pass filter to further reduce supply voltage ripple.
14, 15	SW	Switch. Minimize the trace length on this pin to reduce EMI.
	Exposed Pad	GND. Solder to a large copper plane on the PCB.

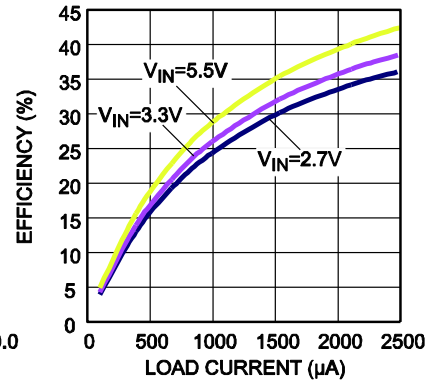
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 3.3V, V_{OUT} = 50V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

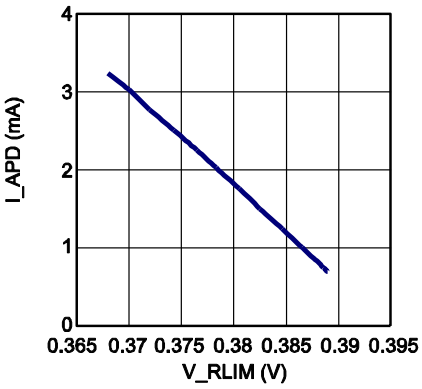
Gain Error vs. APD Current



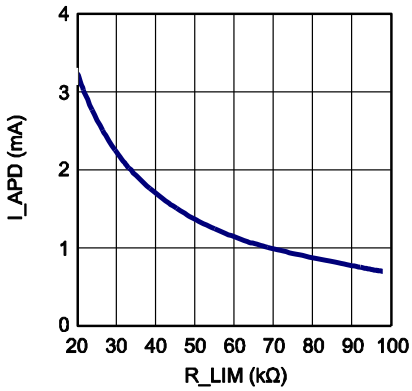
Efficiency vs. Load Current



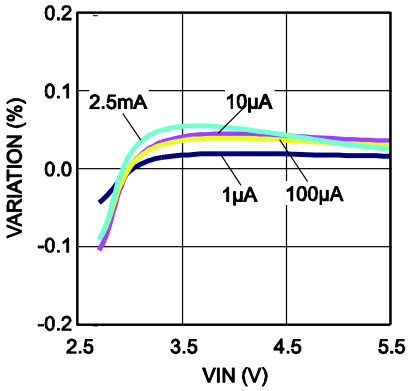
V-RLIM vs. APD Current Limit



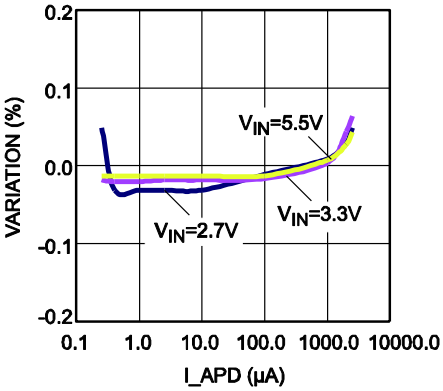
R_LIM vs. APD Current Limit



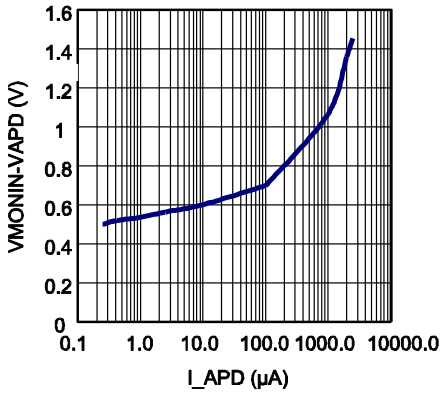
Line Regulation



Load Regulation



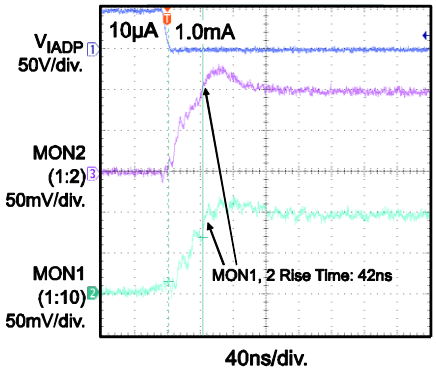
Voltage Drop - Vmonin to Vapd



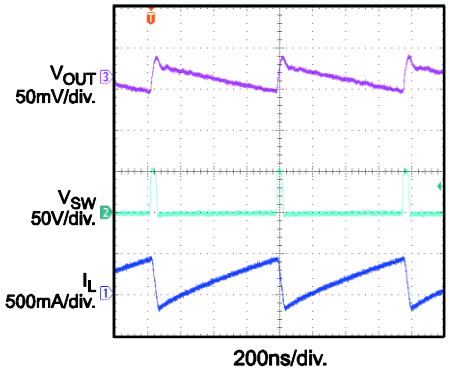
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN} = 3.3V, V_{OUT} = 50V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

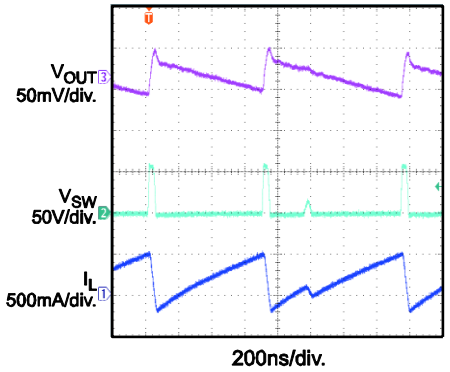
APD Monitor Current Response Speed – 10µA to 1mA Step
V_{IN} = 3.3V, V_{OUT} = 50V



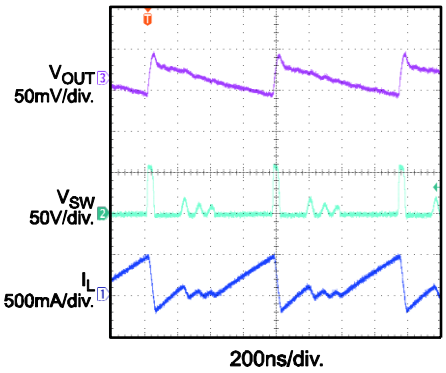
Steady State
I_{APD}=2mA, V_{IN} = 2.7V



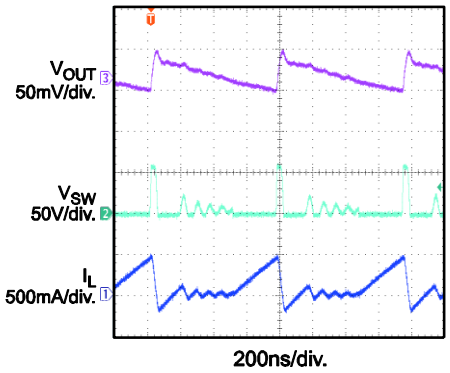
Steady State
I_{APD}=2mA, V_{IN} = 3.3V



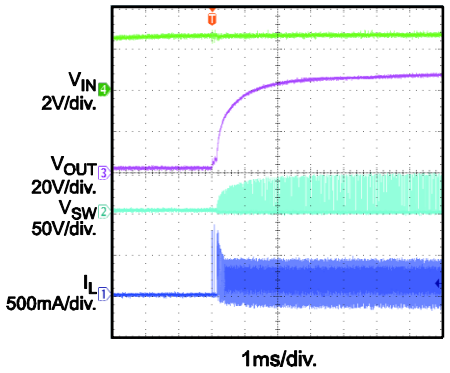
Steady State
I_{APD}=2mA, V_{IN} = 4.5V



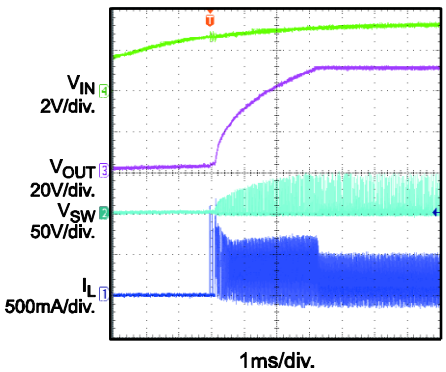
Steady State
I_{APD}=2mA, V_{IN} = 5.5V



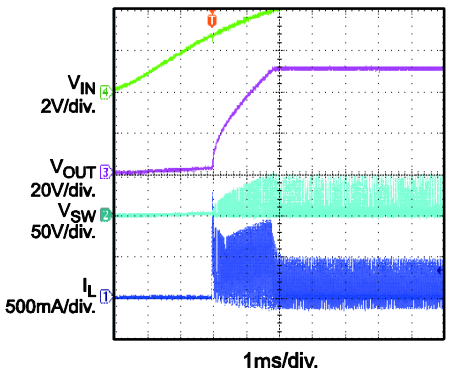
Power Start Up
I_{APD}=2.5mA, V_{IN} = 2.7V



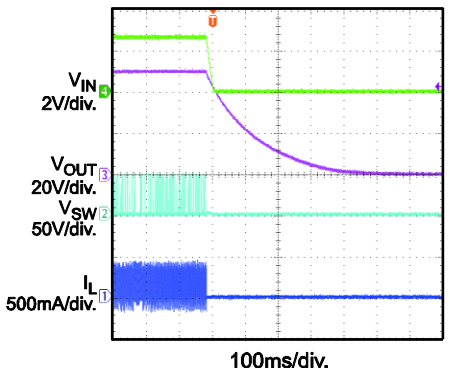
Power Start Up
I_{APD}=2.5mA, V_{IN} = 3.3V



Power Start Up
I_{APD}=2.5mA, V_{IN} = 5.5V



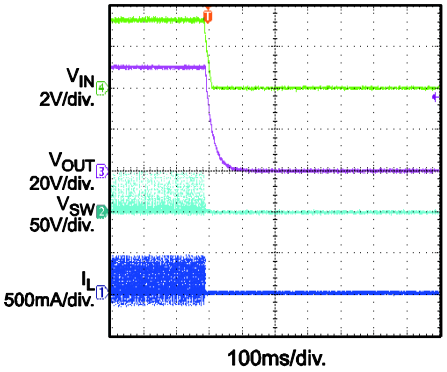
Power Shutdown
I_{APD}=2.5mA, V_{IN} = 2.7V



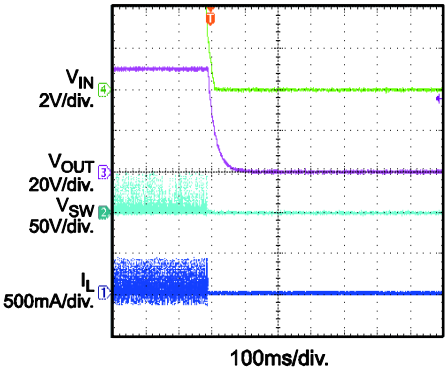
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 3.3V, V_{OUT} = 50V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

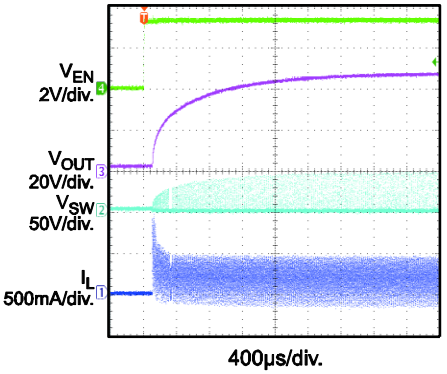
Power Shutdown
I_{APD}=2.5mA, V_{IN} = 3.3V



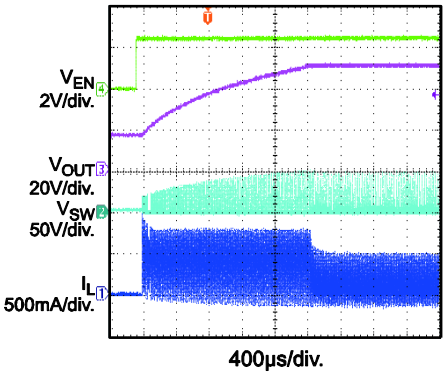
Power Shutdown
I_{APD}=2.5mA, V_{IN} = 5.5V



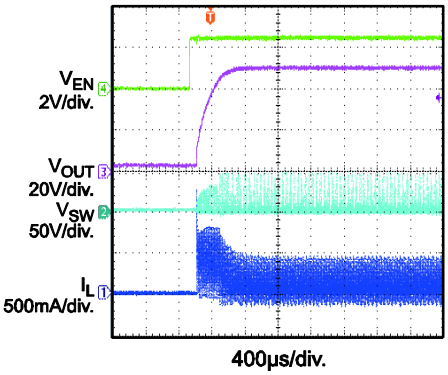
Enable Startup
I_{APD}=2.5mA, V_{IN} = 2.7V



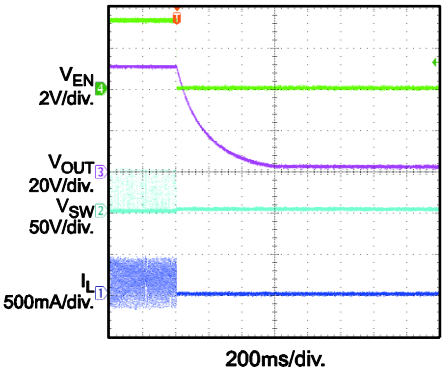
Enable Startup
I_{APD}=2.5mA, V_{IN} = 3.3V



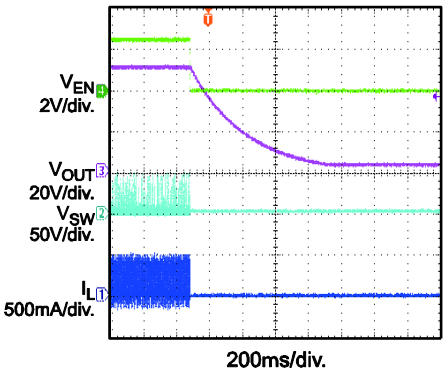
Enable Startup
I_{APD}=2.5mA, V_{IN} = 5.5V



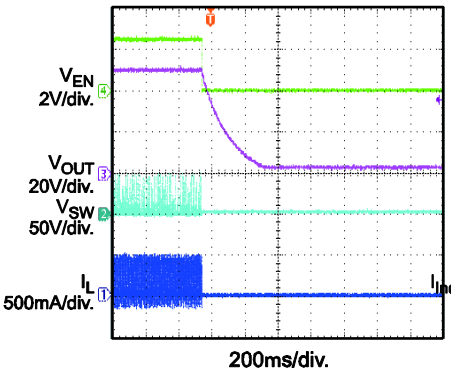
Enable Shutdown
I_{APD}=2.5mA, V_{IN} = 2.7V



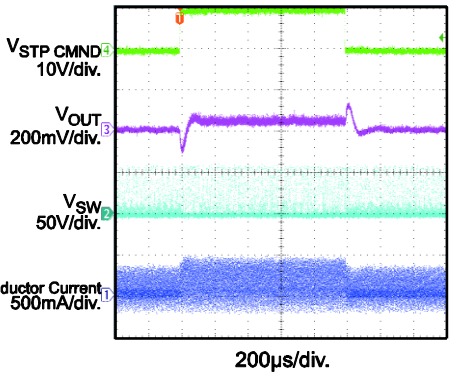
Enable Shutdown
I_{APD}=2.5mA, V_{IN} = 3.3V



Enable Shutdown
I_{APD}=2.5mA, V_{IN} = 5.5V



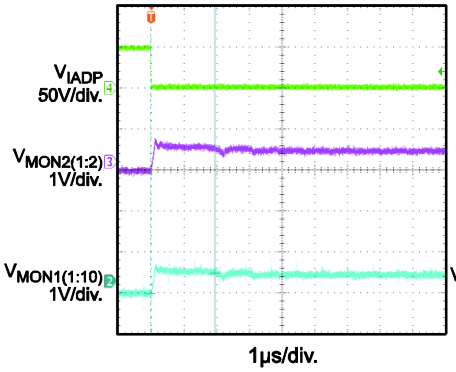
Transient Response
0.5mA to 2mA



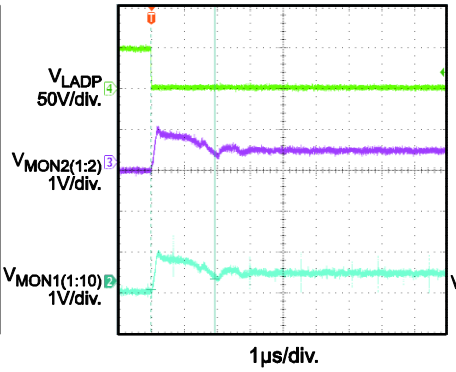
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 3.3V, V_{OUT} = 50V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

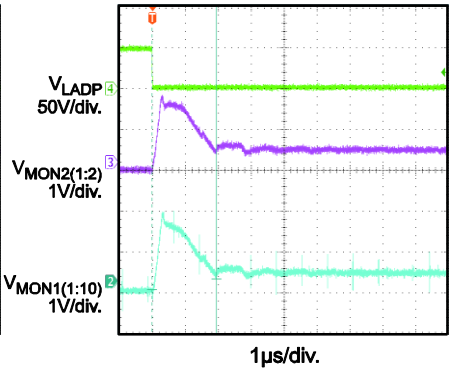
MON1,2 OCP Response - ILIM:2.5mA
0 to 3mA



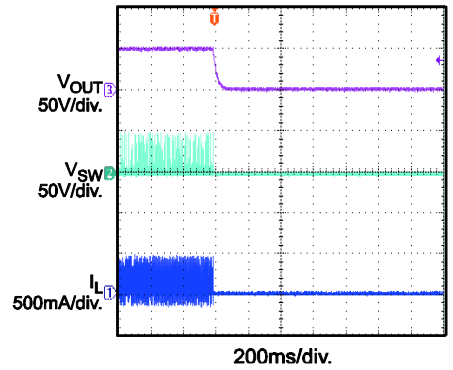
MON1,2 OCP Response - ILIM:2.5mA
0 to 5mA



MON1,2 OCP Response - ILIM:2.5mA
0 to 10mA



Temperature Shutdown @ 148°C



BLOCK DIAGRAM

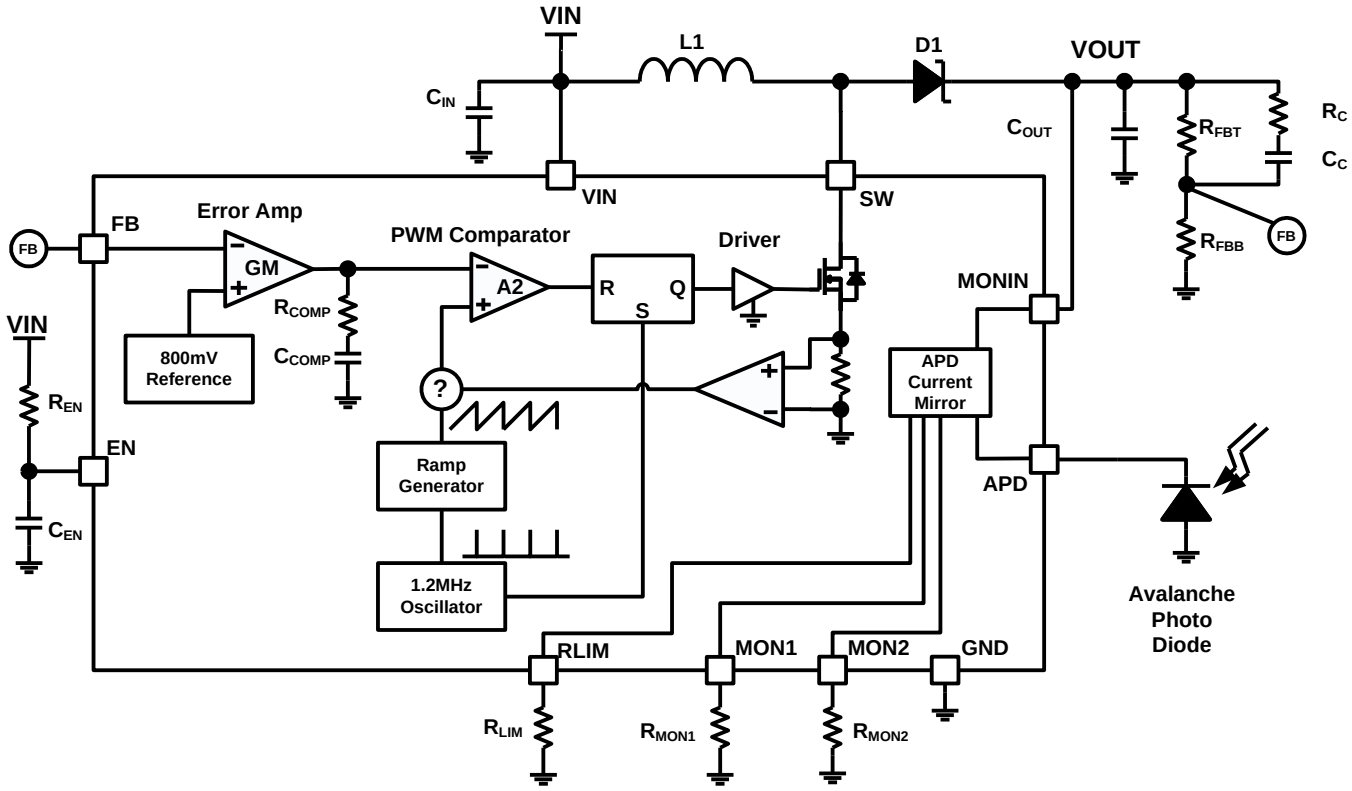


Figure 1: Functional Block Diagram

APPLICATION INFORMATION

The MP3430 step-up converter uses a constant-frequency, current-mode–control scheme to provide excellent line and load regulation.

At the start of each oscillator cycle, the RS latch is set, which turns on the power switch. The output of current sense amplifier—which is proportional to the switching current—is added to a generated ramp. The resulting sum is fed into the positive terminal of the PWM comparator. The RS latch resets, turning off the power switch as soon as the positive terminal exceeds the level of negative input of PWM comparator—which is proportional to the difference between the feedback voltage and the reference voltage. As the load varies, the error amplifier sets the switching peak current necessary to supply the load and regulate the output voltage.

MP3430 has an integrated high-side APD current monitor. The MON pin has an open-circuit protection feature and is internally clamped to 3V. MON1 and MON2 mirror the load current on the APD pin, and convert the currents to voltage signals through resistors R_{MON1} and R_{MON2}. The current mirror ratios are set to be 1:10 and 1:2. The APD output current has over-current protection with a threshold programmed by an external resistor at the RLIM pin.

APD Current-Limit Design

The current limit can be adjusted from 0.5mA to 2.5mA. The current limit is linear with respect to the voltage applied to the RLIM pin, where:

$$I_{\_RLIM}\,(mA) = -122 \times V_{\_RLIM} + 48$$

To program the voltage, connect a resistor from the RLIM pin to ground, where

$$R_{\_RLIM} = \frac{68}{I_{APD,MAX}}$$

$R_{\_RLIM}$ units: kΩ

$I_{\_RLIM}$ units: mA

EN Design

Add a delay (typ. 1ms) to the EN pin so V_{IN} can increase well beyond the UVLO value (typ. 2.6V) before the MP3430 turns on. For most applications, connect a 100kΩ resistor from V_{IN} to EN and a 10nF capacitor from EN to GND.

Soft-Start

There is no need for a soft-start because V_{OUT} rises very slowly—on the order of ms. The portion of the inductor current that actually drives up the output voltage is small due to the high conversion ratio. The inductor current limit (typ. 900mA), the output capacitor (typ. 0.1µF), and V_{IN} limit the V_{OUT} rise time.

Component Design

V_{OUT} Programming

A resistor feedback network programs the output voltage. Typically, the top resistor—from V_{OUT} to V_{FB} —is 1MΩ. The bottom resistor—from V_{FB} to GND—is:

$$R_{BOTTOM} = R_{TOP} \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$$

R_{TOP}: kΩ

R_{BOTTOM}: kΩ

In addition, place a series resistor and capacitor of 100kΩ and 100pF, respectively, in parallel with R_{TOP}. This gives a phase boost for good phase margin as well as decreases the gain for good gain margin in the extreme cases of V_{IN} and V_{OUT}.

Inductor Design

There are three main considerations in inductor design:

1. Design "$D3*t_S$" to be long enough for the reverse-inductor current to stop
2. Must always stay in discontinuous conduction mode (DCM)
3. The peak inductor current must be less than the current limit of the MP3430 and the saturation current of the inductor.

Design $D3 \times t_s$ to be Long Enough for the Reverse-Inductor Current to Stop

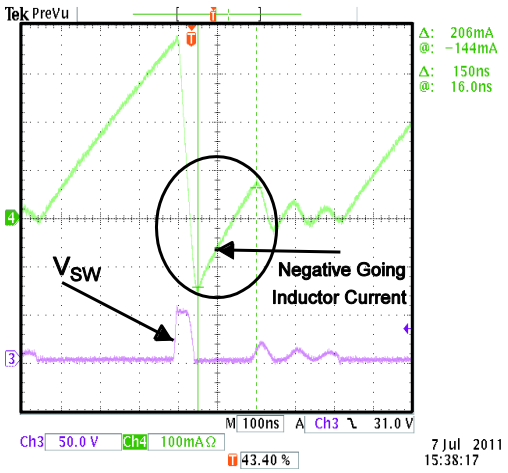
In DCM mode there are three modes:

$D_1 \times t_S$: the switch is closed and current builds in the inductor,

$D_2 \times t_S$: when the built-up current transfers to C_{OUT}

$D_3 \times t_S$: the L current reverses due to energy in the SW MOSFET capacitor followed by LC ringing.

There is a “reverse current” – current going from the SW node back into V_{IN} – during D_3.



Due to the applied high-output voltage on the switch node combined with the C_{DS} capacitive coupling of the MP3430 FET, a significant reverse current flows through the inductor during the D_3 period.

The energy stored in C_{DS} transfers to the inductor. This negative inductor current turns the FET body diode on. V_{IN} (combined with the negative voltage applied by the conducting body diode to the SW node) causes the inductor current to ramp up from the maximum negative going current to about 60% of that magnitude in the positive direction—where the positive current goes from V_{IN} to the SW node, and the negative current feeds back into V_{IN} through the inductor.

Ringing current occurs after the current turns off the body diode. D_3 is always greater than the time for the current to turn off the FET body diode and to start ringing. Determine D_3 as per the following equations:

$$I_{MAX,REVERSE} = V_{OUT} \times \sqrt{\frac{40pF}{L}}$$

$$t_{ReverseCurrent} \cong \frac{1.6 \cdot L \cdot I_{MAX,REVERSE}}{V_{IN,MIN} + 1}$$

$$D_1 = 2.2\sqrt{\frac{K}{4}\left[\left(\frac{2V_{OUT}}{V_{IN}} - 1\right)^2 - 1\right]}$$

$$D_2 = \frac{D_1 \times V_{IN}}{V_{OUT} - V_{IN}}$$

$$D_3 = 1 - D_1 - D_2$$

$$D_3 \times t_s \geq t_{ReverseCurrent}$$

Where, $K = \frac{2 \times L \times f_S \times I_{OUT}}{V_{OUT} \times 1000}$,

V_{OUT}: V, L: µH, f_S: MHz, I_{OUT}: mA

Staying in Discontinuous Conduction Mode (DCM)

The system must operate in discontinuous conduction mode (DCM) to maintain stability due to the high conversion ratio from VIN to VOUT. A boost converter has a right-hand zero that can cause system instability if that zero moves into the system’s operational-frequency range. Furthermore the right hand zero moves into lower frequencies—where the system operates—as the conversion ratio increases. This right-hand zero does not exist when operating in DCM

Stability therefore requires that the system operates in DCM under all conditions. To this end, a dimensionless parameter called K measures a system’s tendency to operate in DCM mode. The other parameter is K_{CRIT} which is the DCM, CCM (continuous conduction mode) system boundary. If $K<K_{CRIT}$, then the system is in DCM mode operation.

$$K_{CRIT} = D_{CCM} \times \left(D'_{CCM}\right)^2 = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2$$

$$K = \frac{2 \times L \times f_S \times I_{OUT}}{V_{OUT} \times 1000}$$

DCM Mode: $K < K_{CRIT}$:

$$L \leq \frac{K_{CRIT} \times V_{OUT} \times 1000}{2 \times f_S \times I_{OUT}}$$

V_{IN}, V_{OUT}: V

L: µH

f_S: MHz

I_{OUT}: mA

There is a size limit to the inductor that can cause the system to enter CCM mode and risk instability.

The peak inductor current must always be less than the MP3430 current limit and the inductor saturation current.

In addition, chose an inductor such that the saturation current is greater than either the IC current limit (900mA, typ.) or the worst-case calculated peak current—whichever is smaller. Generally, pick an inductor with at least 20% greater saturation current than the IC current limit, so that the minimum saturation current would be 1.08A (900mA + 180mA). To ensure that the calculated maximum current does not exceed the maximum current allowed by the MP3430.

$$I_{L,PEAK} = \frac{V_{IN} \times D_1}{L \times f_S} < 900mA \text{ , typical}$$

Diode Design

Due to the high-output voltage combined with the diode capacitive coupling, there is a significant reverse current through the inductor. Generally, a low reverse bias capacitance equates to a low reverse inductor current. However, this is not always true though; so test the diodes prior to final selection. Two recommended diodes with relatively small reverse currents are the DFLS1150-7 (Diodes Inc, Schottky, 1A (avg), 150V) and the BAT46ZFILM (STMicroelectronics, Schottky, 150mA (avg), 100V)

Also, select a diode with an RMS current rating greater than the actual RMS current. The maximum RMS current occurs when V_{IN} is minimal (2.7V). The RMS current equation is:

$$I_{DIODE,RMS} \geq I_{RMS} = I_{PK} \times \sqrt{\frac{D_2}{3}}$$

D_2 = fractional diode conduction period:

$$D_2 = \frac{D_1 \times V_{IN}}{V_{OUT} - V_{IN}}$$

I_{DIODE}, I_{PK}: mA

R_{MON1}, R_{MON2} Design

The maximum allowed voltage on either R_{MON1} or R_{MON2} is 2.5V (typ). The maximum allowed current is 2.5mA (typ). For faster response, chose the maximum output less than the maximum allowed voltage.

$$I_{MON1,MAX} = \frac{I_{APD,MAX}}{10}$$

$$I_{MON2,MAX} = \frac{I_{APD,MAX}}{2}$$

$$R_{MON1} = \frac{V_{MON1,MAX}}{I_{MON1,MAX}}$$

$$R_{MON2} = \frac{V_{MON2,MAX}}{I_{MON2,MAX}}$$

Where:

$V_{MON1,MAX}$, $V_{MON2,MAX}$ < 2.5V

$R_{MON1,2}$: kΩ

$I_{MON1,2}$: mA

C_{OUT} Design

The output ripple is typically 0.1%. Use 0.1µF capacitor for most cases. Make sure that the capacitor voltage rating is at least 50% more than V_{OUT}. The ripple equation is:

$$V_{OUT,RIPPLE} = \frac{I_{APD} \times (1 - D_2)}{f_S \times C_{OUT}} \times 0.001$$

I_{APD}: mA

f_S: MHz

C_{OUT} µF

C_{IN} Design

If the C_{IN} is not big enough, the initial current pulses will pull V_{IN} down below UVLO during power start-up. This may cause false starts. Select a C_{IN} of at least 10µF.

Recommended Values (V_{IN}: 2.7V to 5.5V)

V_{OUT} (V)	$I_{OUT,MAX}$ (mA)	L (µH)	$R_{FB,TOP}$ (MΩ) (V_{OUT} to FB)	$R_{FB,BOTTOM}$ (kΩ) (FB to GND)	Diode (Schottky Small Signal)	C_{OUT} (µF 100V)	C_{IN} (µF)
30	2.5	3.3	1.0	27.4	BAT46W	0.1	10
40	2.5	2.7		20.5			
50	2.5	2.0		16.2			
60	2.0	1.5		13.3			
70	0.9	1.5		11.5			
80	0.5	1.2		10.0			
90	0.5	1.0		8.87			

Design Example:

Desired Parameters:

V_{IN} = 2.7V to 5.5V
$V_{IN,TYP}$ = 3.3V
V_{OUT} = 50V
V_{FB} = 0.8V
f_S = 1.3MHz;
$I_{APD,MAX}$ = 2.5mA
$V_{MON1,MAX}$ = 0.5V
$V_{MON2,MAX}$ = 0.5V
R_{TOP} = 1MΩ
t_S = 769ns

Calculations:

V_{OUT}

$$R_{BOTTOM} = R_{TOP} \times \frac{V_{FB}}{V_{OUT} - V_{FB}} = 1M\Omega \times \frac{0.8}{50 - 0.8} = 16.2k\Omega$$

$R_{\_RLIM}$ = 68 / $I_{APD,MAX}$ = 68/2.5-= 27.2kΩ

Inductor

Choose L = 2.0µH

First Consideration (most important)

$$I_{MAX,REVERSE} = V_{OUT} \times \sqrt{40pF/L} = 50 \times \sqrt{40pF/2\mu H} = 224mA$$

$$t_{ReverseCurrent} \cong \frac{1.6 \cdot L \cdot I_{MAX,REVERSE}}{V_{IN,MIN} + 1} = \frac{1.6 \times 2\mu H \times 224mA}{2.7 + 1} = 194ns$$

$$K = \frac{2 \times L \times f_S \times I_{OUT}}{V_{OUT} \times 1000} = \frac{2 \times 2 \times 1.3 \times 2.5}{50 \times 1000} = 0.00026$$

$$D_1 = 2.2\sqrt{\frac{K}{4}\left[\left(\frac{2V_{OUT}}{V_{IN,MIN}} - 1\right)^2 - 1\right]} = 2.2\sqrt{\frac{0.00026}{4}\left[\left(\frac{2 \times 50}{2.7} - 1\right)^2 - 1\right]}$$

$$= 0.639$$

$$D_2 = D_1 \frac{V_{IN}}{V_{OUT} - V_{IN,MIN}} = 0.639 \times \frac{2.7}{50 - 2.7} = 0.0365$$

$$D_3 = 1 - D_1 - D_2 = 1 - 0.639 - 0.0365 = 0.325$$

$$D_3 \times t_S = 250ns > t_{ReverseCurrent} = 194ns$$

So 2.0µH is good.

Second Consideration

$$K_{CRIT} = D \times D'^2 = \left(1 - \frac{V_{IN,MIN}}{V_{OUT}}\right) \times \left(\frac{V_{IN,MIN}}{V_{OUT}}\right)^2$$

$$= \left(1 - \frac{2.7}{50}\right) \times \left(\frac{2.7}{50}\right)^2 = 0.00276$$

$$L < \frac{K_{CRIT,MIN} \times V_{OUT} \times 1000}{2f_S \times I_{OUT}} = \frac{0.00276 \times 50 \times 1000}{2 \times 1.3 \times 2.5} = 21\mu H$$

K_{CRIT}>K : 0.00276>0.00026.

Third Consideration:

$$I_{L,PEAK} = \frac{V_{IN,MIN} \times D_1}{L \times f_S} = \frac{2.7 \times 0.639}{2.0 \times 1.3} = 664mA < 900mA$$

Make sure the inductor has at least 20% more capability than the saturation current

DIODE

D_2 = diode conduction fraction of period = 0.0365

$$I_{DIODE,RMS} > I_{RMS} = I_{PK}\sqrt{\frac{D_2}{3}} = 664 \times \sqrt{\frac{0.0365}{3}} = 73mA$$

Make sure diode average current rating is above this value

Output Capacitor

Choose C_{OUT} = 0.1µF

$$V_{OUT,RIPPLE} = \frac{I_{APD} \times (1 - D_2)}{f_S \times C_{OUT}} \times 0.001$$

$$= \frac{2.5 \times (1 - 0.0365)}{1.3 \times 0.1} \times 0.001 = 19mV$$

= 0.04% of V_{OUT} ,<0.1%

Monitor Resistors

Select $V_{MON1} = V_{MON2} = 0.5V<2.5V$

$R_{MON1} = V_{MON1} / I_{MON1,MAX} = 0.5/0.25 = 2\ k\Omega$

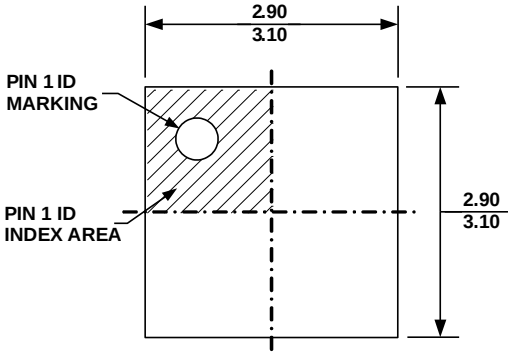
$R_{MON2} = V_{MON2} / I_{MON2,MAX} = 0.5/1.25 = 400\ \Omega$

Input Capacitors

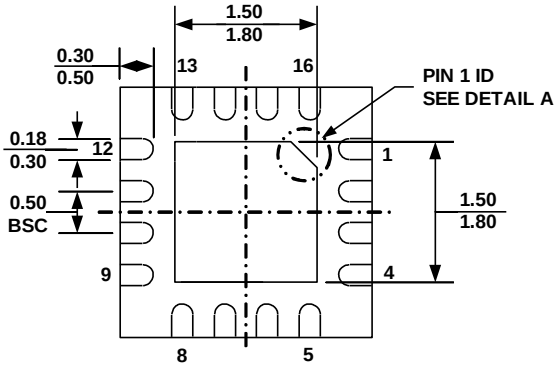
Choose $C_{IN} = 10\mu F$

PACKAGE INFORMATION

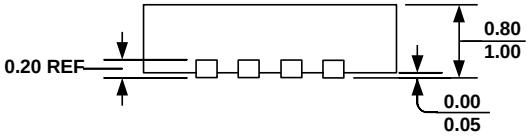
QFN16 (3X3mm)



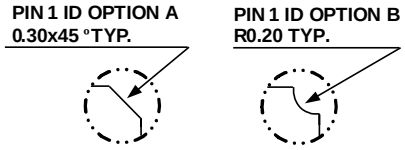
TOP VIEW



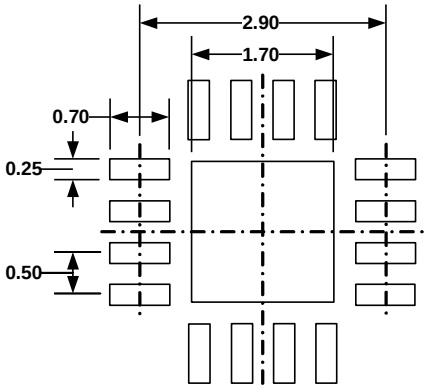
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VEED-4.
5) DRAWING IS NOT TO SCALE