

DMP2123L

P-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR



Features

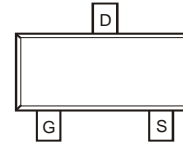
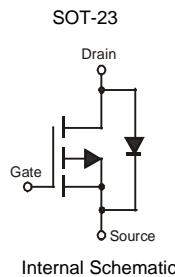
- Low $R_{DS(ON)}$:
 - 72 m Ω @ $V_{GS} = -4.5V$
 - 108 m Ω @ $V_{GS} = -2.7V$
 - 123 m Ω @ $V_{GS} = -2.5V$
- Low Input/Output Leakage
- **Lead Free By Design/RoHS Compliant (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **"Green" Device (Note 4)**

Mechanical Data

- Case: SOT-23
- Case Material - Molded Plastic, "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminals: Finish - Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram Below
- Weight: 0.008 grams (approximate)



TOP VIEW



TOP VIEW

Maximum Ratings @ $T_A = 25^\circ C$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Drain Current (Note 1) Continuous	I_D	$T_A = 25^\circ C$	-3.0
		$T_A = 70^\circ C$	-2.4
Pulsed Drain Current (Note 2)	I_{DM}	-15	A
Body-Diode Continuous Current (Note 1)	I_S	2.0	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 1)	P_D	1.4	W
Thermal Resistance, Junction to Ambient (Note 1); Steady-State	$R_{\theta JA}$	90	$^\circ C/W$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

- Notes:
1. Device mounted on 1"x1", FR-4 PC board with 2 oz. Copper and test pulse width $t \leq 10s$.
 2. Repetitive Rating, pulse width limited by junction temperature.
 3. No purposefully added lead.

DMP2123L

P-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR



Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV _{DSS}	-20	—	—	V	I _D = -250μA, V _{GS} = 0V
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1	μA	V _{DS} = -20V, V _{GS} = 0V
Gate-Body Leakage Current	I _{GSS}	—	—	±100	nA	V _{DS} = 0V, V _{GS} = ±12V
Gate Threshold Voltage	V _{GS(th)}	-0.6	—	-1.25	V	V _{DS} = V _{GS} , I _D = -250μA
On State Drain Current (Note 5)	I _{D(ON)}	-15	—	—	A	V _{GS} = -4.5V, V _{DS} = -5V
Static Drain-Source On-Resistance (Note 5)	R _{DS(ON)}	—	51 87 99	72 108 123	mΩ	V _{GS} = -4.5V, I _D = -3.5A V _{GS} = -2.7V, I _D = -3.0A V _{GS} = -2.5V, I _D = -2.6A
Forward Transconductance (Note 5)	g _{FS}	—	7.3	—	S	V _{DS} = -10V, I _D = -3.0A
Diode Forward Voltage (Note 5)	V _{SD}	—	0.79	-1.26	V	I _S = -1.7A, V _{GS} = 0V
Maximum Body-Diode Continuous Current (Note 1)	I _S	—	—	1.7	A	—
DYNAMIC PARAMETERS (Note 6)						
Total Gate Charge	Q _g	—	7.3	—	nC	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -3.0A
Gate-Source Charge	Q _{gs}	—	2.0	—	nC	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -3.0A
Gate-Drain Charge	Q _{gd}	—	1.9	—	nC	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -3.0A
Turn-On Delay Time	t _{D(on)}	—	12	—	ns	V _{DS} = -10V, V _{GS} = -4.5V, R _L = 10Ω, R _G = 6Ω
Turn-On Rise Time	t _r	—	20	—	ns	
Turn-Off Delay Time	t _{D(off)}	—	38	—	ns	
Turn-Off Fall Time	t _f	—	41	—	ns	
Input Capacitance	C _{iss}	—	443	—	pF	V _{DS} = -16V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	—	128	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	101	—	pF	

Notes: 4. Test pulse width t = 300μs.
5. Guaranteed by design. Not subject to production testing.