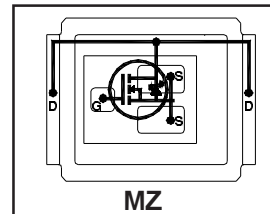


**Features**

- Latest MOSFET Silicon technology
- Key parameters optimized for Class-D audio amplifier applications
- Low  $R_{DS(on)}$  for improved efficiency
- Low  $Q_g$  for better THD and improved efficiency
- Low  $Q_{rr}$  for better THD and lower EMI
- Low package stray inductance for reduced ringing and lower EMI
- Can deliver up to 250W per channel into 4Ω Load in Half-Bridge Configuration Amplifier
- Dual sided cooling compatible
- Compatible with existing surface mount technologies
- RoHS compliant containing no lead or bromide
- Lead-Free (Qualified up to 260°C Reflow)

Key Parameters		
$V_{DS}$	150	V
$R_{DS(on)}$ typ. @ $V_{GS} = 10V$	47	mΩ
$Q_g$ typ.	25.0	nC
$R_{G(int)}$ max.	3.0	Ω



Applicable DirectFET Outline and Substrate Outline (see p. 6, 7 for details)

SQ	SX	ST	SH	MQ	MX	MT	MN	<b>MZ</b>		
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**Description**

This Digital Audio MOSFET is specifically designed for Class-D audio amplifier applications. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, gate charge, body-diode reverse recovery and internal gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD, and EMI.

The IRF6775MPbF device utilizes DirectFET™ packaging technology. DirectFET™ packaging technology offers lower parasitic inductance and resistance when compared to conventional wirebonded SOIC packaging. Lower inductance improves EMI performance by reducing the voltage ringing that accompanies fast current transients. The DirectFET™ package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing method and processes. The DirectFET™ package also allows dual sided cooling to maximize thermal transfer in power systems, improving thermal resistance and power dissipation. These features combine to make this MOSFET a highly efficient, robust and reliable device for Class-D audio amplifier applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	150	V
$V_{GS}$	Gate-to-Source Voltage	± 20	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	28	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.9	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.9	
$I_{DM}$	Pulsed Drain Current ①	39	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	89	W
$P_D @ T_A = 25^\circ C$	Power Dissipation ③	2.8	
$P_D @ T_A = 70^\circ C$	Power Dissipation ③	1.8	
$E_{AS}$	Single Pulse Avalanche Energy②	33	mJ
$I_{AR}$	Avalanche Current ①	5.6	A
	Linear Derating Factor ③	0.022	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-40 to + 150	°C

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③④	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑥④	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦④	20	—	
$R_{\theta JC}$	Junction-to-Case ③④	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.4	—	

Notes ① through ④ are on page 2

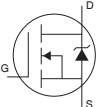
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	150	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	47	56	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.6A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 120V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G(int)</sub>	Internal Gate Resistance	—	—	3.0	Ω	

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	11	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 5.6A
Q <sub>g</sub>	Total Gate Charge	—	25	36		V <sub>DS</sub> = 75V V <sub>GS</sub> = 10V I <sub>D</sub> = 5.6A See Fig. 6 and 17
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	5.8	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	1.4	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	6.6	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	11	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	8.0	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	5.9	—		V <sub>DD</sub> = 75V I <sub>D</sub> = 5.6A R <sub>G</sub> = 6.0Ω V <sub>GS</sub> = 10V ④
t <sub>r</sub>	Rise Time	—	7.8	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	5.8	—		
t <sub>f</sub>	Fall Time	—	15	—		
C <sub>iss</sub>	Input Capacitance	—	1411	—		V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 120V, f = 1.0MHz V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 120V ⑤
C <sub>oss</sub>	Output Capacitance	—	193	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	40	—		
C <sub>oss</sub>	Output Capacitance	—	1557	—		
C <sub>oss</sub>	Output Capacitance	—	93	—		
C <sub>oss</sub> eff.	Effective Output Capacitance	—	175	—		

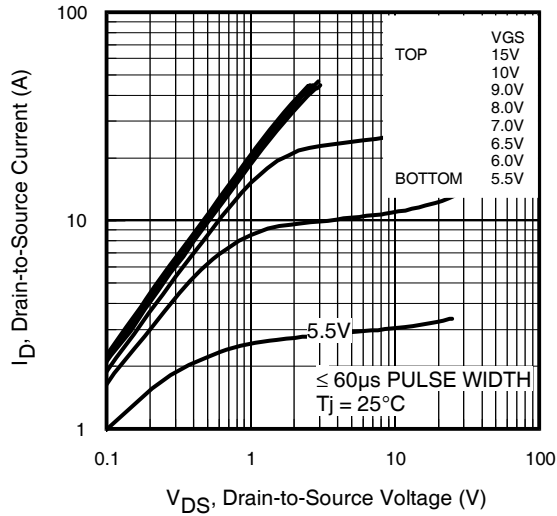
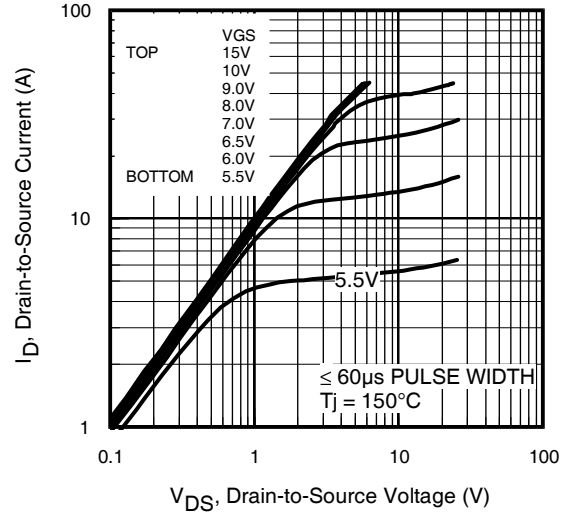
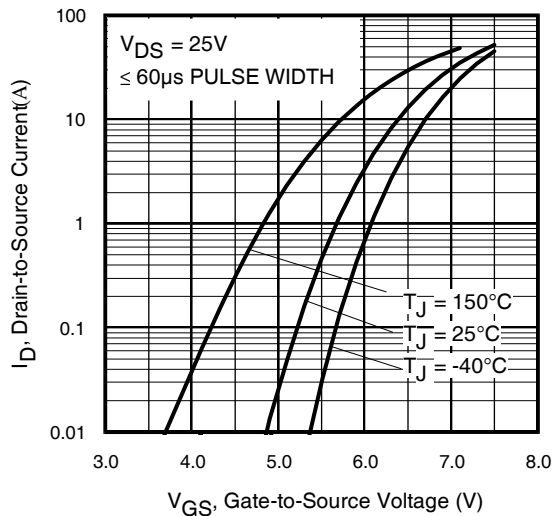
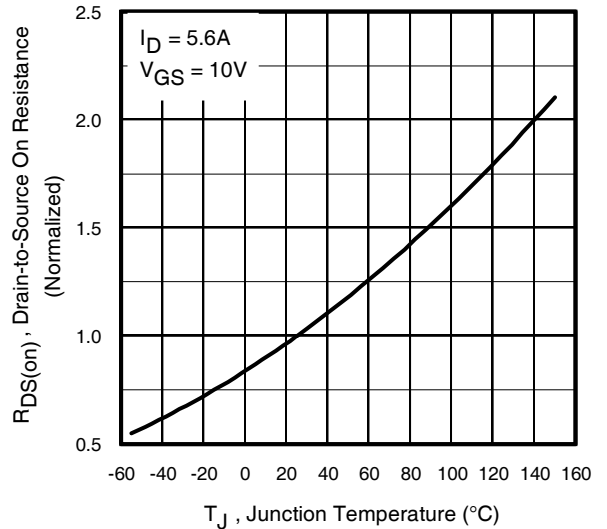
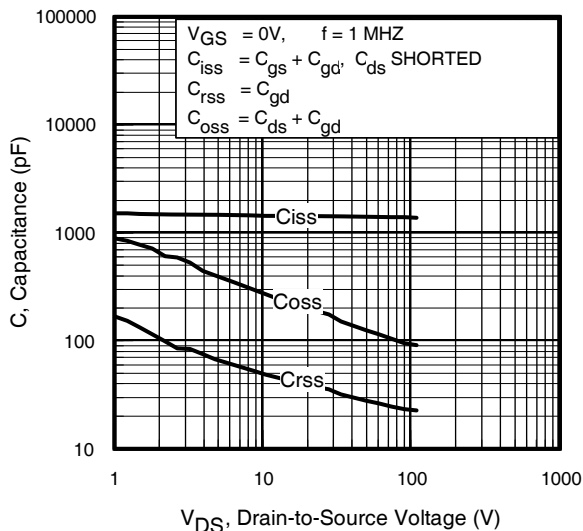
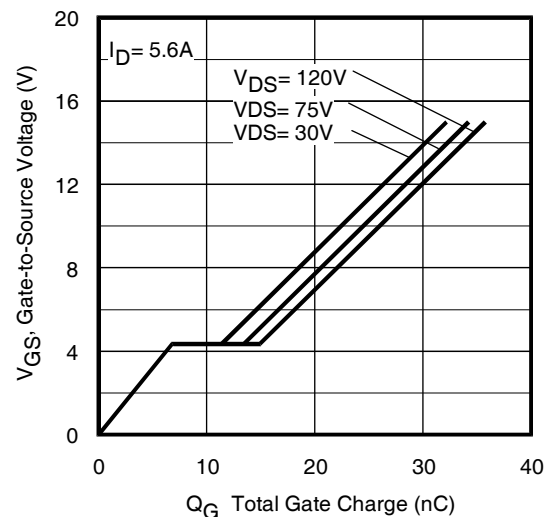
**Diode Characteristics**

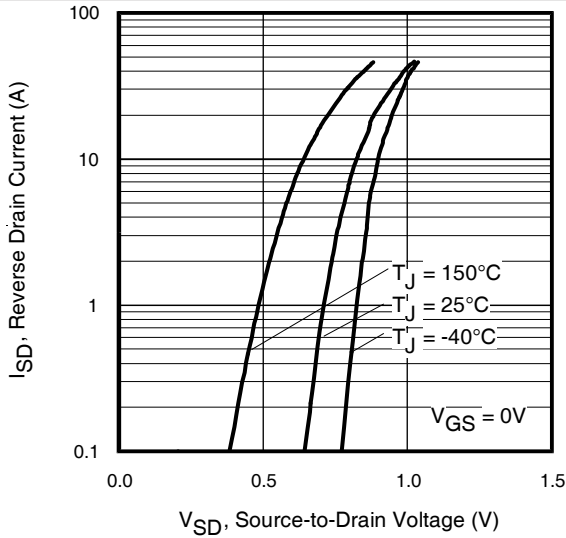
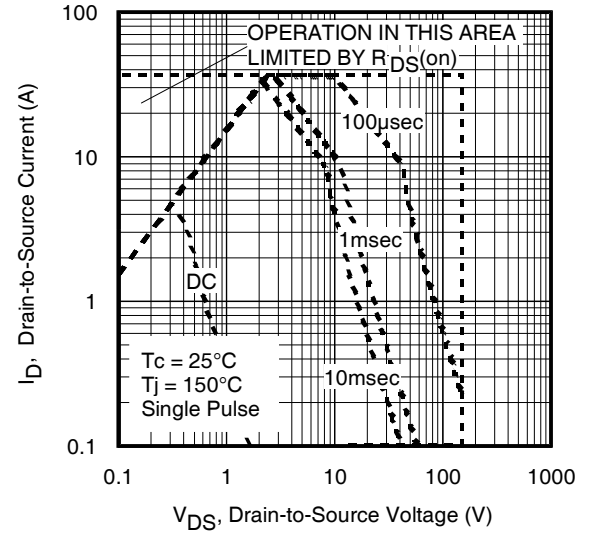
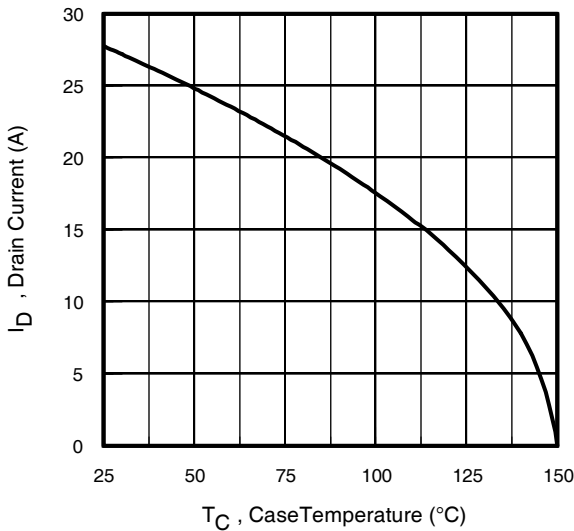
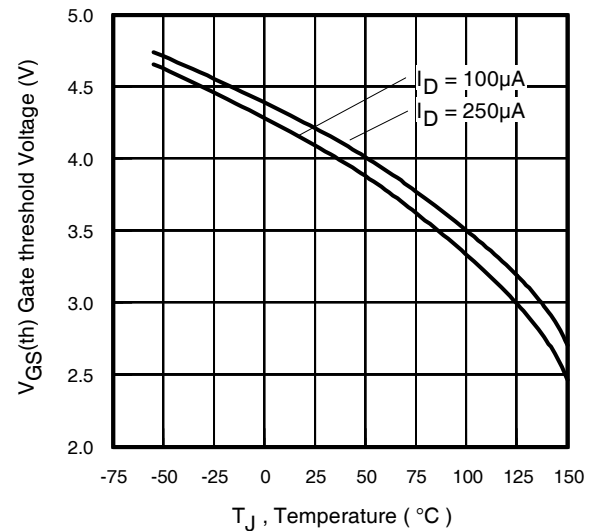
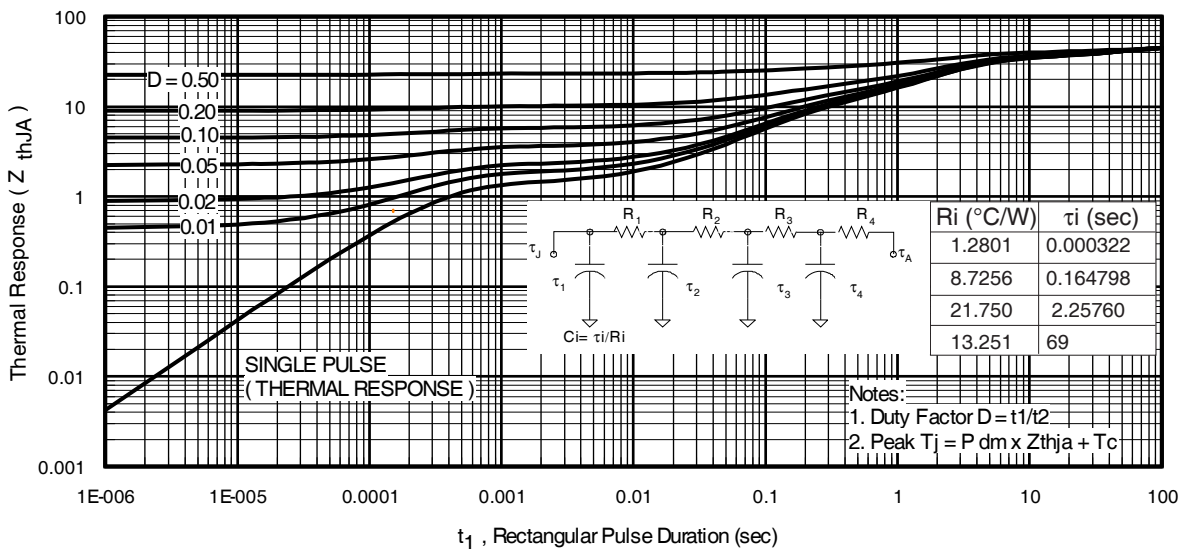
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	28	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	39		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 5.6A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	62	—	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 5.6A, V <sub>DD</sub> = 25V
Q <sub>rr</sub>	Reverse Recovery Charge	—	164	—	nC	di/dt = 100A/μs ④

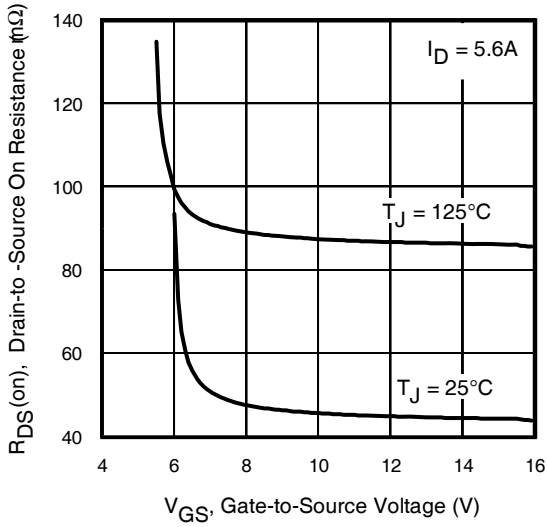
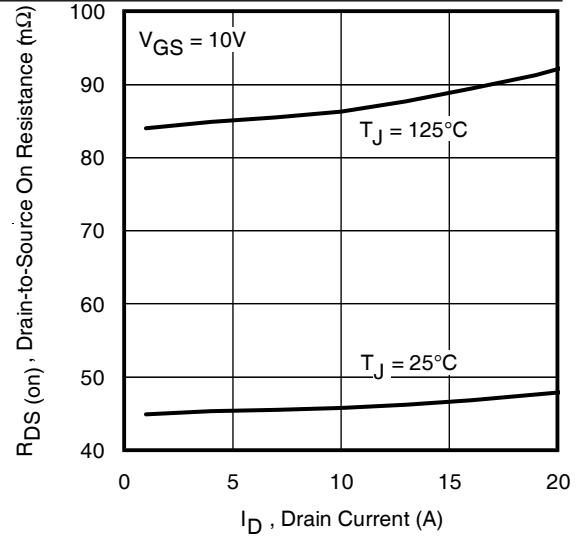
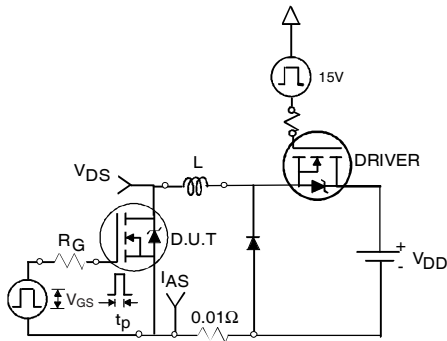
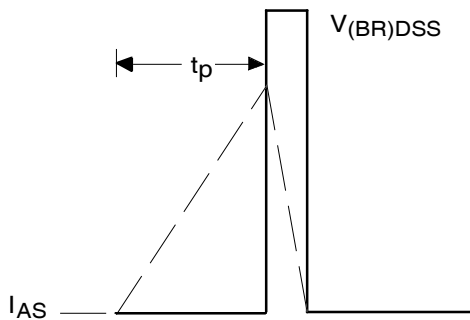
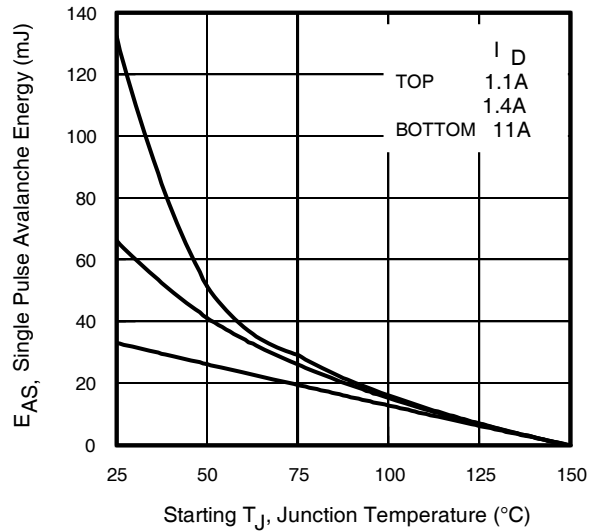
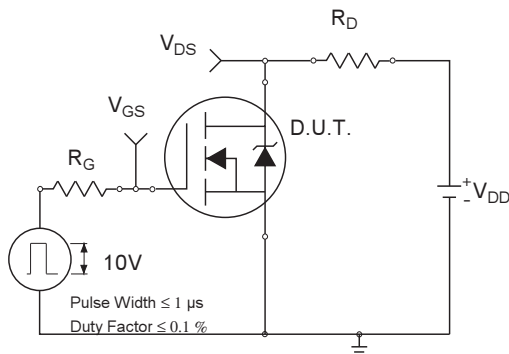
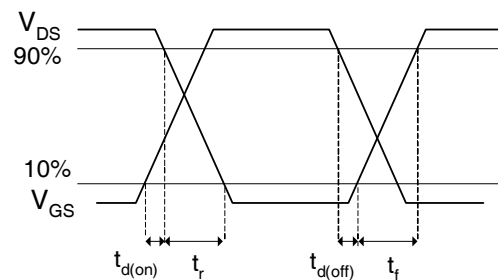
**Notes:**

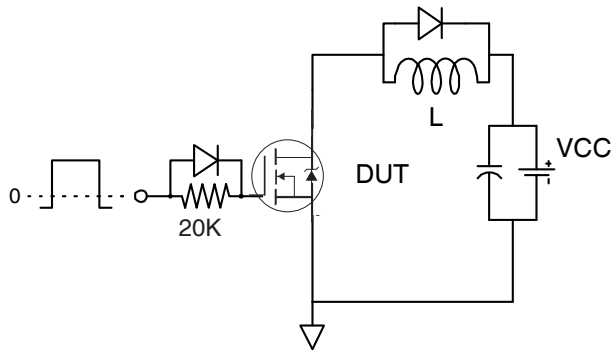
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T<sub>J</sub> = 25°C, L = 0.53mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 11.2A.
- ③ Surface mounted on 1 in. square Cu board.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss</sub> eff. is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.

- ⑥ Used double sided cooling, mounting pad with large heatsink.
- ⑦ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑧ T<sub>C</sub> measured with thermal couple mounted to top (Drain) of part.
- ⑨ R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.

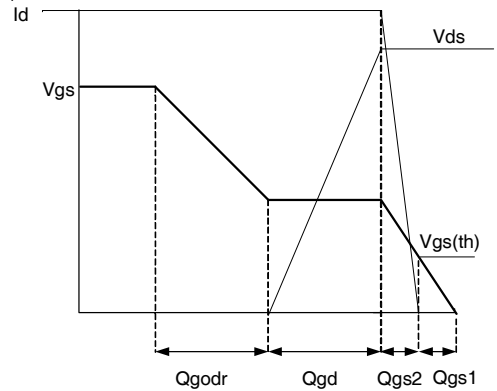

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Threshold Voltage vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ©

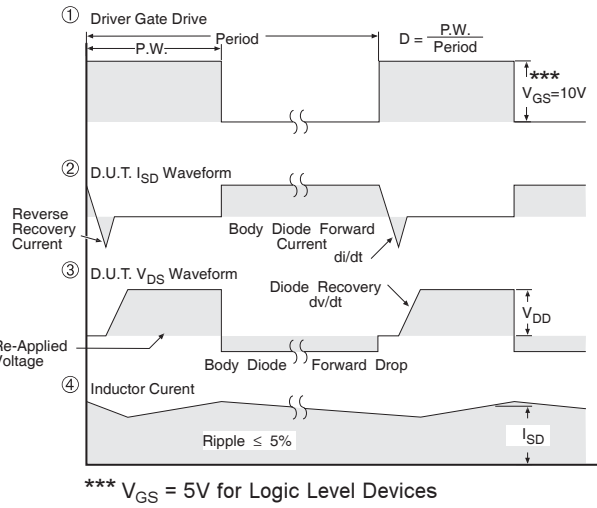
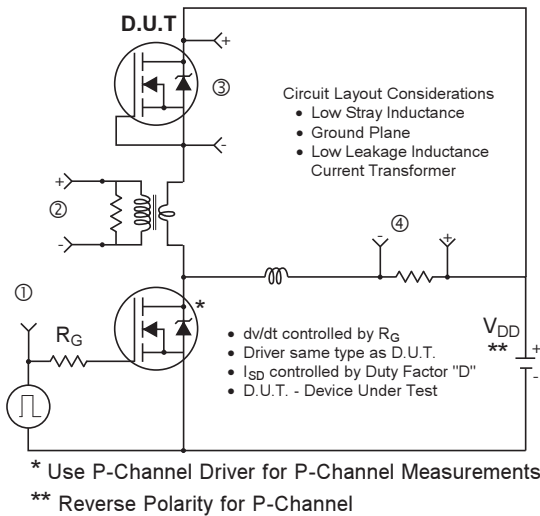

**Fig 12. On-Resistance vs. Gate Voltage**

**Fig 13. On-Resistance vs. Drain Current**

**Fig 15a. Unclamped Inductive Test Circuit**

**Fig 15b. Unclamped Inductive Waveforms**

**Fig 14. Maximum Avalanche Energy vs. Drain Current**

**Fig 16a. Switching Time Test Circuit**

**Fig 16b. Switching Time Waveforms**



**Fig 17a. Gate Charge Test Circuit**



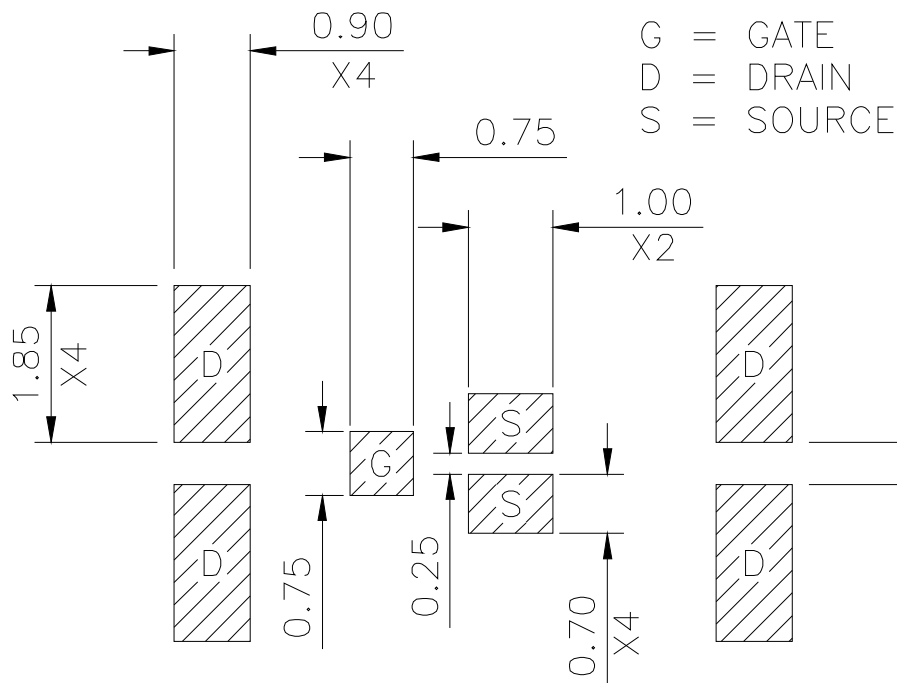
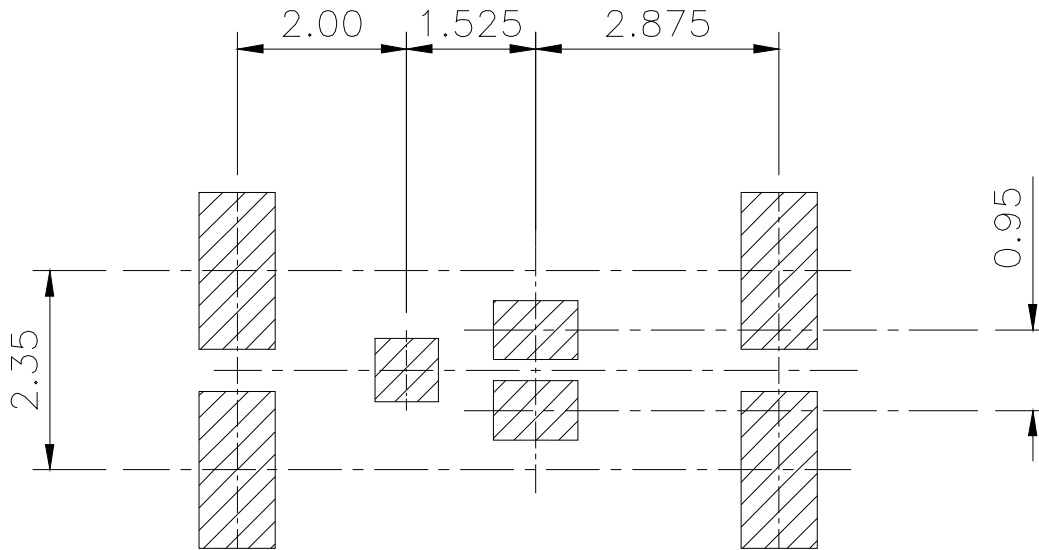
**Fig 17b. Gate Charge Waveform**



**Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs**

### DirectFET™ Substrate and PCB Layout, MZ Outline (Medium Size Can, Z-Designation).

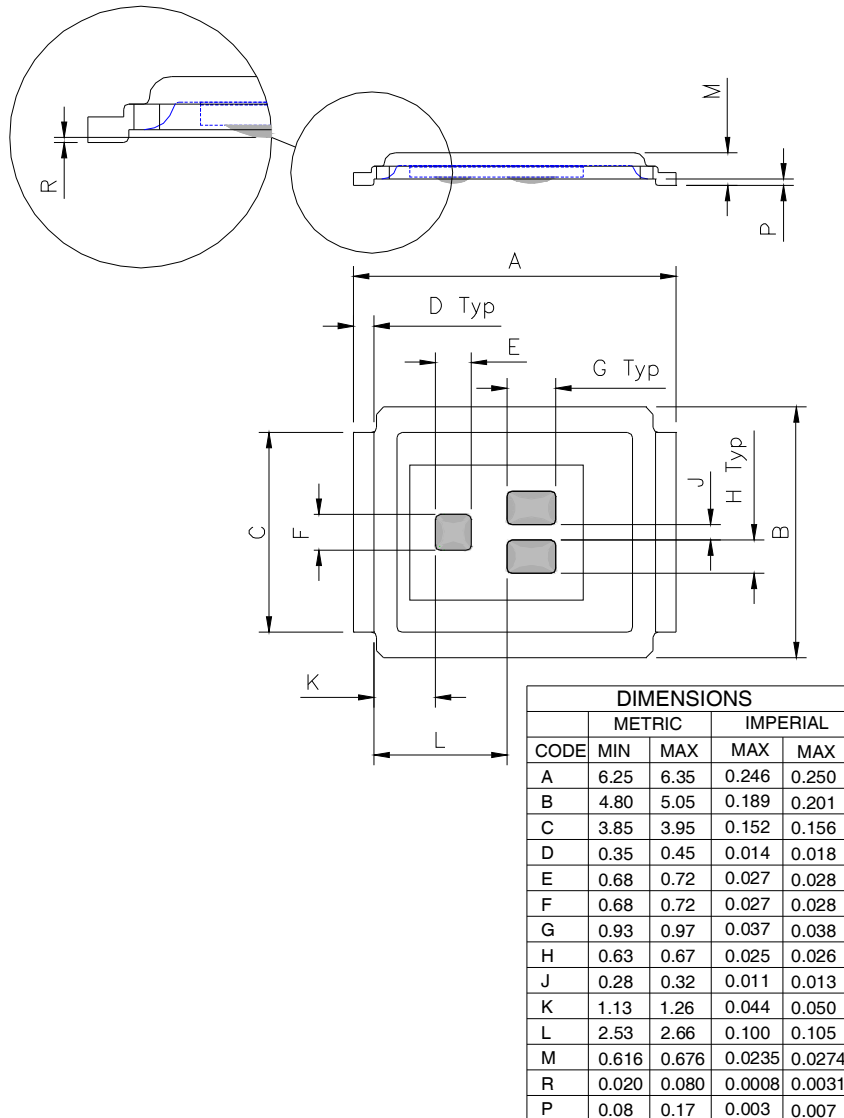
Please see DirectFET application note AN-1035 for all details regarding PCB assembly using DirectFET. This includes all recommendations for stencil and substrate designs.



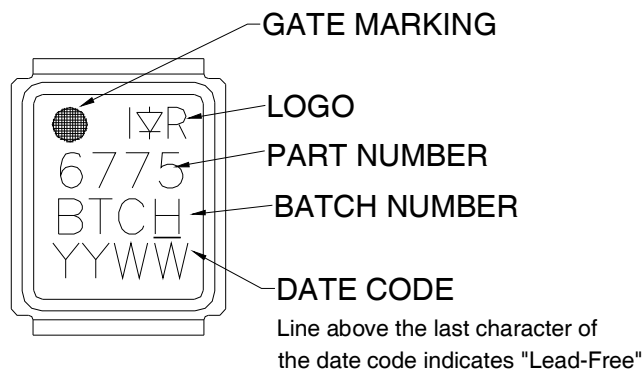
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

### DirectFET™ Outline Dimension, MZ Outline (Medium Size Can, Z-Designation).

Please see DirectFET application note AN-1035 for all details regarding PCB assembly using DirectFET. This includes all recommendations for stencil and substrate designs.

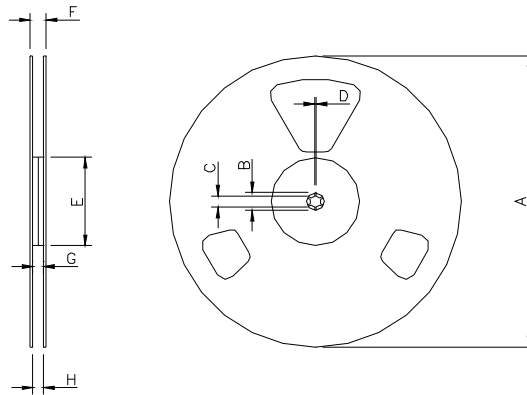


DirectFET™



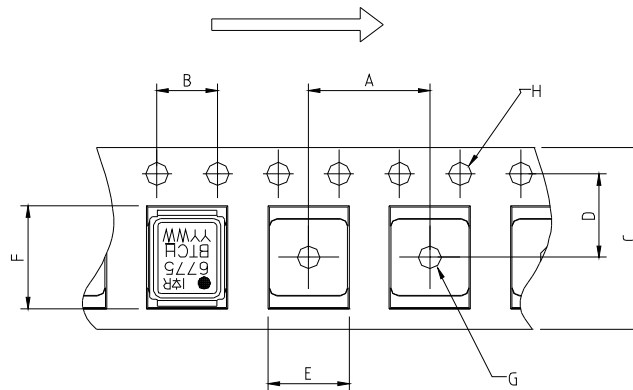
Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



**DirectFET™ Tape & Reel Dimension (Showing component orientation).**


NOTE: Controlling dimensions in mm  
 Std reel quantity is 4800 parts. (ordered as IRF6775TRPbF). For 1000 parts on 7" reel, order IRF6775TR1PbF

REEL DIMENSIONS								
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

**LOADED TAPE FEED DIRECTION**


NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Revision History**

Date	Comments
2/26/2014	<ul style="list-style-type: none"> <li>• Updated SOA curve figure 8 to extend x axis to 150V because this device is 150V, on page 4.</li> <li>• Updated datasheet with new IR corporate template.</li> </ul>

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Consumer market.  
 Qualification Standards can be found on IR's Web site.

International  
 Rectifier

**IR WORLD HEADQUARTERS:** 101 N. Sepulveda Blvd., El Segundo, California 90245, USA  
 To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>