

S5D9 Microcontroller

Datasheet

Renesas Synergy™ Platform

Synergy Microcontrollers
S5 Series

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General Precautions

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table 1.13 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	<ul style="list-style-type: none">xSecurity algorithms:<ul style="list-style-type: none">- Symmetric algorithms: AES, 3DES, and ARC4- Asymmetric algorithms: RSA and DSA.xOther support features:<ul style="list-style-type: none">- TRNG (True Random Number Generator)- Hash-value generation: SHA1, SHA224, SHA256, GHASH- 128-bit unique ID.

1.2 Block Diagram

Figure 1.1 shows the block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

1. Overview

The S5D9 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 120 MHz with the following features:

- Up to 2-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	<ul style="list-style-type: none"> • Maximum operating frequency: up to 120 MHz • ARM Cortex-M4 core: <ul style="list-style-type: none"> - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating point unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): <ul style="list-style-type: none"> - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: <ul style="list-style-type: none"> - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 2 MB of code flash memory. See section 55, Flash Memory in User's Manual.
Data flash memory	64 KB of data flash memory. See section 55, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	On-chip high-speed SRAM providing either parity-bit or Error Correction Code (ECC). The first 32 KB of SRAM0 is subject to ECC. Parity check is performed for other areas. See section 53, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 54, Standby SRAM in User's Manual.

Table 1.3 System (1 of 3)

Feature	Functional description
Operating modes	Two operating modes: <ul style="list-style-type: none"> - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual.

Table 1.3 System (2 of 3)

Feature	Functional description
Resets	<p>14 resets:</p> <ul style="list-style-type: none"> • RES pin reset • Power-on reset • Voltage monitor reset 0 • Voltage monitor reset 1 • Voltage monitor reset 2 • Independent Watchdog Timer reset • Watchdog Timer reset • Deep Software Standby reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. <p>See section 6, Resets in User's Manual.</p>
Low Voltage Detection (LVD)	<p>The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected in the software program. See section 8, Low Voltage Detection (LVD) in User's Manual.</p>
Clocks	<ul style="list-style-type: none"> • Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • Independent Watchdog Timer (WDT) on-chip oscillator • Clock out support. <p>See section 9, Clock Generation Circuit in User's Manual.</p>
Clock Frequency Accuracy Measurement Circuit (CAC)	<p>The CAC checks the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications.</p> <p>See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.</p>
Interrupt Controller Unit (ICU)	<p>The ICU controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.</p>
Key interrupt function (KINT)	<p>A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.</p>
Low-power modes	<p>Power consumption can be reduced in multiple ways, including by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low-power modes. See section 11, Low-Power Modes in User's Manual.</p>
Battery backup function	<p>A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual.</p>
Register write protection	<p>The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.</p>
Memory Protection Unit (MPU)	<p>Four MPUs and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.</p>
Watchdog Timer (WDT)	<p>The WDT is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and be used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual.</p>

Table 1.3 System (3 of 3)

Feature	Functional description
Independent Watchdog Timer (IWDT)	The IWDT consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The ELC uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A DTC module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	An 8-channel DMAC module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.6 External bus interface

Feature	Functional description
External buses	<ul style="list-style-type: none"> • CS area (EXBIU): Connected to the external devices (external memory interface) • SDRAM area (EXBIU): Connected to the SDRAM (external memory interface) • QSPI area (EXBIUT2): Connected to the QSPI (external device interface).

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The GPT is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General-Purpose Timer (AGT)	The AGT is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The RTC has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual.

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	<p>The SCI is configurable to five asynchronous and synchronous serial interfaces:</p> <ul style="list-style-type: none"> • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. <p>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol.</p> <p>Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 34, Serial Communications Interface (SCI) in User's Manual.</p>
IrDA Interface (IrDA)	<p>The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 35, IrDA Interface in User's Manual.</p>
I ² C Bus Interface (IIC)	<p>The three-channel IIC conforms with and provides a subset of the NXP I²C bus (Inter-Integrated Circuit bus) interface functions. See section 36, I²C Bus Interface (IIC) in User's Manual.</p>
Serial Peripheral Interface (SPI)	<p>Two independent SPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 38, Serial Peripheral Interface (SPI) in User's Manual.</p>
Serial Sound Interface Enhanced (SSIE)	<p>The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I²S 2ch, 4ch, 6ch, 8ch, WS Continue/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 41, Serial Sound Interface Enhanced (SSIE) in User's Manual.</p>
Quad Serial Peripheral Interface (QSPI)	<p>The QSPI is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 39, Quad Serial Peripheral Interface (QSPI) in User's Manual.</p>
CAN module (CAN)	<p>The CAN module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 37, Controller Area Network (CAN) Module in User's Manual.</p>
USB 2.0 Full-Speed Module (USBFS)	<p>Full-Speed USB controller that can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 32, USB 2.0 Full-Speed Module (USBFS) in User's Manual.</p>
USB 2.0 High-Speed Module (USBHS)	<p>High-Speed USB controller that can operate as a host controller or a device controller. As a host controller, the USBHS supports high-speed transfer, full-speed transfer, and low-speed transfer as defined in Universal Serial Bus Specification 2.0. As a device controller, the USBHS supports high-speed transfer and full-speed transfer as defined in Universal Serial Bus Specification 2.0. The USBHS has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USBHS has FIFO buffers for data transfer, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or your system for communication. See section 33, USB 2.0 High-Speed Module (USBHS) in User's Manual.</p>

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Ethernet MAC with IEEE 1588 PTP (ETHERC)	<p>One-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. An ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU.</p> <p>To handle timing and synchronization between devices, an on-chip Precision Time Protocol (PTP) module for the Ethernet PTP Controller (EPTPC) applies the PTP defined in the IEEE 1588-2008 version 2.0 standard.</p> <p>The EPTPC is composed of:</p> <ul style="list-style-type: none"> • Synchronization Frame Processing unit (SYNFP0) • A Statistical Time Correction Algorithm unit (STCA). <p>Use the EPTPC in combination with the on-chip Ethernet MAC Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). See section 29, Ethernet MAC Controller (ETHERC) in User's Manual.</p>
SD/MMC Host Interface (SDHI)	<p>The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA).</p> <p>The MMC interface supports 1-, 4-, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 43, SD/MMC Host Interface (SDHI) in User's Manual.</p>

Table 1.9 Analog

Feature	Functional description
12-Bit A/D Converter (ADC12)	<p>Up to two successive approximation 12-Bit A/D Converters are provided. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 11 analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-, 10-, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 47, 12-Bit A/D Converter (ADC12) in User's Manual.</p>
12-Bit D/A Converter (DAC12)	<p>The DAC12 D/A converts data and includes an output amplifier. See section 48, 12-Bit D/A Converter (DAC12) in User's Manual.</p>
Temperature sensor (TSN)	<p>The on-chip temperature sensor can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 49, Temperature Sensor (TSN) in User's Manual.</p>
High-Speed Analog Comparator (ACMPHS)	<p>Analog comparators can be used to compare a test voltage with a reference voltage and to provide a digital output based on the conversion result.</p> <p>Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA.</p> <p>Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 50, High-Speed Analog Comparator (ACMPHS) in User's Manual.</p>

Table 1.10 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	<p>The CTSU measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by the software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that fingers do not come into direct contact with the electrodes. See section 51, Capacitive Touch Sensing Unit (CTSU) in User's Manual.</p>

Table 1.11 Graphics

Feature	Functional description
Graphics LCD Controller (GLCDC)	<p>The GLCDC provides multiple functions and supports various data formats and panels. Key GLCDC features include:</p> <ul style="list-style-type: none"> • GPX bus master function for accessing graphics data • Superimposition of three planes (single color background plane, graphic 1 plane, and graphic 2 plane) • Support for many types of 32- or 16-bit per pixel graphics data and 8-, 4-, or 1-bit LUT data format • Digital interface signal output supporting a video image size of WVGA or greater. <p>See section 58, Graphics LCD Controller (GLCDC) in User's Manual.</p>
2D Drawing Engine (DRW)	<p>The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased. Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box. The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering. If it is outside, it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing. Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the DRW. The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write). The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write. See section 56, 2D Drawing Engine (DRW) in User's Manual.</p>
JPEG Codec (JPEG)	<p>The JPEG Codec (JPEG) incorporates a JPEG codec that conforms to the JPEG baseline compression and decompression standard. This provides high-speed compression of image data and high-speed decoding of JPEG data. See section 57, JPEG Codec (JPEG) in User's Manual.</p>
Parallel Data Capture Unit (PDC)	<p>One PDC unit is provided for communicating with external I/O devices, including image sensors, and transferring parallel data such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 44, Parallel Data Capture Unit (PDC) in User's Manual.</p>

Table 1.12 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	<p>The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 40, Cyclic Redundancy Check (CRC) Calculator in User's Manual.</p>
Data Operation Circuit (DOC)	<p>The DOC compares, adds, and subtracts 16-bit data. See section 52, Data Operation Circuit (DOC) in User's Manual.</p>
Sampling Rate Converter (SRC)	<p>The SRC converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 42, Sampling Rate Converter (SRC) in User's Manual.</p>

Table 1.13 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	<ul style="list-style-type: none">• Security algorithms:<ul style="list-style-type: none">- Symmetric algorithms: AES, 3DES, and ARC4- Asymmetric algorithms: RSA and DSA.• Other support features:<ul style="list-style-type: none">- TRNG (True Random Number Generator)- Hash-value generation: SHA1, SHA224, SHA256, GHASH- 128-bit unique ID.

1.2 Block Diagram

[Figure 1.1](#) shows the block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

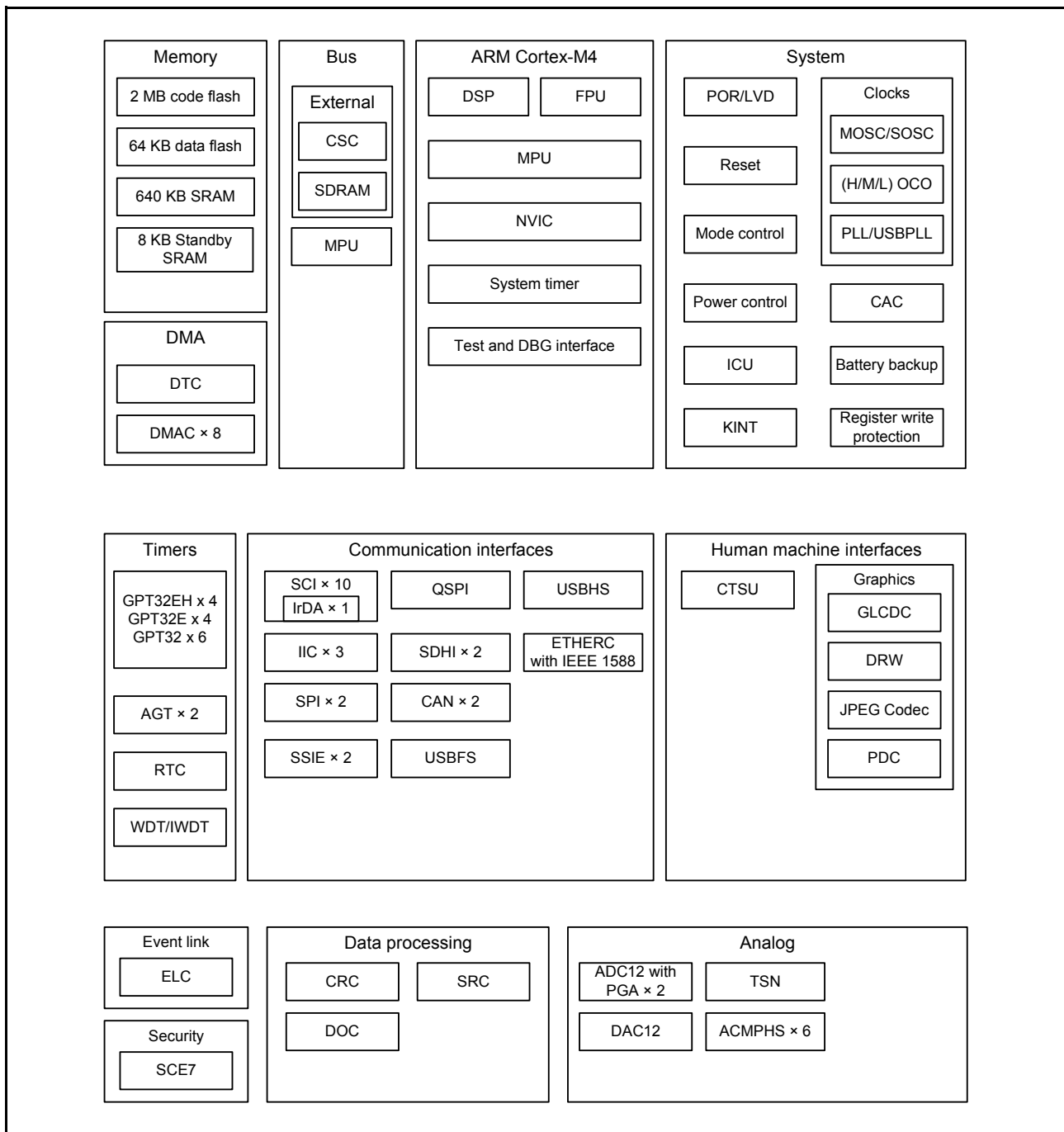


Figure 1.1 Block diagram

1.3 Part Numbering

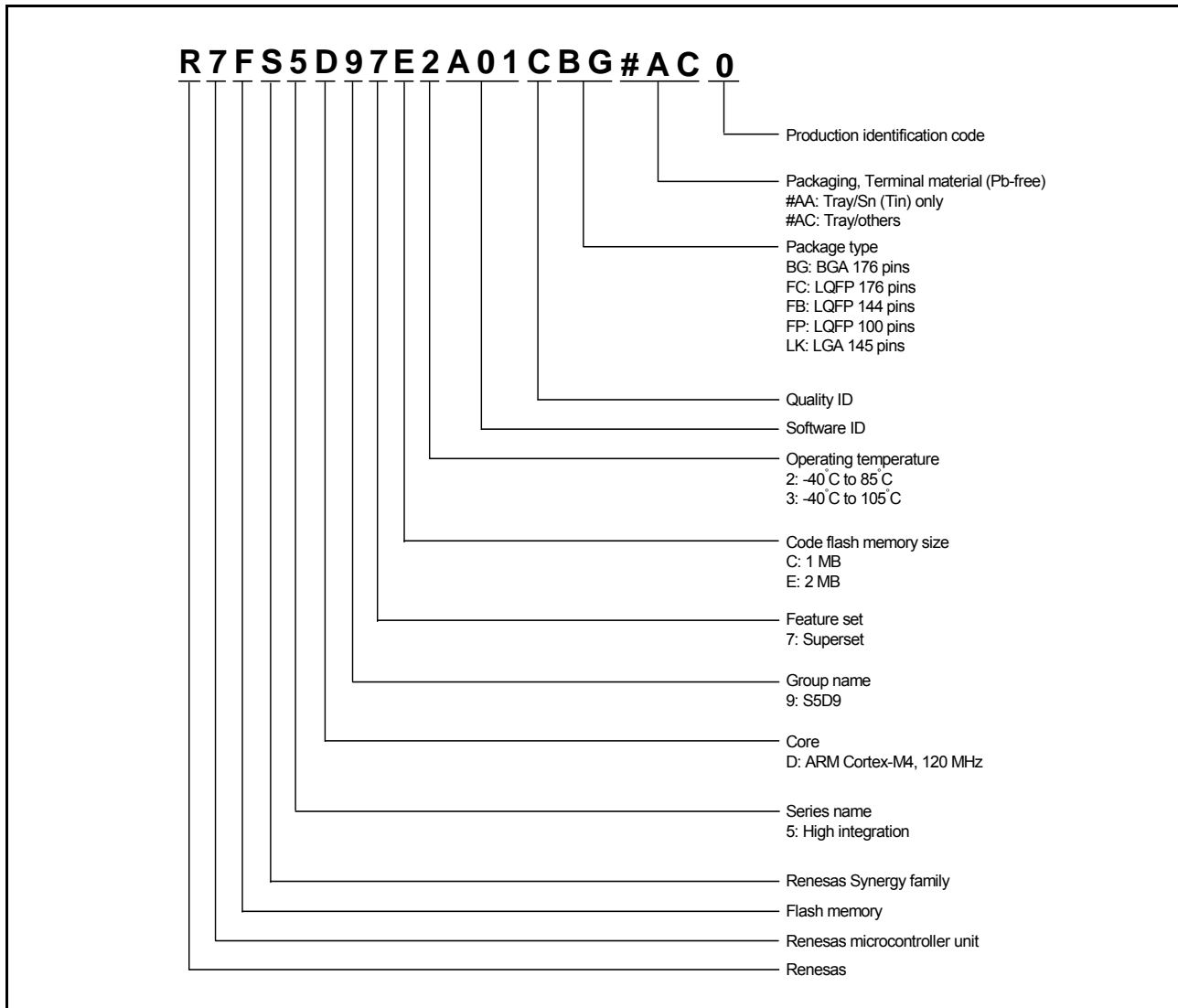


Figure 1.2 Part numbering scheme

Table 1.14 List of Products

Part Number	Orderable Part Number	Package	Code flash	Data flash	SRAM	Operating Temperature
R7FS5D97E2A01CBG	R7FS5D97E2A01CBG#AC0	PLBG0176GE-A	2 MB	64 KB	640 KB	-40 to +85°C
R7FS5D97E3A01CFC	R7FS5D97E3A01CFC#AA0	PLQP0176KB-A				-40 to +105°C
R7FS5D97E2A01CLK	R7FS5D97E2A01CLK#AC0	PTLG0145KA-A				-40 to +85°C
R7FS5D97E3A01CFB	R7FS5D97E3A01CFB#AA0	PLQP0144KA-B				-40 to +105°C
R7FS5D97E3A01CFP	R7FS5D97E3A01CFP#AA0	PLQP0100KB-B				-40 to +105°C
R7FS5D97C2A01CBG	R7FS5D97C2A01CBG#AC0	PLBG0176GE-A				1 MB
R7FS5D97C3A01CFC	R7FS5D97C3A01CFC#AA0	PLQP0176KB-A	-40 to +105°C			
R7FS5D97C2A01CLK	R7FS5D97C2A01CLK#AC0	PTLG0145KA-A	-40 to +85°C			
R7FS5D97C3A01CFB	R7FS5D97C3A01CFB#AA0	PLQP0144KA-B	-40 to +105°C			
R7FS5D97C3A01CFP	R7FS5D97C3A01CFP#AA0	PLQP0100KB-B	-40 to +105°C			

1.4 Function Comparison

Table 1.15 Functional comparison (Graphics)

Function	Part numbers					
	R7FS5D97E2XXXCBG/ R7FS5D97C2XXXCBG	R7FS5D97E3XXXCFE/ R7FS5D97C3XXXCFE	R7FS5D97E2XXXCLK/ R7FS5D97C2XXXCLK	R7FS5D97E3XXXCFB/ R7FS5D97C3XXXCFB	R7FS5D97E3XXXCFP/ R7FS5D97C3XXXCFP	
Pin count	176	176	145	144	100	
Package	BGA	LQFP	LGA	LQFP	LQFP	
Code flash memory	2/1 MB					
Data flash memory	64 KB					
SRAM	640 KB					
	Parity	608 KB				
	ECC	32 KB				
Standby SRAM	8 KB					
System	CPU clock	120 MHz				
	Backup registers	512 B				
	ICU	Yes				
	KINT	8				
Event link	ELC	Yes				
DMA	DTC	Yes				
	DMAC	8				
BUS	External bus	16-bit bus			8-bit bus	
	SDRAM	Yes			No	
Timers	GPT32EH	4	4	4	4	
	GPT32E	4	4	4	4	
	GPT32	6	6	6	5	
	AGT	2	2	2	2	
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	10				
	IIC	3			2	
	SPI	2				
	SSIE	2			1	
	QSPI	1				
	SDHI	2				
	CAN	2				
	USBFS	Yes				
	USBHS	Yes		No		
ETHERC	1					
Analog	ADC12	24		22	19	
	DAC12	2				
	ACMPHS	6				
	TSN	Yes				
HMI	CTSU	13		18	12	
	Graphics	GLCDC	RGB888			
		DRW	Yes			
		JPEG	Yes			
		PDC	Yes			
Data processing	CRC	Yes				
	DOC	Yes				
	SRC	Yes				
Security	SCE7					

1.5 Pin Functions

Table 1.16 Pin functions (1 of 5)

Function	Signal	I/O	Description
Power supply	VCC	Input	Digital voltage supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect to the system power supply. Connect to VSS through a 0.1- μ F smoothing capacitor close to each VCC pin.
	VCL0	-	Connect to VSS through a 0.1- μ F smoothing capacitor close to each VCL pin. Stabilize the internal power supply.
	VCL	-	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOU and XCIN.
	XCOU	Output	
	EBCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ15	Input	Maskable interrupt request pins.
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins.
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins.
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TDATA0 to TDATA3	Output	Trace data output.
	SWDIO	I/O	Serial wire debug data input/output pin.
	SWCLK	Input	Serial wire clock pin.
	SWO	Output	Serial wire trace output pin.
	External bus interface	RD	Output
WR		Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active low.
WR0 to WR1		Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active low.
BC0 to BC1		Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active low.
ALE		Output	Address latch signal when address/data multiplexed bus is selected.
WAIT		Input	Input pin for wait request signals in access to the external space, active low.
CS0 to CS7		Output	Select signals for CS areas, active low.
A00 to A23		Output	Address bus.
D00 to D15		I/O	Data bus.
A00/D00 to A15/D15		I/O	Address/data multiplexed bus.

Table 1.16 Pin functions (2 of 5)

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM clock enable signal.
	SDCS	Output	SDRAM chip select signal, active low.
	RAS	Output	SDRAM low address strobe signal, active low.
	CAS	Output	SDRAM column address strobe signal, active low.
	WE	Output	SDRAM write enable signal, active low.
	DQM0	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00.
	DQM1	Output	SDRAM I/O data mask enable signal for DQ15 to DQ08.
	A00 to A15	Output	Address bus.
DQ00 to DQ15	I/O	Data bus.	
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins.
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	Input capture, output compare, or PWM output pins.
	GTIU	Input	Hall sensor input pin U.
	GTIV	Input	Hall sensor input pin V.
	GTIW	Input	Hall sensor input pin W.
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U phase).
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U phase).
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V phase).
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V phase).
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W phase).
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W phase).
AGT	AGTEE0, AGTEE1	Input	External event input enable signals.
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins.
	AGTO0, AGTO1	Output	Pulse output pins.
	AGTOA0, AGTOA1	Output	Output compare match A output pins.
	AGTOB0, AGTOB1	Output	Output compare match B output pins.
RTC	RTCOU	Output	Output pin for 1-Hz or 64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
SCI	SCK0 to SCK9	I/O	Input/output pins for the clock (clock synchronous mode).
	RXD0 to RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode).
	TXD0 to TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode).
	CTS0_RTS0 to CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active low.
	SCL0 to SCL9	I/O	Input/output pins for the I ² C clock (simple IIC mode).
	SDA0 to SDA9	I/O	Input/output pins for the I ² C data (simple IIC mode).
	SCK0 to SCK9	I/O	Input/output pins for the clock (simple SPI mode).
	MISO0 to MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode).
	MOSI0 to MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode).
	SS0 to SS9	Input	Chip-select input pins (simple SPI mode), active low.
IIC	SCL0 to SCL2	I/O	Input/output pins for the clock.
	SDA0 to SDA2	I/O	Input/output pins for data.
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins.
	SSIBCK1		
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins.
	SSILRCK1/SSIFS1		
	SSITXD0	Output	Serial data output pins.
	SSIRXD0	Input	Serial data input pins.
	SSIDATA1	I/O	Serial data input/output pins.
AUDIO_CLK	Input	External clock pin for audio (input oversampling clock).	

Table 1.16 Pin functions (3 of 5)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin.
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master.
	MISOA, MISOB	I/O	Input or output pins for data output from the slave.
	SSLA0, SSLB0	I/O	Input or output pin for slave selection.
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection.
QSPI	QSPCLK	Output	QSPI clock output pin.
	QSSL	Output	QSPI slave output pin.
	QIO0 to QIO3	I/O	Data0 to Data3.
CAN	CRX0, CRX1	Input	Receive data.
	CTX0, CTX1	Output	Transmit data.
USBFS	VCC_USB	Input	Power supply pins.
	VSS_USB	Input	Ground pins.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip.
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip.
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode.
USBHS	VCC_USBHS	Input	Power supply pin.
	VSS1_USBHS	Input	Ground pin.
	VSS2_USBHS	Input	Ground pin.
	AVCC_USBHS	Input	Analog power supply pin for the USBHS.
	AVSS_USBHS	Input	Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin.
	PVSS_USBHS	Input	PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin.
	USBHS_RREF	I/O	USBHS reference current source pin. Connect this pin to the AVSS_USBHS pin through a 2.2-kΩ resistor ($\pm 1\%$).
	USBHS_DP	I/O	USB bus D+ data pin.
	USBHS_DM	I/O	USB bus D- data pin.
	USBHS_EXICEN	Output	Connect this pin to the OTG power supply IC.
	USBHS_ID	Input	Connect this pin to the OTG power supply IC.
	USBHS_VBUSEN	Output	VBUS power enable signal for USB.
	USBHS_OVRCURA, USBHS_OVRCURB	Input	Overcurrent pin for USB.
	USBHS_VBUS	Input	USB cable connection monitor input pin.

Table 1.16 Pin functions (4 of 5)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode.
	RMII0_CRS_DV	Input	Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode.
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode.
	RMII0_TXD_EN	Output	Output pin for data transmit enable signal in RMII mode.
	RMII0_RX_ER	Input	Indicates an error occurred during reception of data in RMII mode.
	ET0_CRS	Input	Carrier detection/data reception enable signal.
	ET0_RX_DV	Input	Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0.
	ET0_EXOUT	Output	General-purpose external output pin.
	ET0_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data.
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data.
	ET0_TX_EN	Output	Transmit enable signal. Functions as signal indicating that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET0_TX_ER	Output	Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission.
	ET0_RX_ER	Input	Receive error pin. Functions as signal to recognize an error during reception.
	ET0_TX_CLK	Input	Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER.
	ET0_RX_CLK	Input	Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER.
	ET0_COL	Input	Input collision detection signal.
	ET0_WOL	Output	Receive Magic packets.
	ET0_MDC	Output	Output reference clock signal for information transfer through ET0_MDIO.
ET0_MDIO	I/O	Input or output bidirectional signal for exchange of management data with PHY-LSI.	
SDHI	SD0CLK, SD1CLK	Output	SD clock output pins.
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pins.
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins.
	SD0CD, SD1CD	Input	SD card detection pins.
	SD0WP, SD1WP	Input	SD write-protect signals.
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.

Table 1.16 Pin functions (5 of 5)

Function	Signal	I/O	Description
ADC12	AN000 to AN007, AN016 to AN020	Input	Input pins for the analog signals to be processed by the ADC12.
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion.
	ADTRG1	Input	
	PGAVSS000/PGAVS S100	Input	Differential input pins.
DAC12	DA0, DA1	Output	Output pins for the analog signals processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin.
	IVREF0 to IVREF3	Input	Reference voltage input pins for comparator.
	IVCMP0 to IVCMP2	Input	Analog voltage input pins for comparator.
CTSU	TS00 to TS17	Input	Capacitive touch detection pins (touch pins).
	TSCAP	-	Secondary power supply pin for the touch driver.
I/O ports	P000 to P007	Input	General-purpose input pins.
	P008 to P010, P014, P015	I/O	General-purpose input/output pins.
	P100 to P115	I/O	General-purpose input/output pins.
	P200	Input	General-purpose input pin.
	P201 to P214	I/O	General-purpose input/output pins.
	P300 to P315	I/O	General-purpose input/output pins.
	P400 to P415	I/O	General-purpose input/output pins.
	P500 to P508, P511 to P513	I/O	General-purpose input/output pins.
	P600 to P615	I/O	General-purpose input/output pins.
	P700 to P713	I/O	General-purpose input/output pins.
	P800 to P806	I/O	General-purpose input/output pins.
	P900, P901, P905 to P908	I/O	General-purpose input/output pins.
	PA00, PA01, PA08 to PA10	I/O	General-purpose input/output pins.
	PB00, PB01	I/O	General-purpose input/output pins.
GLCDC	LCD_DATA23 to LCD_DATA00	Output	Data output pins for panel.
	LCD_TCON3 to LCD_TCON0	Output	Output pins for panel timing adjustment.
	LCD_CLK	Output	Panel clock output pin.
	LCD_EXTCLK	Input	Panel clock source input pin.
PDC	PIXCLK	Input	Image transfer clock pin.
	VSYNC	Input	Vertical synchronization signal pin.
	HSYNC	Input	Horizontal synchronization signal pin.
	PIXD0 to PIXD7	Input	8-bit image data pins.
	PCKO	Output	Output pin for dot clock.

1.6 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments.

R7FS5D9XX2XXXCBG

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	P708	USBHS_DM	PVSS_USBHS	P212 /XTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_DP	AVSS_USBHS	P213 /XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_USB	VSS_USB	P408	P413	VCC_USBHS	USBHS_RREF	AVCC_USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_USBHS	VSS2_USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	P214	P211	P901	VSS								VSS	P006	P008	P005	10
9	P210	P209	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	P208	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	P508	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK /SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL	P606	P602	P600	P106	P103	P100	P801	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 1.3 Pin assignment for 176-pin BGA (top view)

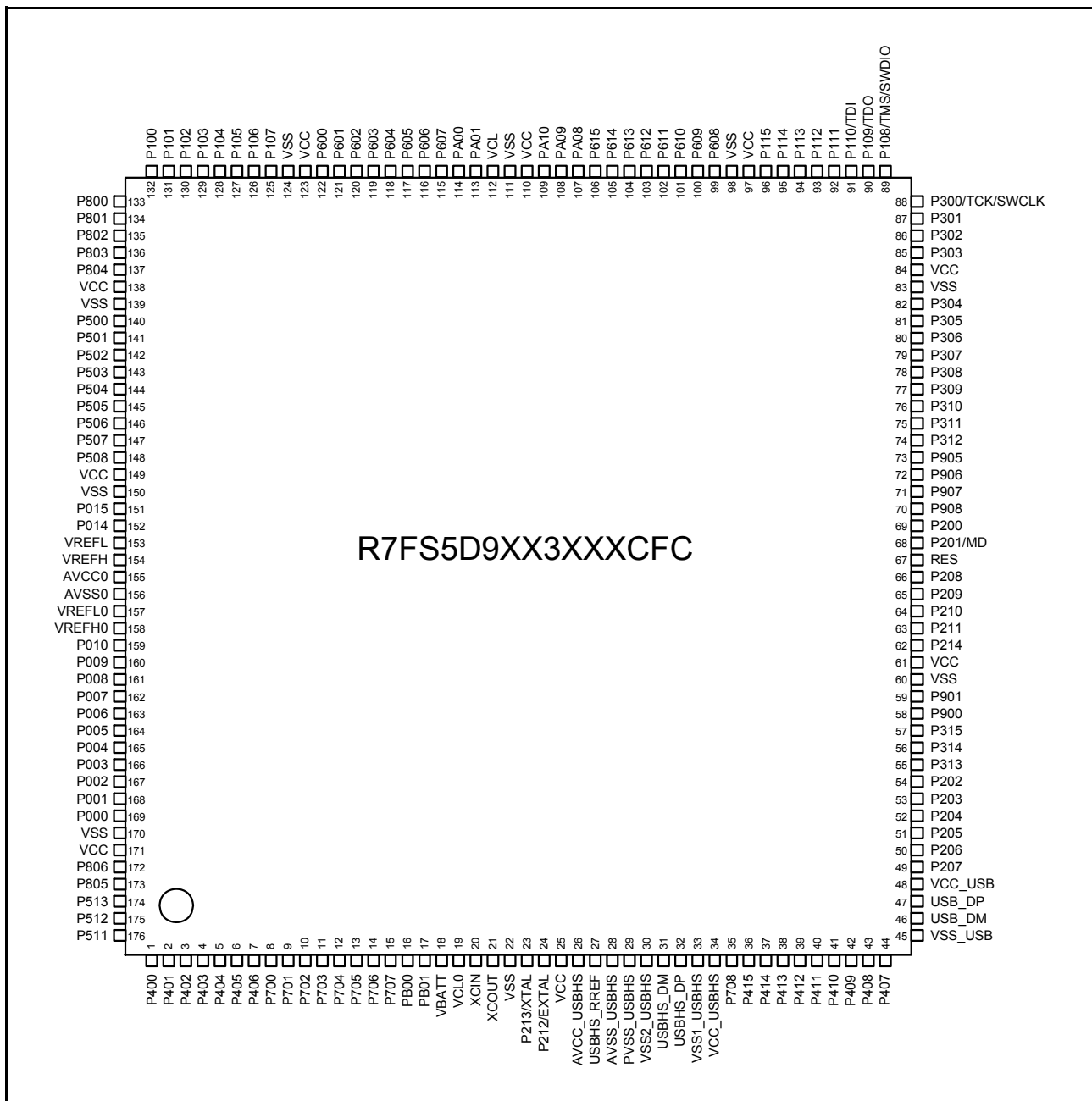


Figure 1.4 Pin assignment for 176-pin LQFP (top view)

R7FS5D9XX2XXXCLK

	A	B	C	D	E	F	G	H	J	K	L	M	N		
13	P407	P409	P412	P708	P711	VCC	P212 /XTAL	XCIN	VCLO	P702	P405	P402	P400	13	
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOU	VBATT	P701	P404	P511	VCC	12	
11	VCC_USB	VSS_USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11	
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10	
9	P203	P313	P202	VSS						P004	P006	P009	P008	9	
8	P214	P211	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8	
7	P210	P209	RES	P310						P007	AVCC0	VREFL	VREFH	7	
6	P208	P201/MD	P312	P305						P505	P506	P015	P014	6	
5	P309	P311	P308	P303	NC						P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	P508	4	
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3	
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2	
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL	P602	VSS	P103	P102	P100	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N		

Figure 1.5 Pin assignment for 145-pin LGA (top view)

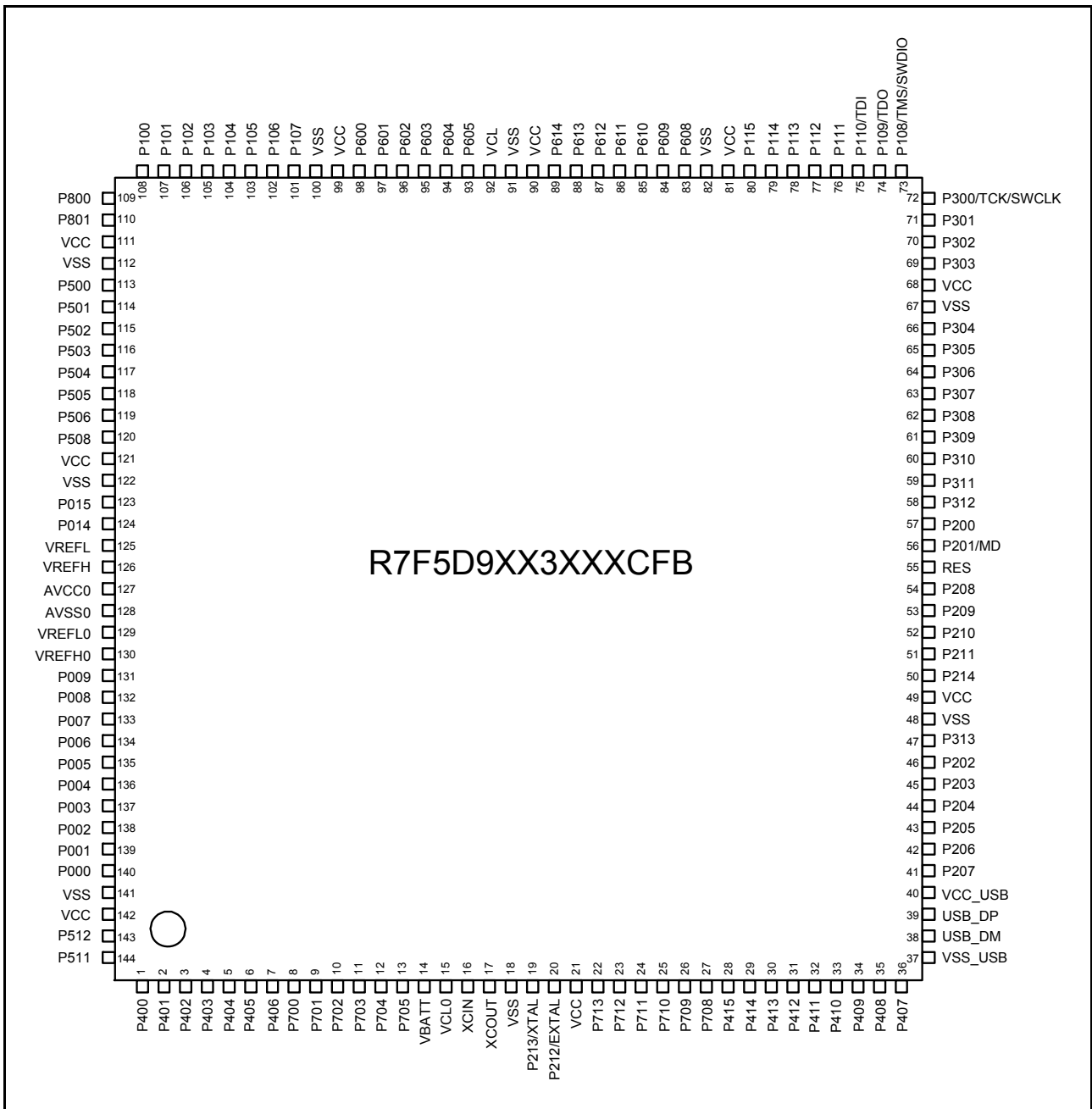


Figure 1.6 Pin assignment for 144-pin LQFP (top view)

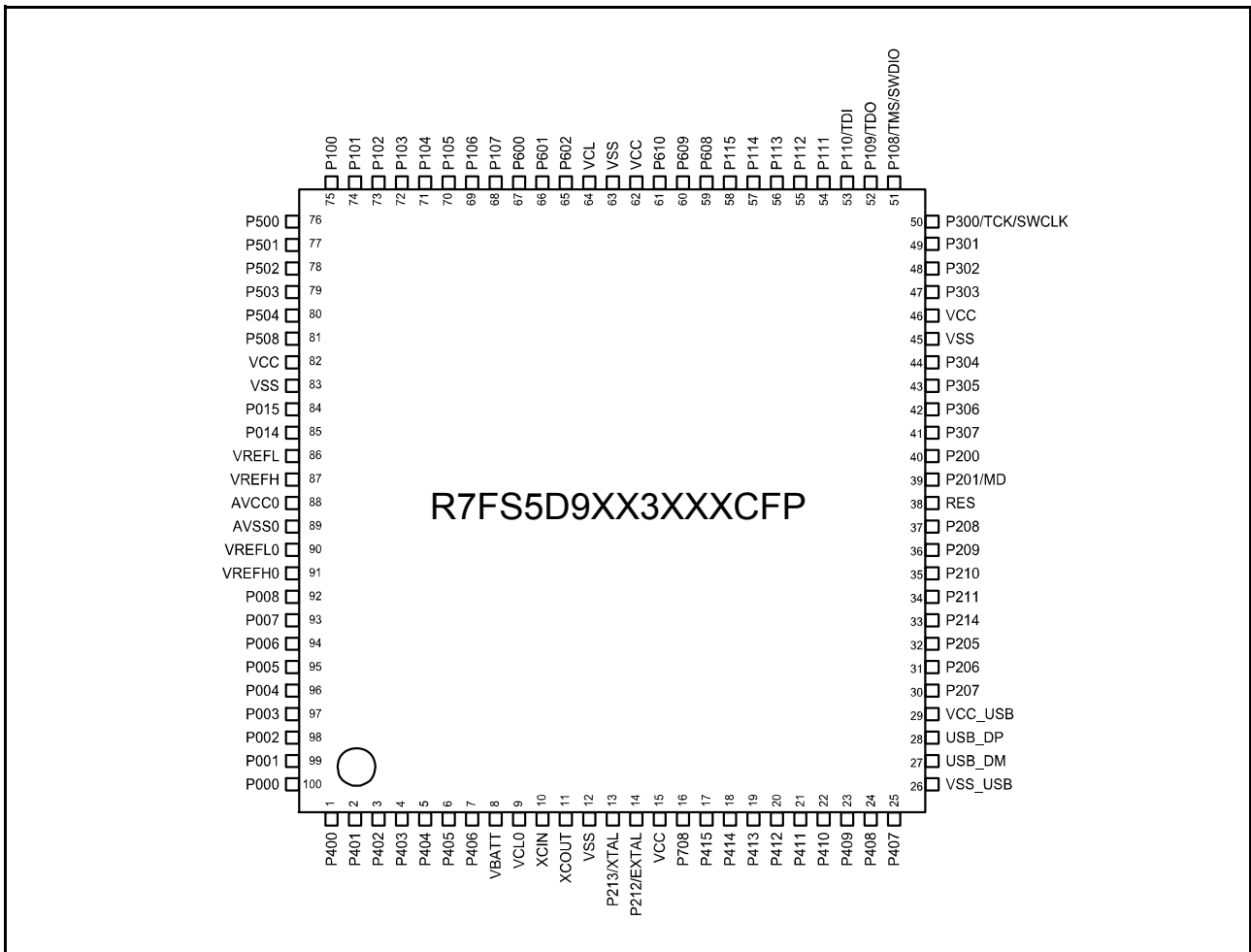


Figure 1.7 Pin assignment for 100-pin LQFP (top view)

1.7 Pin Lists

Pin number		Power, System, Clock, Debug, CAC				Interrupt	I/O port	Extbus		Timers				Communication interfaces							Analog			HMI				
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI(2,4,6,8 (30 MHz))	SCI(3,5,7,9 (30 MHz))	IIC	SPI, QSPI	SSIE	ETHERC (MI) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC	
N13	1	N13	1	1		IRQ0	P400			AGTIO1		GTIOC6A			SCK4	SCK7	SCL0_A		AUDIO_CLK	ET0_WOL	ET0_WOL			ADTRG1				
R15	2	L11	2	2		IRQ5-DS	P401				GTETRGA	GTIOC6B		CTX0	CTS4_RTS4/SS4	TXD7/MOSI7/SDA7	SDA0_A				ET0_MDC	ET0_MDC						
P14	3	M13	3	3	CACREF	IRQ4-DS	P402			AGTIO0/AGTIO1			RTCIC0	CRX0		RXD7/MISO7/SCL7			AUDIO_CLK	ET0_MDIO	ET0_MDIO						VSYN	
M12	4	K11	4	4			P403			AGTIO0/AGTIO1		GTIOC3A	RTCIC1		CTS7_RTS7/SS7				SSIBC_K0_A	ET0_LI_NKSTA	ET0_LI_NKSTA		SD1_DAT7_B				PIXD7	
M13	5	L12	5	5			P404					GTIOC3B	RTCIC2						SSILRCK0/SIFS0_A	ET0_EX_OUT	ET0_EX_OUT		SD1_DAT6_B				PIXD6	
P15	6	L13	6	6			P405					GTIOC1A							SSITX_D0_A	ET0_TX_EN	RMII0_TXD_EN_B		SD1_DAT5_B				PIXD5	
N14	7	J10	7	7			P406					GTIOC1B						SSLB3_C	SSIRX_D0_A	ET0_RX_ER	RMII0_TXD1_B		SD1_DAT4_B				PIXD4	
N15	8	H10	8				P700					GTIOC5A						MISOB_C		ET0_ETXD1	RMII0_TXD0_B		SD1_DAT3_B				PIXD3	
M14	9	K12	9				P701					GTIOC5B						MOSIB_C		ET0_ETXD0	REF50_CK0_B		SD1_DAT2_B				PIXD2	
L12	10	K13	10				P702					GTIOC6A						RSPC_KB_C		ET0_ERXD1	RMII0_RXD0_B		SD1_DAT1_B				PIXD1	
M15	11	J11	11				P703					GTIOC6B						SSLB0_C		ET0_ERXD0	RMII0_RXD1_B		SD1_DAT0_B		VCOU		PIXD0	
L13	12	H11	12				P704			AGT00								SSLB1_C		ET0_RX_CLK	RMII0_RXE_B		SD1_CLK_B				HSYNC	
K12	13	G11	13				P705			AGTIO0								SSLB2_C		ET0_CRS	RMII0_CRS_DV_B		SD1_CMD_B				PIXCLK	
L14	14					IRQ7	P706									RXD3/MISO3/SCL3					USB_HS_OVRCUR_B		SD1_CD_B					
L15	15					IRQ8	P707									TXD3/MOSI3/SDA3					USB_HS_OVRCUR_A		SD1_WP_B					
J12	16						PB00									SCK3						USB_HS_VBUS						
K13	17						PB01									CTS3_RTS3/SS3							USB_HS_VBUS					
K14	18	J12	14	8	VBATT																							
K15	19	J13	15	9	VCL0																							
J15	20	H13	16	10	XCLN																							
J14	21	H12	17	11	XCOU																							
J13	22	F12	18	12	VSS																							
H14	23	G12	19	13	XTAL	IRQ2	P213				GTETRGC	GTIOC0A			TXD1/MOSI1/SDA1									ADTRG1				
H15	24	G13	20	14	EXTAL	IRQ3	P212			AGTEE1	GTETRGD	GTIOC0B			RXD1/MISO1/SCL1													
H12	25	F13	21	15	VCC																							
H13	26				AVCC_U_SBHS																							
G13	27				USBHS_RREF																							
G14	28				AVSS_U_SBHS																							
G15	29				PVSS_U_SBHS																							
G12	30				VSS2_U_SBHS																							
F15	31																										USB_HS_DM	
F14	32																										USB_HS_DP	
F12	33				VSS1_U_SBHS																							
F13	34				VCC_US_BHS																							
E15	35						P708																					

Pin number				Extbus		Timers				Communication interfaces										Analog		HMI							
BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MI) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACOMP5	CTS0	GLDC, PDC		
-	-	G10	22	-	-	-	P713	-	-	AGTOA0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TS17	-	
-	-	F11	23	-	-	-	P712	-	-	AGTOB0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TS16	-	
-	-	E13	24	-	-	-	P711	-	-	AGTEE0	-	-	-	-	-	CTS1 RTS1/ SS1	-	-	-	ET0_TX _CLK	-	-	-	-	-	-	TS15	-	
-	-	E12	25	-	-	-	P710	-	-	-	-	-	-	-	-	SCK1	-	-	-	ET0_TX _ER	-	-	-	-	-	-	TS14	-	
-	-	F10	26	-	-	-	IRQ10	P709	-	-	-	-	-	-	-	TXD1/ MOS11 /SDA1	-	-	-	ET0_ET XD2	-	-	-	-	-	-	TS13	-	
-	-	D13	27	16	CACREF	IRQ11	P708	-	-	-	-	-	-	-	-	RXD1/ MISO1 /SCL1	-	SSLA3 _B	AUDIO _CLK	ET0_ET XD3	-	-	-	-	-	-	TS12	PCKO	
E14	36	E11	28	17	-	IRQ8	P415	-	-	-	-	-	-	USB _VBUS _EN	-	-	-	-	SSLA2 _B	ET0_TX _EN	RMII0_ TXD_E N_A	-	SD0 CD_ A	-	-	TS11	PIXD5		
D15	37	D12	29	18	-	IRQ9	P414	-	-	-	-	-	-	-	-	-	-	-	SSLA1 _B	ET0_RX _ER	RMII0_ TXD1_ A	-	SD0 WP_ A	-	-	TS10	PIXD4		
E13	38	E10	30	19	-	-	P413	-	-	-	-	-	-	-	CTS0_ RTS0/ SS0	-	-	-	SSLA0 _B	ET0_ET XD1	RMII0_ TXD0_ A	-	SD0 CLK_ A	-	-	TS09	PIXD3		
D14	39	C13	31	20	-	-	P412	-	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPC KA_B	-	ET0_ET XD0	REF50 CK0_A	-	SD0 CMD _A	-	-	TS08	PIX02		
C15	40	D11	32	21	-	IRQ4	P411	-	-	AGTOA1	GTOVUP	GTIOC 9A	-	-	TXD0/ MOS10 /SDA0	CTS3_ RTS3/ SS3	-	MOSIA _B	-	ET0_ER XD1	RMII0_ RXD0_ A	-	SD0 DAT0 _A	-	-	TS07	PIX01		
C14	41	C12	33	22	-	IRQ5	P410	-	-	AGTOB1	GTOVLO	GTIOC 9B	-	-	RXD0/ MISO0 /SCL0	SCK3	-	MISOA _B	-	ET0_ER XD0	RMII0_ RXD1_ A	-	SD0 DAT1 _A	-	-	TS06	PIXD0		
B15	42	B13	34	23	-	IRQ6	P409	-	-	-	GTOVUP	GTIOC 10A	-	USB _EXIC _EN	TXD3/ MOS13 /SDA3	-	-	-	-	ET0_RX _CLK	RMII0_ RX_E R_A	-	USB HS_ EXIC _EN	-	-	TS05	HSYNC		
D13	43	D10	35	24	-	IRQ7	P408	-	-	-	GTOVLO	GTIOC 10B	-	USB _ID	RXD3/ MISO3 /SCL3	-	-	-	-	ET0_C RS	RMII0_ CRS_ DV_A	-	USB HS_ I D	-	-	TS04	PIXCLK		
A15	44	A13	36	25	-	-	P407	-	-	AGTIO0	-	-	RTC _OUT	USB _VBUS	CTS4_ RTS4/ SS4	-	SDA0 _B	SSLB3 _A	-	ET0_EX XOUT	-	-	-	ADTRG 0	-	-	TS03	-	
C13	45	B11	37	26	VSS_US _B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
B14	46	A12	38	27	-	-	-	-	-	-	-	-	-	USB _DM	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A14	47	B12	39	28	-	-	-	-	-	-	-	-	-	USB _DP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B13	48	A11	40	29	VCC_US _B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
C12	49	C11	41	30	-	-	P207	A17	-	-	-	-	-	-	-	-	-	-	SSLB2 _A/QS _SL	-	-	-	-	-	-	TS02	LCD_DATA 23_B		
D12	50	B10	42	31	-	IRQ0- DS	P206	WAIT	-	-	GTIU	-	-	USB _VBUS _EN	RXD4/ MISO4 /SCL4	-	SDA1 _A	SSLB1 _A	SSIDA TA1_A	ET0_LI NKSTA _A	ET0_LI NKST _A	-	SD0 DAT2 _A	-	-	TS01	-		
E12	51	A10	43	32	CLKOUT	IRQ1- DS	P205	A16	-	AGTO1	GTIV	GTIOC 4A	-	USB _OVR CUR A-DS	TXD4/ MOS14 /SDA4	CTS9_ RTS9/ SS9	SCL1 _A	SSLB0 _A	SSILR CK1/S SIFS1 _A	ET0_W OL	ET0_W OL	-	SD0 DAT3 _A	-	-	TS00	TSCA P		
A13	52	C10	44	-	CACREF	-	P204	A18	-	AGTIO1	GTIW	GTIOC 4B	-	USB _OVR CUR B-DS	SCK4	SCK9	SCL0 _B	RSPC KB_A	SSIBC K1_A	ET0_RX _DV	-	-	-	SD0 DAT4 _A	-	-	TS00	-	
D11	53	A9	45	-	-	IRQ2- DS	P203	A19	-	-	-	GTIOC 5A	-	CTX0	CTS2_ RTS2/ SS2	TXD9/ MOS19 /SDA9	-	MOSIB _A	-	ET0_C OL	-	-	-	SD0 DAT5 _A	-	-	TS00	TSCA P	
B12	54	C9	46	-	-	IRQ3- DS	P202	WR1/ BC1	-	-	-	GTIOC 5B	-	CRX0	SCK2	RXD9/ MISO9 /SCL9	-	MISOB _A	-	ET0_ER XD2	-	-	-	SD0 DAT6 _A	-	-	-	LCD_TCO N3_B	
A12	55	B9	47	-	-	-	P313	A20	-	-	-	-	-	-	-	-	-	-	-	ET0_ER XD3	-	-	-	SD0 DAT7 _A	-	-	-	LCD_TCO N2_B	
C11	56	-	-	-	-	-	P314	A21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ADTRG 0	-	-	-	LCD_TCO N1_B	
B11	57	-	-	-	-	-	P315	A22	-	-	-	-	-	-	RXD4	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N0_B
A11	58	-	-	-	-	-	P900	A23	-	-	-	-	-	-	TXD4	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK _B
C10	59	-	-	-	-	-	P901	-	-	AGTIO1	-	-	-	-	SCK4	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 15_B
D10	60	D9	48	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	61	D8	49	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A10	62	A8	50	33	TRCLK	-	P214	-	-	-	GTIU	-	-	-	-	-	-	-	QSPC LK	ET0_M DC	ET0_M DC	-	SD0 CLK_ B	-	-	-	-	LCD_DATA 22_B	
B10	63	B8	51	34	TRDATA 0	-	P211	-	-	-	GTIV	-	-	-	-	-	-	-	-	ET0_M DIO	ET0_M DIO	-	SD0 CMD _B	-	-	-	-	LCD_DATA 21_B	
A9	64	A7	52	35	TRDATA 1	-	P210	-	-	-	GTIW	-	-	-	-	-	-	-	-	ET0_W OL	ET0_W OL	-	SD0 CD_ B	-	-	-	-	LCD_DATA 20_B	
B9	65	B7	53	36	TRDATA 2	-	P209	-	-	-	GTOVUP	-	-	-	-	-	-	-	-	ET0_EX OUT	ET0_E XOUT	-	SD0 WP_ B	-	-	-	-	LCD_DATA 19_B	

Pin number		Power, System, Clock, Debug, CAC				Interrupt	I/O port	Extbus		Timers				Communication interfaces							Analog		HMI						
BGA176	LQFP176	LG145	LQFP144	LQFP100	TRDATA3		P208	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACOMP5	CTSU	GLCDC, PDC		
A8	66	A6	54	37			P208				GTOVLO							QIO3		ET0_LI NKSTA	ET0_LI NKST A	SD0 DAT0 B					LCD_DATA 18_B		
C9	67	C7	55	38	RES																								
B8	68	B6	56	39	MD		P201																						
C8	69	C8	57	40			P200																						
D8	70						P908	CS7				GTIOC 2A																LCD_DATA 14_B	
D7	71						P907	CS6				GTIOC 2B																LCD_DATA 13_B	
A7	72						P906	CS5				GTIOC 3A																LCD_DATA 12_B	
B7	73						P905	CS4				GTIOC 3B																LCD_DATA 11_B	
C7	74	C6	58				P312	CS3	CAS	AGTOA1																			
D6	75	B5	59				P311	CS2	RAS	AGTOB1																		LCD_DATA 23_A	
A6	76	D7	60				P310	A15	A15	AGTEE1																		LCD_DATA 22_A	
B6	77	A5	61				P309	A14	A14																			LCD_DATA 21_A	
A5	78	C5	62				P308	A13	A13																			LCD_DATA 20_A	
C6	79	A4	63	41			P307	A12	A12		GTOUUP				CTS6													LCD_DATA 19_A	
A4	80	B4	64	42			P306	A11	A11		GTOULO				SCK6													LCD_DATA 18_A	
B5	81	D6	65	43			IRQ8	P305	A10	A10		GTOUUP																LCD_DATA 17_A	
B4	82	C4	66	44			IRQ9	P304	A09	A09		GTOULO	GTIOC 7A															LCD_DATA 16_A	
C5	83	A3	67	45	VSS																								
D5	84	B3	68	46	VCC																								
A3	85	D5	69	47			P303	A08	A08																			LCD_DATA 15_A	
B3	86	A2	70	48			IRQ5	P302	A07	A07		GTOUUP	GTIOC 4A															LCD_DATA 14_A	
A2	87	C3	71	49			IRQ6	P301	A06	A06	AGTIO0	GTOULO	GTIOC 4B															LCD_DATA 13_A	
C4	88	B2	72	50	TCK/SW CLK		P300				GTOUUP	GTIOC 0A_A																	
C3	89	A1	73	51	TMS/SW DIO		P108				GTOULO	GTIOC 0B_A																	
A1	90	D4	74	52	CLKOUT /TDO/S WO		P109				GTOUUP	GTIOC 1A_A																	
D3	91	B1	75	53	TDI		IRQ3	P110			GTOVLO	GTIOC 1B_A																	
D4	92	C2	76	54			IRQ4	P111	A05	A05																		LCD_DATA 12_A	
B2	93	D3	77	55				P112	A04	A04																		LCD_DATA 11_A	
B1	94	C1	78	56				P113	A03	A03																		LCD_DATA 10_A	
C2	95	E4	79	57				P114	A02	A02																		LCD_DATA 09_A	
C1	96	E3	80	58				P115	A01	A01																		LCD_DATA 08_A	
E3	97	D2	81		VCC																								
E4	98	D1	82		VSS																								
D2	99	F4	83	59				P608	A00/ BC0	A00/D QM1																		LCD_DATA 07_A	
D1	100	E2	84	60				P609	CS1	CKE																		LCD_DATA 06_A	
F3	101	F3	85	61				P610	CS0	WE																		LCD_DATA 05_A	
E2	102	E1	86		CLKOUT /CACRE F			P611		SDCS																			
E1	103	F2	87					P612	D08[A08/ D08]	DQ08																			
F4	104	F1	88					P613	D09[A09/ D09]	DQ09																			
F2	105	G3	89					P614	D10[A10/ D10]	DQ10																			
F1	106							P615																				LCD_DATA 10_B	
G1	107							PA08																				LCD_DATA 09_B	

Pin number				Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus			Timers						Communication interfaces						Analog		HMI		GLCDC, PDC	
BGA176	LQFP176	LG145	LQFP144				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU		
G4	108	-	-	-	-	PA09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 08_B	
G2	109	-	-	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 07_B	
G3	110	G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
H3	111	G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
H1	112	H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
H2	113	-	-	-	-	PA01	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 06_B	
H4	114	-	-	-	-	PA00	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 05_B	
J4	115	-	-	-	-	P607	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_B	
J1	116	-	-	-	-	P608	-	-	-	-	-	-	RTC OUT	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_B	
J2	117	H2	93	-	-	P605	D11[A11/ D11]	DQ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	118	G4	94	-	-	P604	D12[A12/ D12]	DQ12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	119	H3	95	-	-	P603	D13[A13/ D13]	DQ13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K1	120	J1	96	65	-	P602	EBC LK	SDCL K	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_A	
K2	121	J2	97	66	-	P601	WR/ WR0	DQM0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_A	
L1	122	H4	98	67	CLKOUT /CACRE F	P600	RD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 02_A	
K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
L2	125	J3	101	68	-	KR07	P107	D07[A07/ D07]	DQ07	AGTOA0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 01_A	
M1	126	K3	102	69	-	KR06	P106	D06[A06/ D06]	DQ06	AGTOB0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 00_A	
L3	127	J4	103	70	-	IRQ0/ KR05	P105	D05[A05/ D05]	DQ05	GTETRGA	GTIOC 1A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N3_A	
M2	128	L3	104	71	-	IRQ1/ KR04	P104	D04[A04/ D04]	DQ04	GTETRGA	GTIOC 1B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N2_A	
N1	129	L1	105	72	-	KR03	P103	D03[A03/ D03]	DQ03	GTOWUP	GTIOC 2A_A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N1_A	
M3	130	M1	106	73	-	KR02	P102	D02[A02/ D02]	DQ02	AGTO0	GTOWLO	GTIOC 2B_A	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N0_A	
N2	131	M2	107	74	-	IRQ1/ KR01	P101	D01[A01/ D01]	DQ01	AGTEE0	GTETRGA	GTIOC 5A	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK_ A	
P1	132	N1	108	75	-	IRQ2/ KR00	P100	D00[A00/ D00]	DQ00	AGTI00	GTETRGA	GTIOC 5B	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_EXT CLK_A	
N3	133	L2	109	-	-	-	P800	D14[A14/ D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
R1	134	N2	110	-	-	-	P801	D15[A15/ D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
P2	135	-	-	-	-	-	P802	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 02_B	
R2	136	-	-	-	-	-	P803	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 01_B	
P3	137	-	-	-	-	-	P804	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 00_B	
N4	138	N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
M4	139	M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
R3	140	K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC 11A	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 CLK_ A	
P4	141	M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC 11B	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 CMD_ A	
R4	142	L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC 12A	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT0_ A	
N5	143	K5	116	79	-	-	P503	-	-	-	GTETRGA	GTIOC 12B	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT1_ A	
P5	144	L5	117	80	-	-	P504	ALE	-	-	GTETRGA	GTIOC 13A	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT2_ A	
P6	145	K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC 13B	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT3_ A	

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

$VCC = AVCC0 = VCC_USB = VBATT = 2.7$ to 3.6 V, $2.7 \leq VREFH0/VREFH \leq AVCC0$, $VCC_USBHS = AVCC_USBHS = 3.0$ to 3.6 V, $VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0$ V, $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

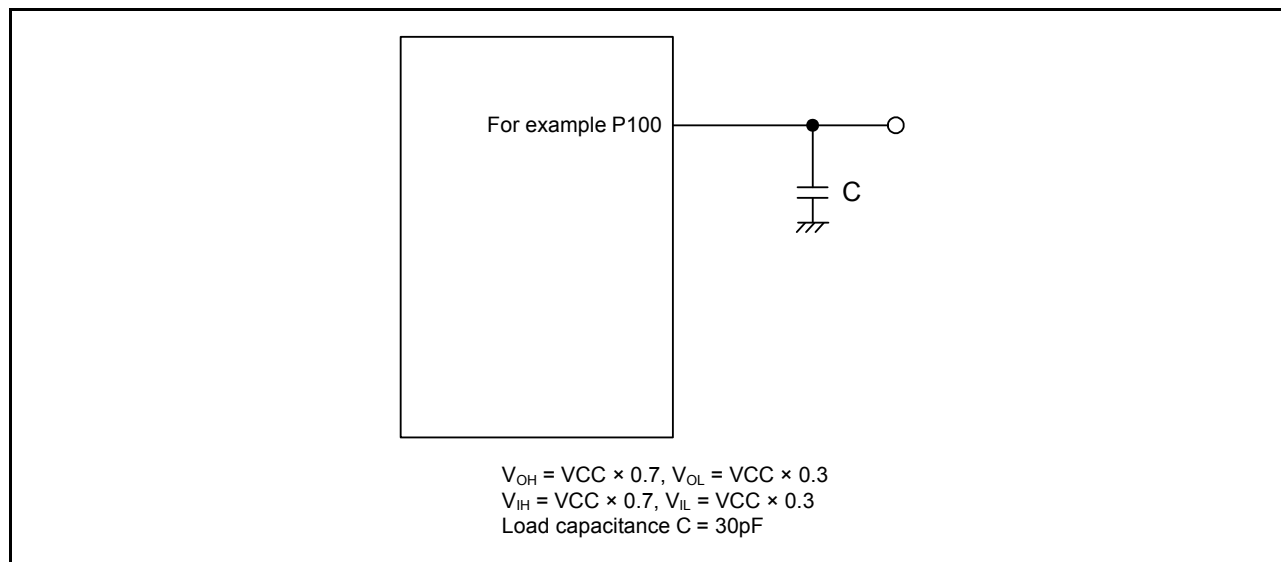


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation, however make sure to adjust driving abilities of each pins to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Item	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB *2	-0.3 to +4.0	V
VBATT power supply voltage	VBATT	-0.3 to +4.0	V
Input voltage (except for 5V-tolerant ports*1)	V_{in}	-0.3 to VCC + 0.3	V
Input voltage (5V-tolerant ports*1)	V_{in}	-0.3 to + VCC + 4.0 (max 5.8)	V
Reference power supply voltage	VREFH/VREFH0	-0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0 *2	-0.3 to +4.0	V
USBHS power supply voltage	VCC_USBHS	-0.3 to +4.0	V
USBHS analog power supply voltage	AVCC_USBHS	-0.3 to +4.0	V
Analog input voltage	V_{AN}	-0.3 to AVCC0 + 0.3	V
Operating temperature*3,*4,*5	T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, and PB01 are 5V-tolerant.

Note 2. Connect AVCC0 and VCC_USB to VCC.

Note 3. See section 2.2.1, T_j/T_a Definition.

Note 4. Contact a Renesas Electronics sales office for information on derating operation when $T_a = +85^\circ\text{C}$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for improved reliability.

Note 5. The upper limit of operating temperature is 85°C or 105°C , depending on the product. For details, see section 1.3, Part Numbering.

Table 2.2 Recommended operating conditions

Item	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/SDRAM is not used	2.7	-	3.6	V
		When USB/SDRAM is used	3.0	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB, VCC_USBHS		-	VCC	-	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		-	0	-	V
VBATT power supply voltage	VBATT		1.8	-	3.6	V
Analog power supply voltages	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter nor the comparator is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +105°C

Item	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$, where total power consumption = $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$.

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature to 85°C, then T_j max is 105°C, otherwise, 125°C.

2.2.2 I/O V_{IH} , V_{IL} Table 2.4 I/O V_{IH} , V_{IL}

Item				Symbol	Min	Typ	Max	Unit	
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), WAIT, SPI (except RSPCK)		V_{IH}	$VCC \times 0.8$	-	-	V	
				V_{IL}	-	-	$VCC \times 0.2$		
		D00 to D15, DQ00 to DQ15		V_{IH}	$VCC \times 0.7$	-	-		
				V_{IL}	-	-	$VCC \times 0.3$		
		ETHERC		V_{IH}	2.3	-	-		
				V_{IL}	-	-	$VCC \times 0.2$		
		IIC (SMBus)*1		V_{IH}	2.1	-	-		
				V_{IL}	-	-	0.8		
		IIC (SMBus)*2		V_{IH}	2.1	-	$VCC + 3.6$ (max 5.8)		
				V_{IL}	-	-	0.8		
		Schmitt trigger input voltage	IIC (except for SMBus)*1		V_{IH}	$VCC \times 0.7$	-		-
					V_{IL}	-	-		$VCC \times 0.3$
ΔV_T	$VCC \times 0.05$				-	-			
IIC (except for SMBus)*2			V_{IH}	$VCC \times 0.7$	-	$VCC + 3.6$ (max 5.8)			
			V_{IL}	-	-	$VCC \times 0.3$			
			ΔV_T	$VCC \times 0.05$	-	-			
5V-tolerant ports*3, *7			V_{IH}	$VCC \times 0.8$	-	$VCC + 3.6$ (max 5.8)			
			V_{IL}	-	-	$VCC \times 0.2$			
			ΔV_T	$VCC \times 0.05$	-	-			
RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function		When VBATT power supply is selected		V_{IH}	$V_{BATT} \times 0.8$	-	$V_{BATT} + 0.3$	
					V_{IL}	-	-	$V_{BATT} \times 0.2$	
					ΔV_T	$V_{BATT} \times 0.05$	-	-	
			When VCC power supply is selected		V_{IH}	$VCC \times 0.8$	-	Higher voltage either $VCC + 0.3$ V or $V_{BATT} + 0.3$ V	
					V_{IL}	-	-	$VCC \times 0.2$	
					ΔV_T	$VCC \times 0.05$	-	-	
	When not using the Battery Backup Function		V_{IH}	$VCC \times 0.8$	-	$VCC + 0.3$			
			V_{IL}	-	-	$VCC \times 0.2$			
			ΔV_T	$VCC \times 0.05$	-	-			
	Other input pins*4		V_{IH}	$VCC \times 0.8$	-	-			
			V_{IL}	-	-	$VCC \times 0.2$			
			ΔV_T	$VCC \times 0.05$	-	-			
Ports	5V-tolerant ports*5, *7		V_{IH}	$VCC \times 0.8$	-	$VCC + 3.6$ (max 5.8)			
			V_{IL}	-	-	$VCC \times 0.2$			
			ΔV_T	$VCC \times 0.05$	-	-			
	Other input pins*6		V_{IH}	$VCC \times 0.8$	-	-			
			V_{IL}	-	-	$VCC \times 0.2$			
			ΔV_T	$VCC \times 0.05$	-	-			

Note 1. SCL0_B (P204), SCL1_B, SDA1_B (total 3 pins).

Note 2. SCL0_A, SDA0_A, SCL0_B (P408), SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 8 pins).

Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 23 pins).

Note 4. All input pins except for the peripheral function pins already described in the table.

Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22 pins).

Note 6. All input pins except for the ports already described in the table.

Note 7. When VCC is less than 2.7 V, the input voltage of 5V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O I_{OH} , I_{OL}

Table 2.5 I/O I_{OH} , I_{OL}

Item			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P008 to P010, P201	-	I_{OH}	-	--	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA
Permissible output current (max value per pin)	Ports P008 to P010, P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
Permissible output current (max value total pins)	Maximum of all output pins		$\Sigma I_{OH} (max)$	-	-	-80	mA
			$\Sigma I_{OL} (max)$	-	-	80	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 μ s.

Note 1. This is the value when low driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 2. This is the value when middle driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. Except for P000 to P007, P200, which are input ports.

2.2.4 I/O V_{OH} , V_{OL} , and Other Characteristics

Table 2.6 I/O V_{OH} , V_{OL} , and other characteristics

Item		Symbol	Min	Typ	Max	Unit	Test conditions	
Output voltage	IIC	V_{OL}	-	-	0.4	V	$I_{OL} = 3.0 \text{ mA}$	
		V_{OL}	-	-	0.6		$I_{OL} = 6.0 \text{ mA}$	
	IIC*1	V_{OL}	-	-	0.4		$I_{OL} = 15.0 \text{ mA}$ (ICFER.FMPE = 1)	
		V_{OL}	-	0.4	-		$I_{OL} = 20.0 \text{ mA}$ (ICFER.FMPE = 1)	
	ETHERC	V_{OH}	$VCC - 0.5$	-	-		$I_{OH} = -1.0 \text{ mA}$	
		V_{OL}	-	-	0.4		$I_{OL} = 1.0 \text{ mA}$	
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)*2	V_{OH}	$VCC - 1.0$	-	-		$I_{OH} = -20 \text{ mA}$ $VCC = 3.3 \text{ V}$	
		V_{OL}	-	-	1.0		$I_{OL} = 20 \text{ mA}$ $VCC = 3.3 \text{ V}$	
	Other output pins	V_{OH}	$VCC - 0.5$	-	-		$I_{OH} = -1.0 \text{ mA}$	
		V_{OL}	-	-	0.5		$I_{OL} = 1.0 \text{ mA}$	
Input leakage current	RES	$ I_{in} $	-	-	5.0	μA	$V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$	
	Ports P000 to P002, P004 to P006, P200		-	-	1.0		$V_{in} = 0 \text{ V}$ $V_{in} = VCC$	
	Ports P003, P007		Before initialization	-	-		45.0	$V_{in} = 0 \text{ V}$ $V_{in} = VCC$
			After initialization	-	-		1.0	$V_{in} = 0 \text{ V}$ $V_{in} = VCC$
Three-state leakage current (off state)	5V-tolerant ports	$ I_{TS} $	-	-	5.0	μA	$V_{in} = 0 \text{ V}$ $V_{in} = 5.5 \text{ V}$	
	Other ports (except for ports P000 to P007, P200)		-	-	1.0		$V_{in} = 0 \text{ V}$ $V_{in} = VCC$	
Input pull-up MOS current	Ports P0 to PB (except for ports P000 to P007)	I_p	-300	-	-10	μA	$VCC = 2.7 \text{ to } 3.6 \text{ V}$ $V_{in} = 0 \text{ V}$	
Input capacitance	USB_DP, USB_DM, and ports P003, P007, P014, P015, P400, P401, P511, P512	C_{in}	-	-	16	pF	$V_{bias} = 0 \text{ V}$ $V_{amp} = 20 \text{ mV}$ $f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$	
	Other input pins		-	-	8			

Note 1. SCL0_A, SDA0_A (total 2 pins).

Note 2. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current (1 of 2)

Item	Symbol	Min	Typ	Max	Unit	Test conditions								
Supply current*1	I_{CC} *3	-	-	137*2	mA	ICLK = 120 MHz PCLKA = 120 MHz*7 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz								
							Maximum*2							
							CoreMark®*5							
							Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4						
								All peripheral clocks disabled, while (1) code executing from flash*5, *6						
							Sleep mode*5, *6							
							Increase during BGO operation	Data flash P/E						
								Code flash P/E						
							Low-speed mode*5							
							Subosc-speed mode*5							
							Software Standby mode							
							Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit	-	30	113	μ A	-	
								Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low-power function disabled	-	13			40
									Power-on reset circuit low-power function enabled	-	6.3			34
								Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use	-	5			-
When a crystal oscillator for low clock loads is in use	-	1.0	-											
When a crystal oscillator for standard clock loads is in use	-	1.5	-											
RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use	-	0.9	-	$V_{BATT} = 1.8$ V, $V_{CC} = 0$ V									
		-	1.3	-	$V_{BATT} = 3.3$ V, $V_{CC} = 0$ V									
	When a crystal oscillator for standard clock loads is in use	-	1.1	-	$V_{BATT} = 1.8$ V, $V_{CC} = 0$ V									
-	-	1.8	-	$V_{BATT} = 3.3$ V, $V_{CC} = 0$ V										
Analog power supply current	I_{CC}	-	-	-	mA	-								
							During 12-bit A/D conversion							
							During 12-bit A/D conversion with S/H amp							
							PGA (1ch)							
							ACMPHS (1unit)							
							Temperature sensor							
							During D/A conversion (per unit)	Without AMP output						
								With AMP output						
							Waiting for A/D, D/A conversion (all units)							
							ADC12, DAC12 in standby modes (all units)*8							
Reference power supply current (VREFH0)	I_{REFH0}	-	-	-	μ A	-								
							During 12-bit A/D conversion (unit 0)							
							Waiting for 12-bit A/D conversion (unit 0)							
ADC12 in standby modes (unit 0)														
Reference power supply current (VREFH)	I_{REFH}	-	-	-	μ A	-								
							During 12-bit A/D conversion (unit 1)							
							During D/A conversion (per unit)	Without AMP output						
								With AMP output						
							Waiting for 12-bit A/D (unit 1), D/A (all units) conversion							
ADC12 unit 1 in standby modes														

Table 2.7 Operating and standby current (2 of 2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions	
USB operating current	Low speed	USB	I _{CCUSBLS}	-	3.5	6.5	mA	VCC_USB
		USBHS		-	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	Full speed	USB	I _{CCUSBFS}	-	4.0	10.0	mA	VCC_USB
		USBHS		-	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	High speed	USBHS	I _{CCUSBHS}	-	50	65	mA	VCC_USBHS = AVCC_USBHS
	Standby mode (direct power down)	USBHS	I _{CCUSBSBY}	-	0.5	4.5	μA	VCC_USBHS = AVCC_USBHS

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. ICC depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK = 2:2:1:1:2:1:1)

ICC Max. = $0.84 \times f + 37$ (max. operation in High-speed mode)

ICC Typ. = $0.09 \times f + 3.7$ (normal operation in High-speed mode)

ICC Typ. = $0.6 \times f + 1.8$ (Low-speed mode 1)

ICC Max. = $0.08 \times f + 37$ (Sleep mode).

Note 4. This does not include the BGO operation.

Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).

Note 7. When using ETHERC, GLCDC, DRW, and JPEG, PCLKA frequency is such that PCLKA = ICLK.

Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module stop bit) and MSTPCRD.MSTPD15 (ADC121 module stop bit) are in the module stop state.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.8 Rise and fall gradient characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	-	20	ms/V
	Voltage monitor 0 reset enabled at startup		0.0084	-	-	
	SCI/USB boot mode*1		0.0084	-	20	
VCC falling gradient*2	SfVCC	0.0084	-	-	ms/V	-

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Note 2. This applies when VBATT is used.

Table 2.9 Rise and fall gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC $\pm 10\%$, the allowable voltage change rising and falling gradient $dt/dVCC$ must be met.

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	-	-	10	kHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.2 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	$dt/dVCC$	1.0	-	-	ms/V	When VCC change exceeds VCC $\pm 10\%$

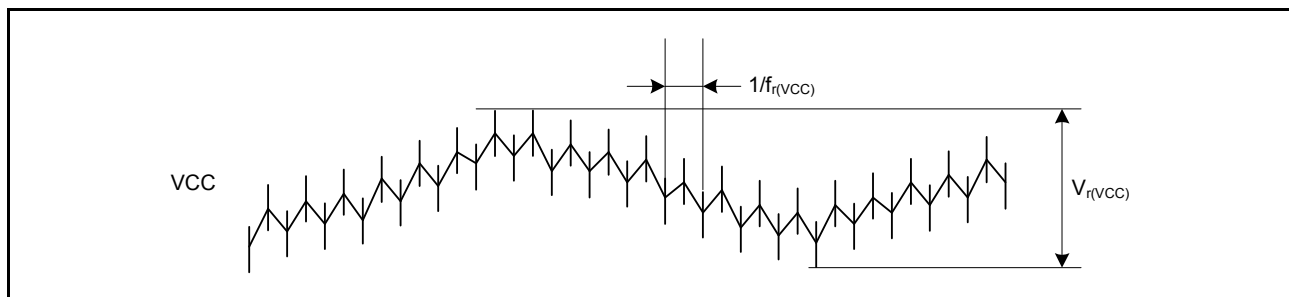


Figure 2.2 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.10 Operation frequency value in high-speed mode

Item	Symbol	Min	Typ	Max	Unit	
Operation frequency	System clock (ICLK)*2	f	-	-	120	MHz
	Peripheral module clock (PCLKA)*2		-	-	120	
	Peripheral module clock (PCLKB)*2		-	-	60	
	Peripheral module clock (PCLKC)*2		-*3	-	60	
	Peripheral module clock (PCLKD)*2		-	-	120	
	Flash interface clock (FCLK)*2		-*1	-	60	
	External bus clock (BCLK)*2		-	-	120	
	EBCLK pin output		-	-	60	
SDCLK pin output	VCC ≥ 3.0 V		-	-	120	

- Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
 Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
 Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.11 Operation frequency value in low-speed mode

Item	Symbol	Min	Typ	Max	Unit	
Operation frequency	System clock (ICLK)*2	f	-	-	1	MHz
	Peripheral module clock (PCLKA)*2	-	-	1		
	Peripheral module clock (PCLKB)*2	-	-	1		
	Peripheral module clock (PCLKC)*2, *3	~*3	-	1		
	Peripheral module clock (PCLKD)*2	-	-	1		
	Flash interface clock (FCLK)*1, *2	-	-	1		
	External bus clock (BCLK)	-	-	1		
	EBCLK pin output	-	-	1		

- Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
 Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
 Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 2.12 Operation frequency value in Subosc-speed mode

Item	Symbol	Min	Typ	Max	Unit	
Operation frequency	System clock (ICLK)*2	f	27.8	-	37.7	kHz
	Peripheral module clock (PCLKA)*2	-	-	37.7		
	Peripheral module clock (PCLKB)*2	-	-	37.7		
	Peripheral module clock (PCLKC)*2, *3	-	-	37.7		
	Peripheral module clock (PCLKD)*2	-	-	37.7		
	Flash interface clock (FCLK)*1, *2	27.8	-	37.7		
	External bus clock (BCLK)*2	-	-	37.7		
	EBCLK pin output	-	-	37.7		

- Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
 Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
 Note 3. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.13 Clock timing except for sub-clock oscillator (1 of 2)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	t_{Bcyc}	16.6	-	-	ns	Figure 2.3
EBCLK pin output high pulse width	t_{CH}	3.3	-	-	ns	
EBCLK pin output low pulse width	t_{CL}	3.3	-	-	ns	
EBCLK pin output rise time	t_{Cr}	-	-	5.0	ns	
EBCLK pin output fall time	t_{Cf}	-	-	5.0	ns	
SDCLK pin output cycle time	t_{SDcyc}	8.33	-	-	ns	
SDCLK pin output high pulse width	t_{CH}	1.0	-	-	ns	
SDCLK pin output low pulse width	t_{CL}	1.0	-	-	ns	
SDCLK pin output rise time	t_{Cr}	-	-	3.0	ns	
SDCLK pin output fall time	t_{Cf}	-	-	3.0	ns	

Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
EXTAL external clock input cycle time	t_{EXCyc}	41.66	-	-	ns	Figure 2.4	
EXTAL external clock input high pulse width	t_{EXH}	15.83	-	-	ns		
EXTAL external clock input low pulse width	t_{EXL}	15.83	-	-	ns		
EXTAL external clock rise time	t_{EXr}	-	-	5.0	ns		
EXTAL external clock fall time	t_{EXf}	-	-	5.0	ns		
Main clock oscillator frequency	f_{MAIN}	8	-	24	MHz	-	
Main clock oscillation stabilization wait time (crystal) *1	$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 2.5	
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	-	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	-	-	60.4	μ s	Figure 2.6	
ILOCO clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	-	
MOCO clock oscillation frequency	F_{MOCO}	6.8	8	9.2	MHz	-	
MOCO clock oscillation stabilization wait time	t_{MOCOWT}	-	-	15.0	μ s	-	
HOCO clock oscillator oscillation frequency	Without FLL*2	f_{HOCO16}	15.78	16	16.22	MHz	$-20 \leq Ta \leq 105^{\circ}C$
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		$-40 \leq Ta \leq -20^{\circ}C$
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045	MHz	$-40 \leq Ta \leq -105^{\circ}C$ Sub-clock frequency accuracy is ± 50 ppm.
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	-	-	64.7	μ s	-	
FLL stabilization wait time	t_{FLLWT}	-	-	1.8	ms	-	
PLL clock frequency	f_{PLL}	120	-	240	MHz	-	
PLL clock oscillation stabilization wait time	t_{PLLWT}	-	-	174.9	μ s	Figure 2.7	

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.

After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.14 Clock timing for the sub-clock oscillator

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	-*Note:	s	-

Note: When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.

After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. Two times the value shown is recommended.

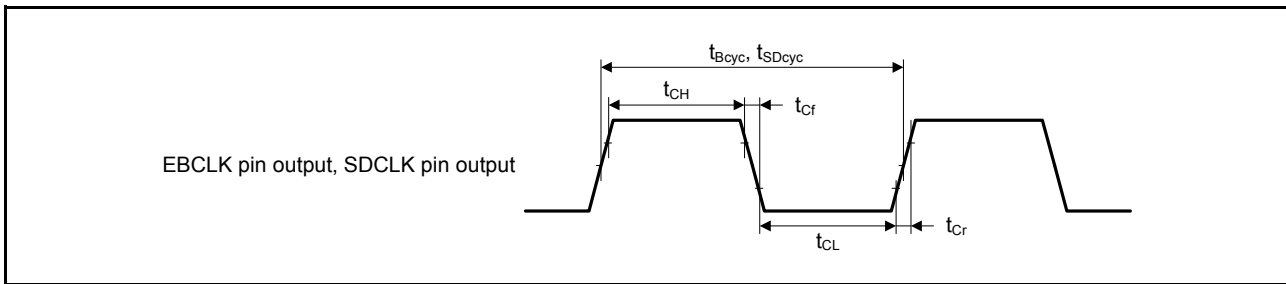


Figure 2.3 EBCLK and SDCLK output timing

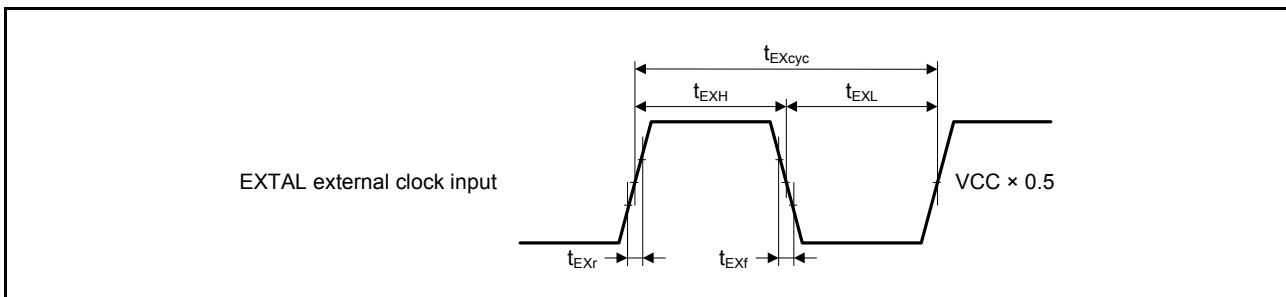


Figure 2.4 EXTAL external clock input timing

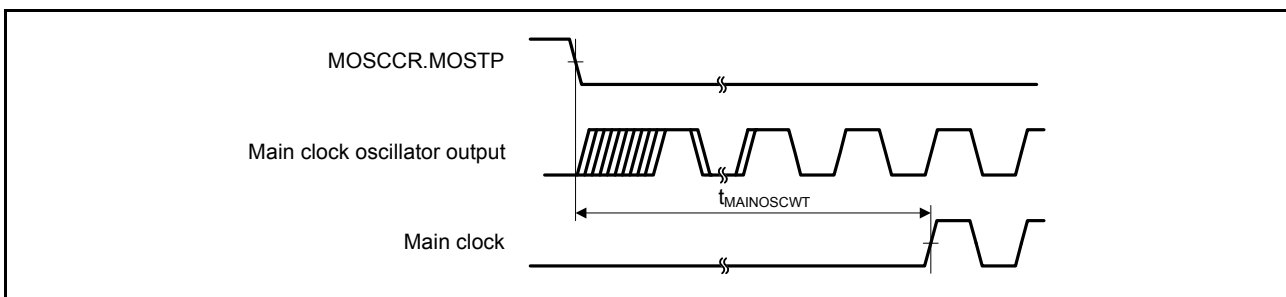


Figure 2.5 Main clock oscillation start timing

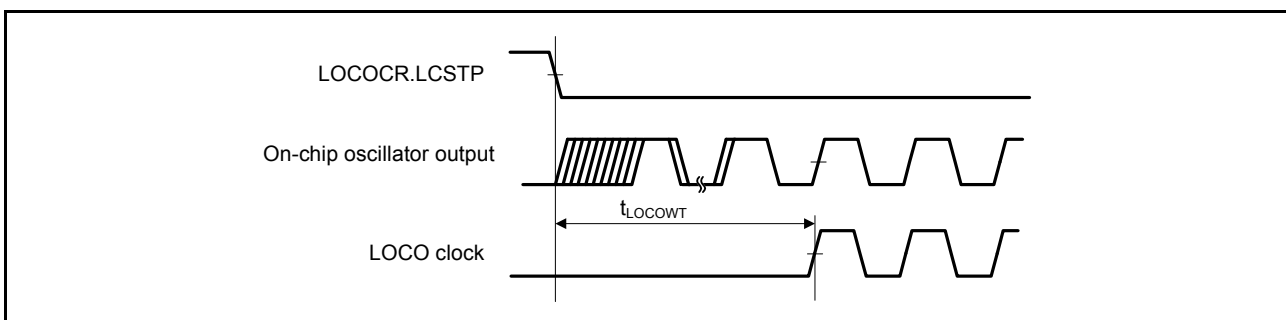


Figure 2.6 LOCO clock oscillation start timing

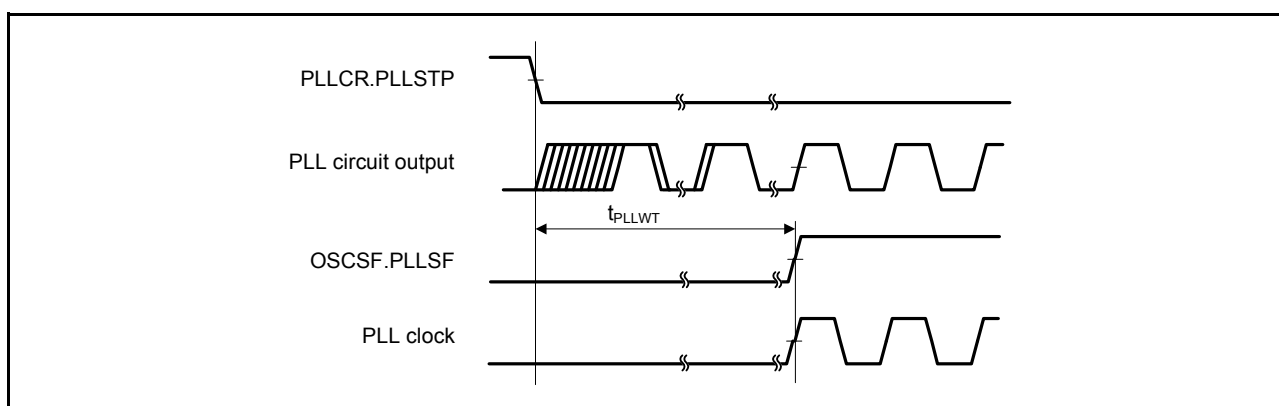


Figure 2.7 PLL clock oscillation start timing

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

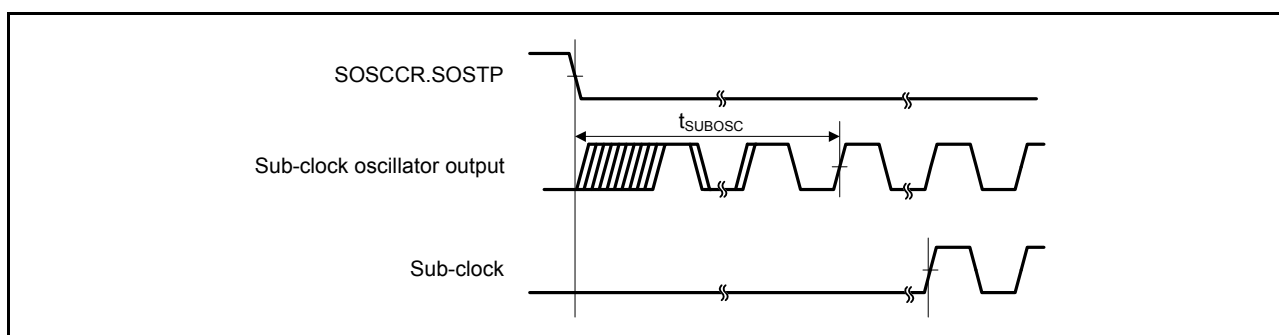


Figure 2.8 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.15 Reset timing

Item		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	1	-	-	ms	Figure 2.9
	Deep Software Standby mode	t_{RESWD}	0.6	-	-	ms	Figure 2.10
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	-	-	ms	
	All other	t_{RESW}	200	-	-	μ s	
Wait time after RES cancellation		t_{RESWT}	-	29	33	μ s	Figure 2.9
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)		t_{RESW2}	-	320	408	μ s	-

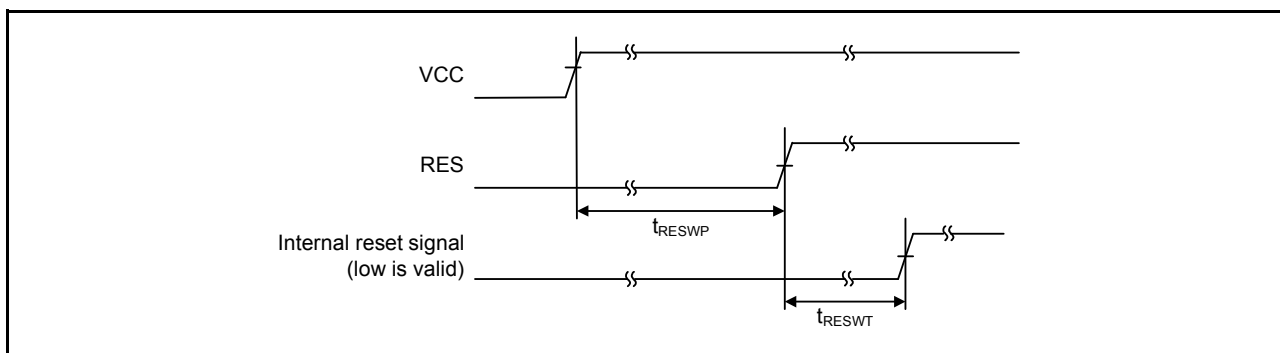


Figure 2.9 Power-on reset timing

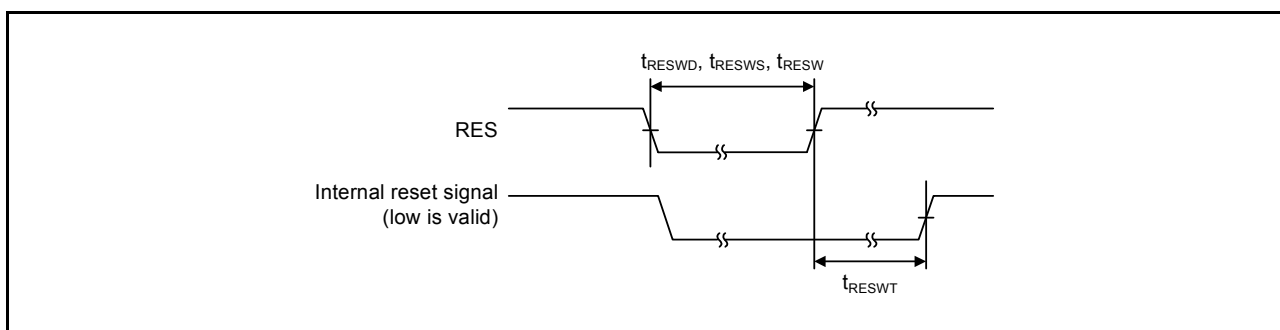


Figure 2.10 Reset input timing

2.3.4 Wakeup Timing

Table 2.16 Timing of recovery from low-power modes

Item	Symbol	Min	Typ	Max	Unit	Test conditions		
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	Figure 2.11 The division ratio of all oscillators is 1.
	System clock source is PLL with main clock oscillator*3		t_{SBYPC}	-	2.7*9	3.2*9	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}	-	230*9	280*9	μ s	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}	-	570*9	700*9	μ s	
	System clock source is sub-clock oscillator*8	t_{SBYSC}	-	1.2*9	1.3*9	ms		
	System clock source is LOCO*8	t_{SBYLO}	-	1.2*9	1.4*9	ms		
	System clock source is HOCO clock oscillator*6	t_{SBYHO}	-	240*9, *10	310*9, *10	μ s		
System clock source is MOCO clock oscillator*7	t_{SBYMO}	-	220*9	300*9	μ s			
Recovery time from Deep Software Standby mode	t_{DSBY}	-	0.65	1.0	ms	Figure 2.12		
Wait time after cancellation of Deep Software Standby mode	t_{DSBYWT}	34	-	35	t_{cyc}			
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)	t_{SNZ}	-	35*9, *10	71*9, *10	μ s	Figure 2.13	
	High-speed mode when system clock source is MOCO (8 MHz)	t_{SNZ}	-	11*9	14*9	μ s		

- Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSOC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).
- Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
 $t_{\text{SBYMC}}(\text{MOSCWTCR} = \text{Xh}) = t_{\text{SBYMC}}(\text{MOSCWTCR} = 05\text{h}) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = \text{Xh}) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 05\text{h}))$
- Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
 $t_{\text{SBYMC}}(\text{MOSCWTCR} = \text{Xh}) = t_{\text{SBYMC}}(\text{MOSCWTCR} = 05\text{h}) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = \text{Xh}) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 05\text{h}))$
- Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
 $t_{\text{SBYMC}}(\text{MOSCWTCR} = \text{Xh}) = t_{\text{SBYMC}}(\text{MOSCWTCR} = 00\text{h}) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = \text{Xh}) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 00\text{h}))$
- Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
 $t_{\text{SBYMC}}(\text{MOSCWTCR} = \text{Xh}) = t_{\text{SBYMC}}(\text{MOSCWTCR} = 00\text{h}) + (t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = \text{Xh}) - t_{\text{MAINOSCWT}}(\text{MOSCWTCR} = 00\text{h}))$
- Note 6. The HOCO frequency is 20 MHz.
- Note 7. The MOCO frequency is 8 MHz.
- Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
- Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:
STCONR.STCON[1:0] = 00b:16 μ s (typical), 34 μ s (maximum)
STCONR.STCON[1:0] = 11b:16 μ s (typical), 104 μ s (maximum).
- Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 μ s (typical) or 18 μ s (maximum) is added as the HOCO wait time.

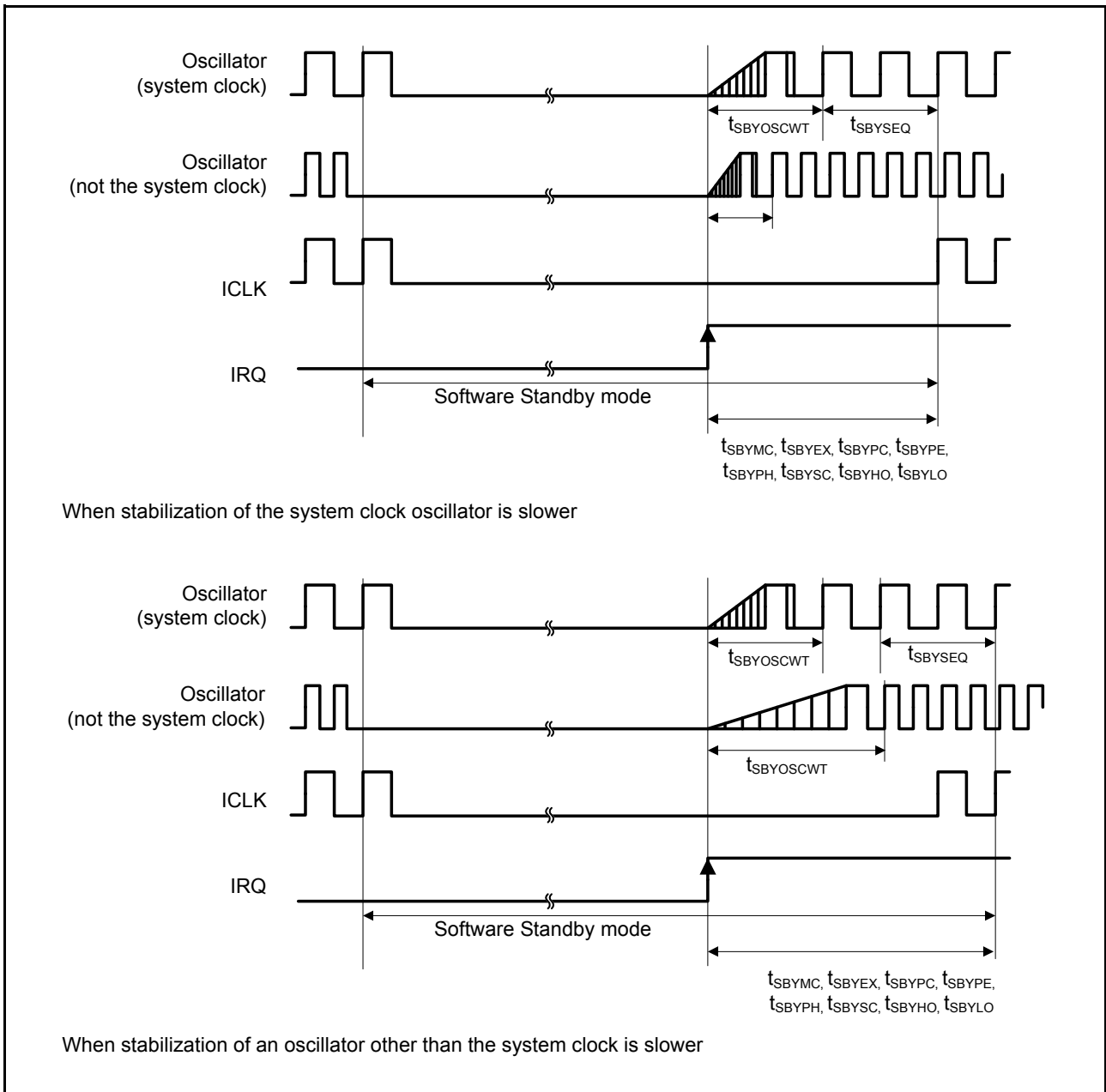


Figure 2.11 Software Standby mode cancellation timing

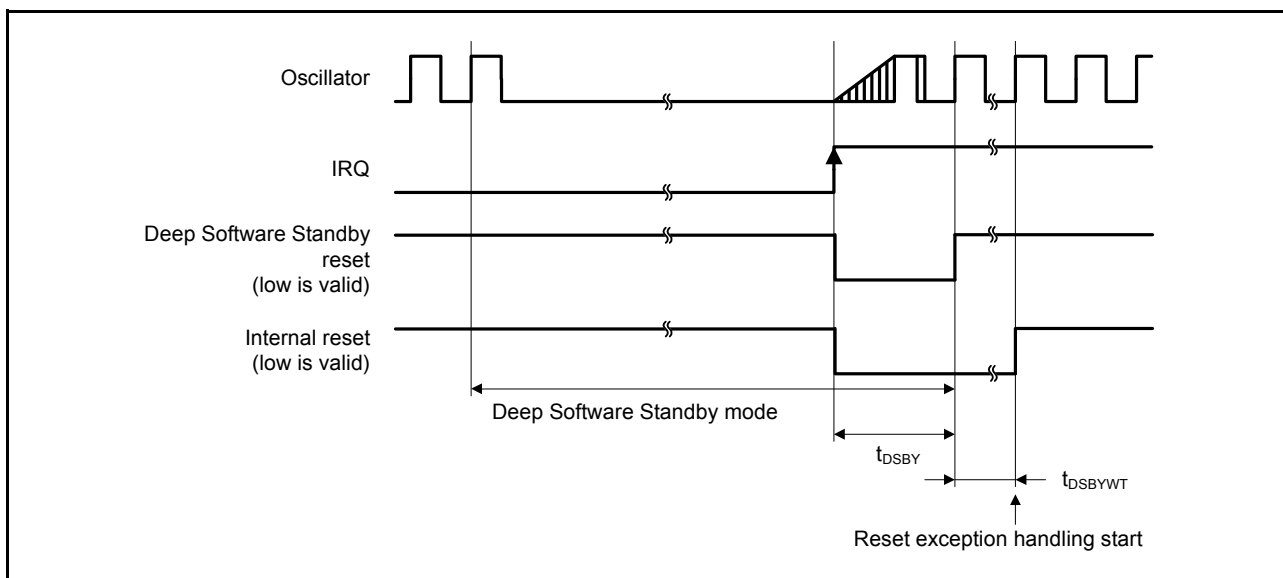


Figure 2.12 Deep Software Standby mode cancellation timing

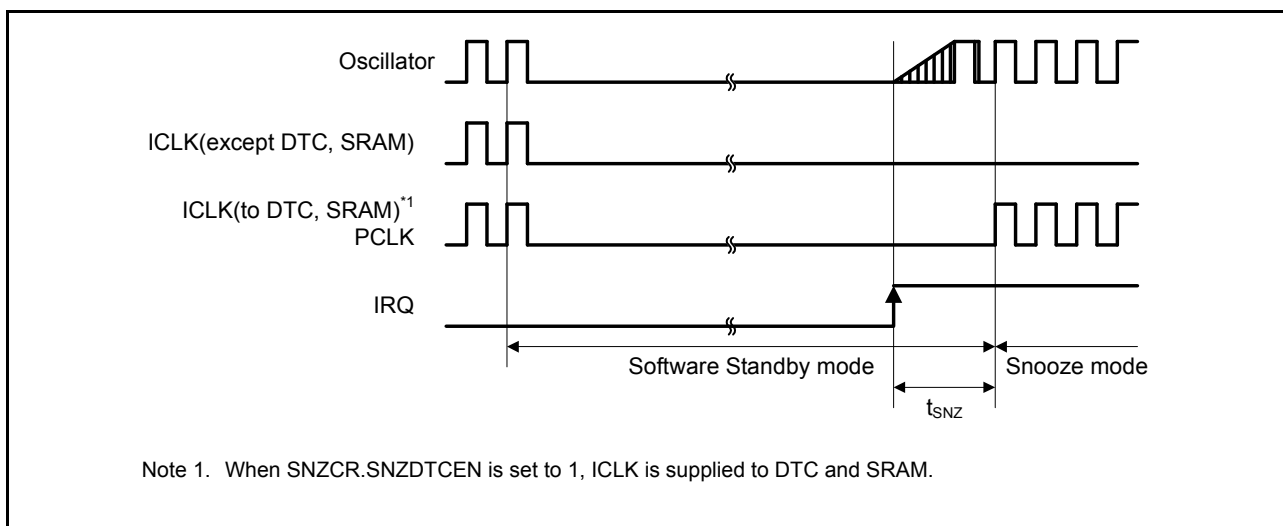


Figure 2.13 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.

Note 1. t_{Pcyc} indicates the PCLKB cycle.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

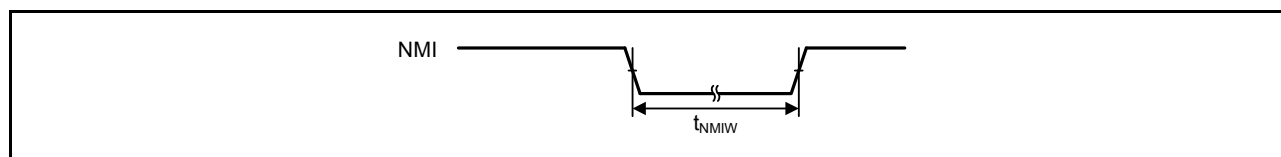


Figure 2.14 NMI interrupt input timing

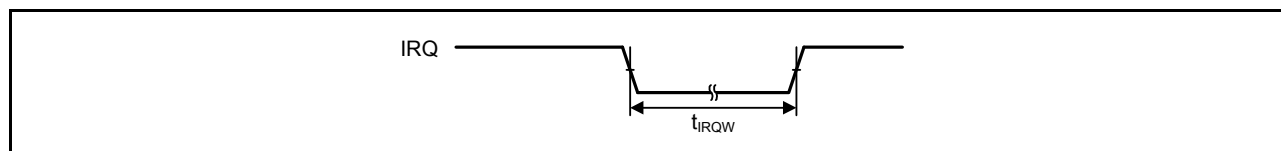


Figure 2.15 IRQ interrupt input timing

2.3.6 Bus Timing

Table 2.18 Bus timing (1 of 2)

Condition 1: When using the CS area controller (CSC).

BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF

EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.

Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).

BCLK = SDCLK = 8 to 120 MHz

VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF

High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.

BCLK = SDCLK = 8 to 60 MHz

VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF

High drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	12.5	ns	Figure 2.18 to Figure 2.21
Byte control delay	t_{BCD}	-	12.5	ns	
CS delay	t_{CSD}	-	12.5	ns	
ALE delay time	t_{ALED}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
Read data setup time	t_{RDS}	12.5	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR/WRn delay	t_{WRD}	-	12.5	ns	
Write data delay	t_{WDD}	-	12.5	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	12.5	-	ns	
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.18 Bus timing (2 of 2)

Condition 1: When using the CS area controller (CSC).

BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF

EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.

Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).

BCLK = SDCLK = 8 to 120 MHz

VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF

High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.

BCLK = SDCLK = 8 to 60 MHz

VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,

VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V

Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF

High drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit	Test conditions
Address delay 2 (SDRAM)	t _{AD2}	0.8	6.8	ns	Figure 2.23 to Figure 2.29
CS delay 2 (SDRAM)	t _{CSD2}	0.8	6.8	ns	
DQM delay (SDRAM)	t _{DQMD}	0.8	6.8	ns	
CKE delay (SDRAM)	t _{CKED}	0.8	6.8	ns	
Read data setup time 2 (SDRAM)	t _{RDS2}	2.9	-	ns	
Read data hold time 2 (SDRAM)	t _{RDH2}	1.5	-	ns	
Write data delay 2 (SDRAM)	t _{WDD2}	-	6.8	ns	
Write data hold time 2 (SDRAM)	t _{WDH2}	0.8	-	ns	
WE delay (SDRAM)	t _{WED}	0.8	6.8	ns	
RAS delay (SDRAM)	t _{RASD}	0.8	6.8	ns	
CAS delay (SDRAM)	t _{CASD}	0.8	6.8	ns	

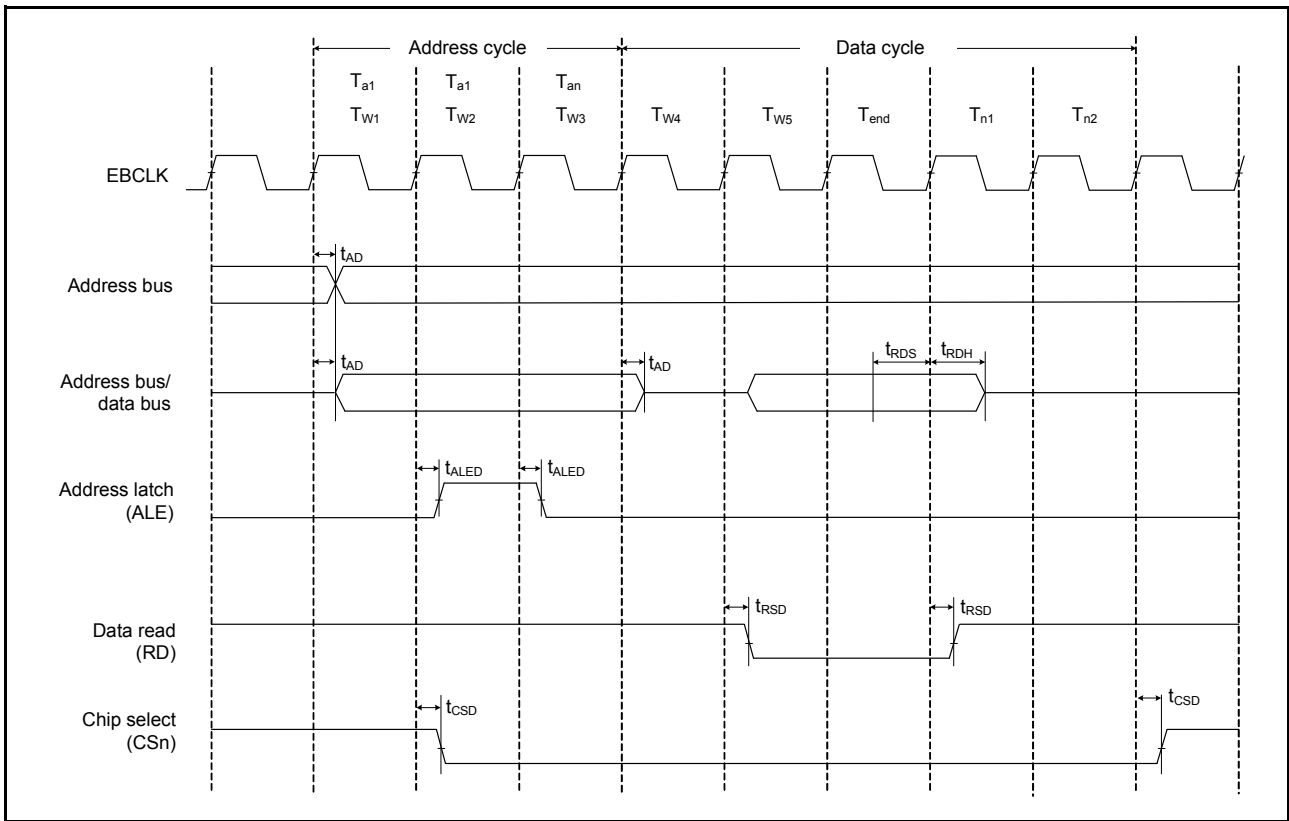


Figure 2.16 Address/data multiplexed bus read access timing

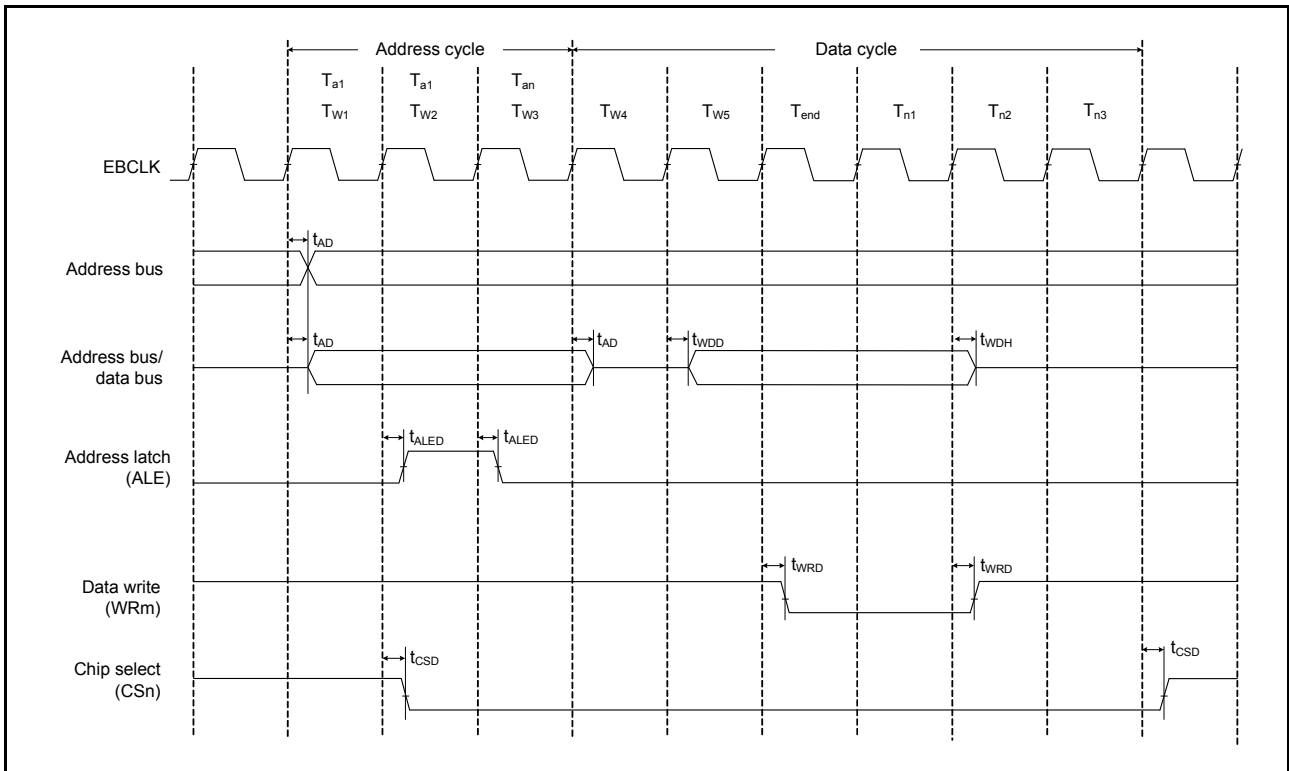


Figure 2.17 Address/data multiplexed bus write access timing

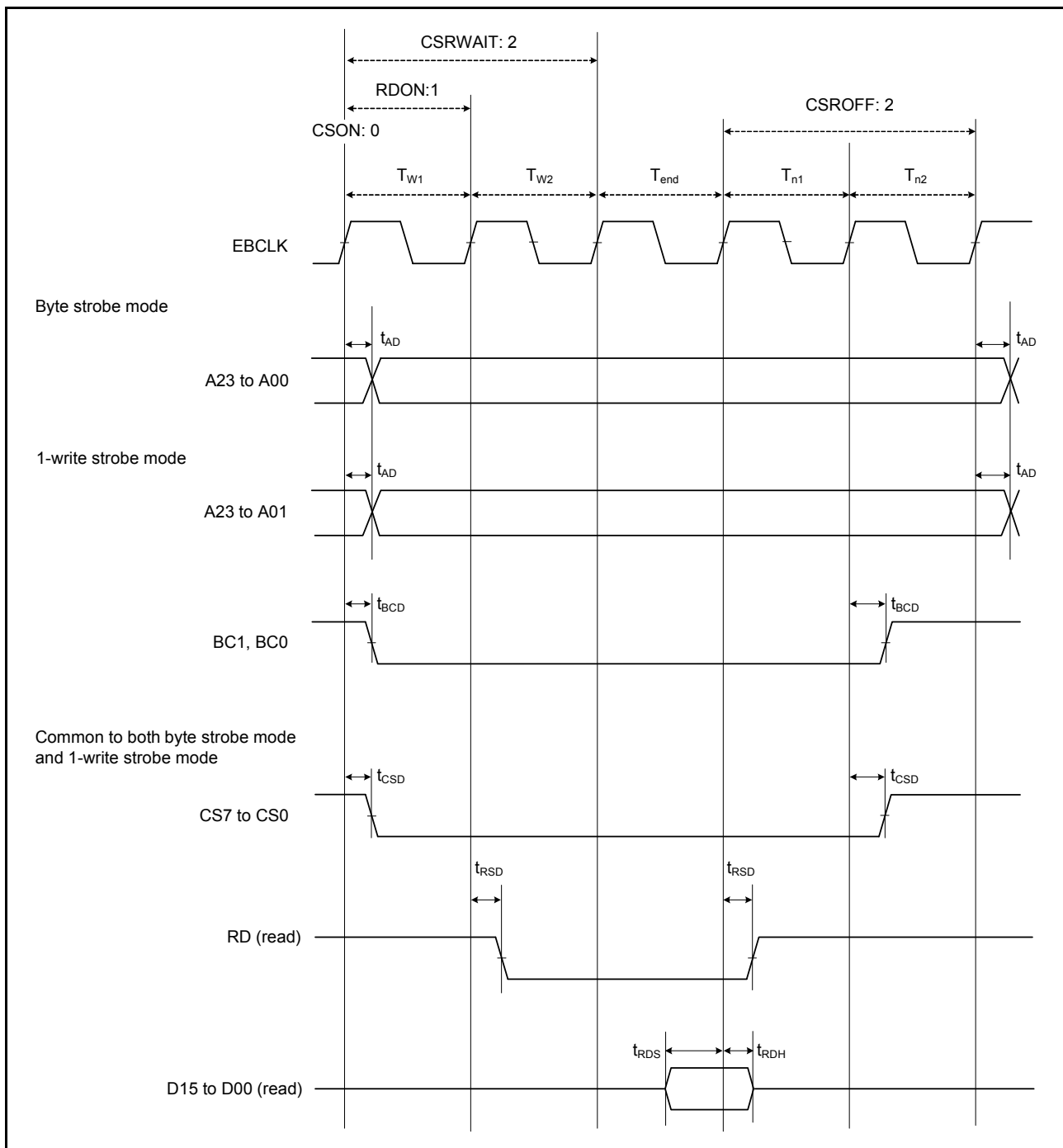


Figure 2.18 External bus timing for normal read cycle with bus clock synchronized

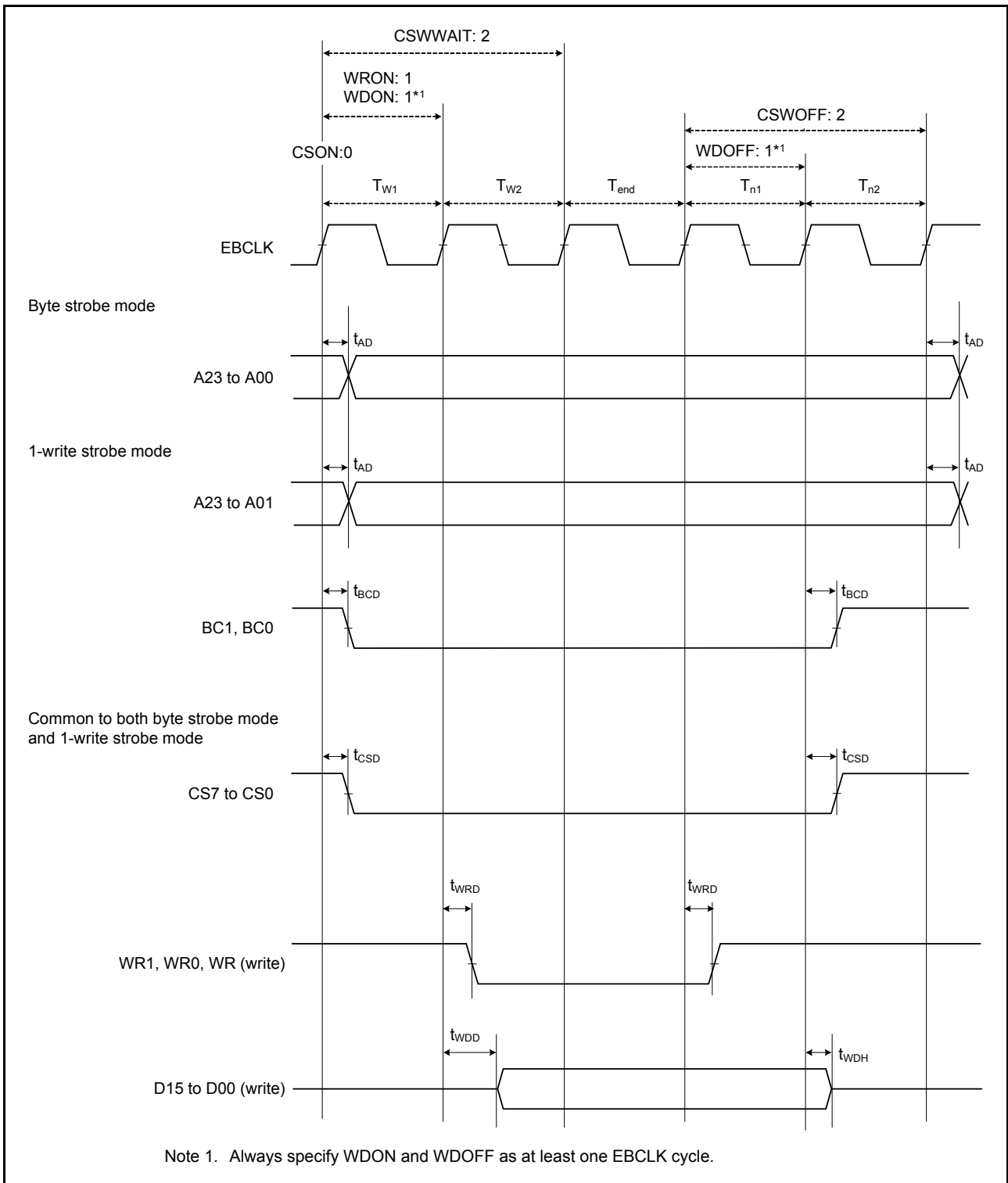


Figure 2.19 External bus timing for normal write cycle with bus clock synchronized

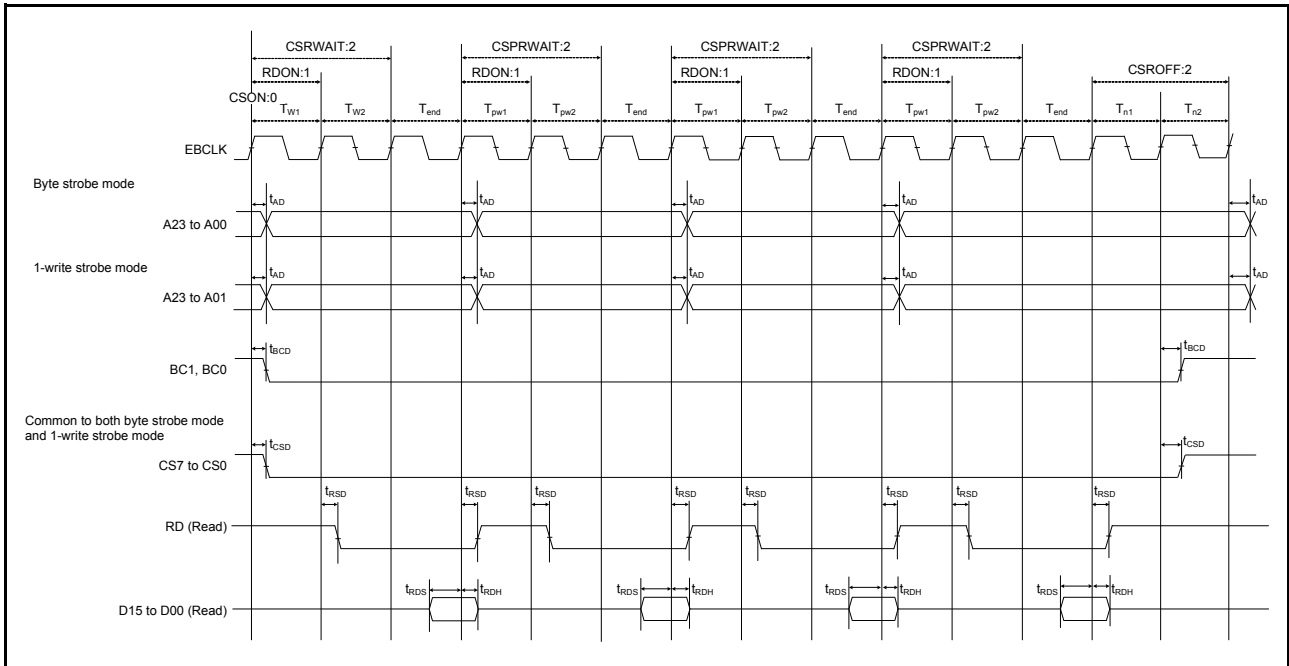
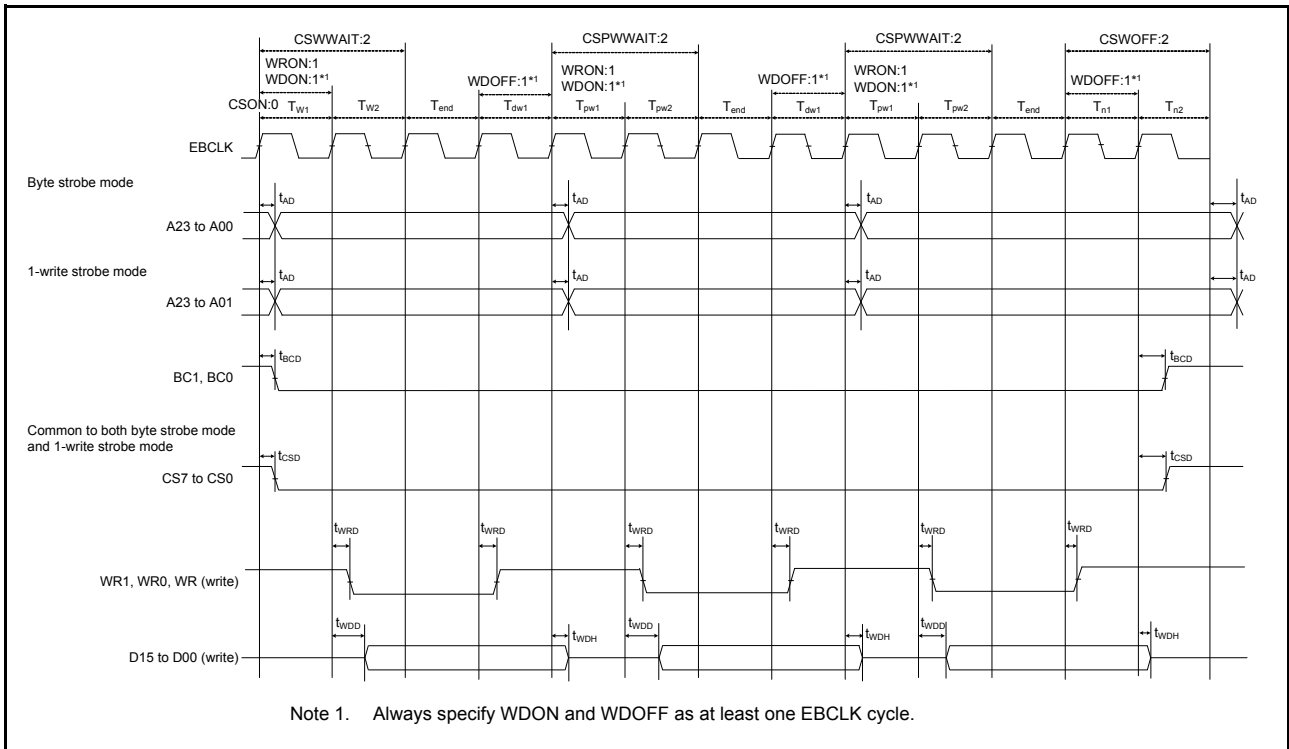


Figure 2.20 External bus timing for page read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.21 External bus timing for page write cycle with bus clock synchronized

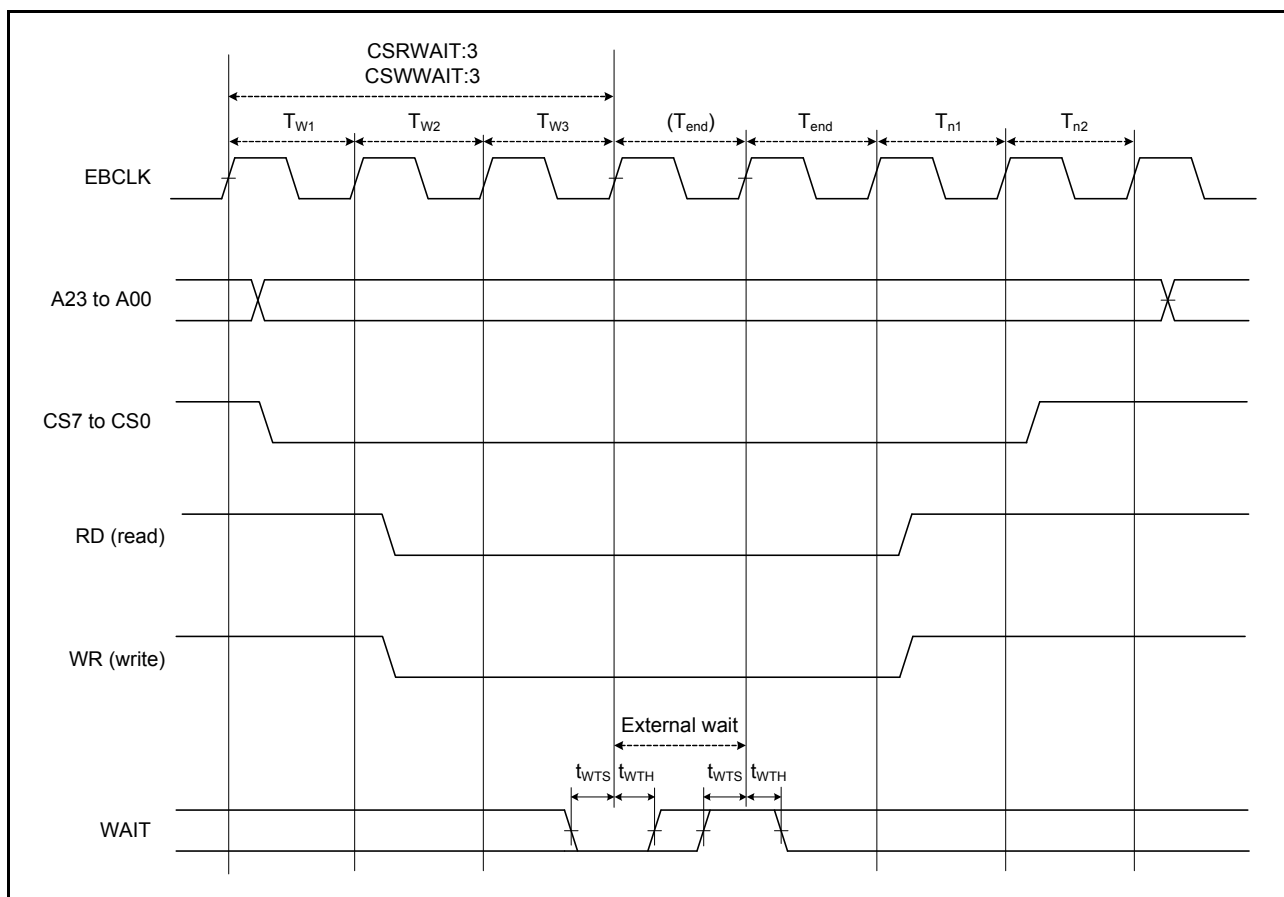


Figure 2.22 External bus timing for external wait control

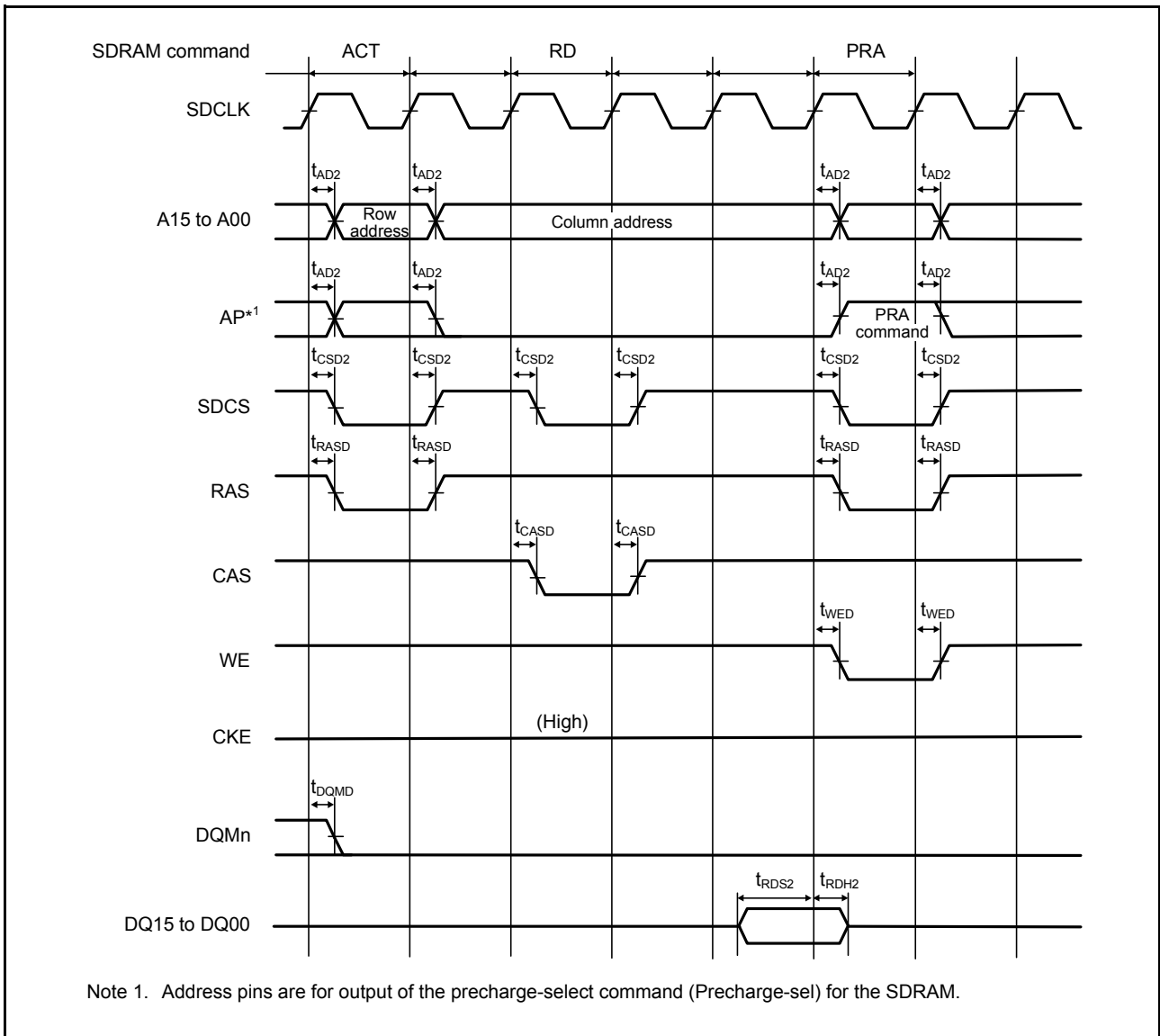


Figure 2.23 SDRAM single read timing

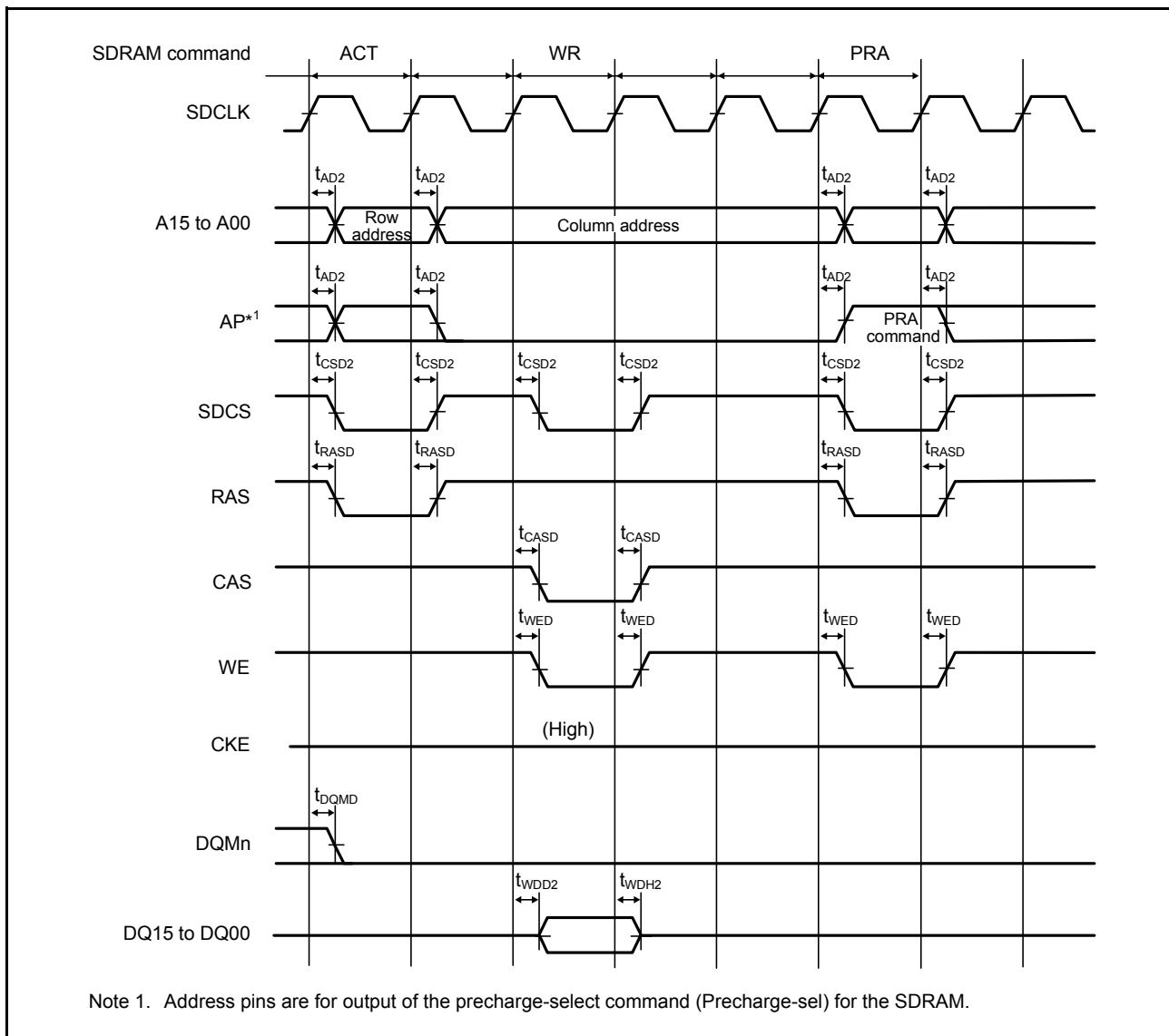


Figure 2.24 SDRAM single write timing

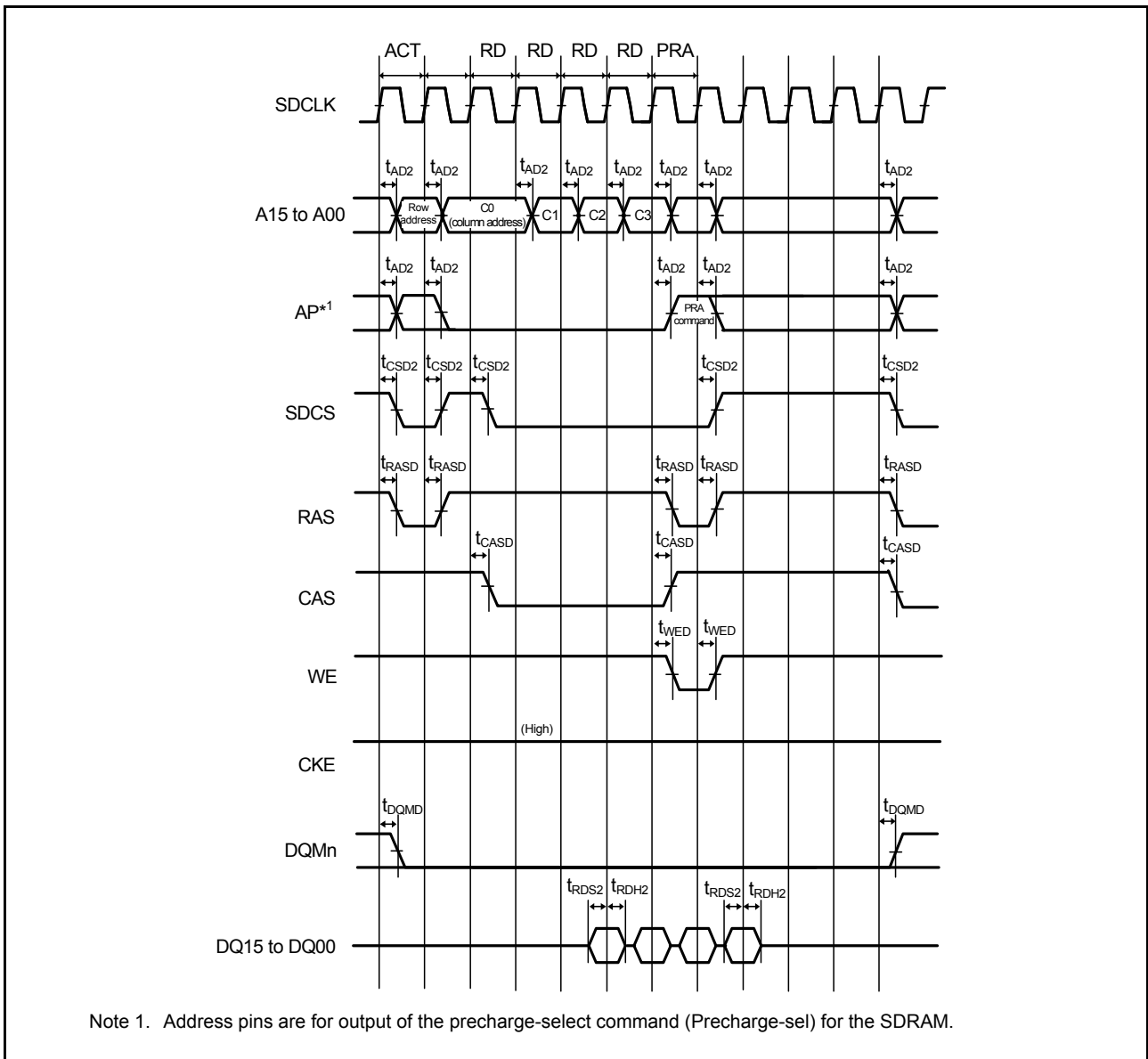


Figure 2.25 SDRAM multiple read timing

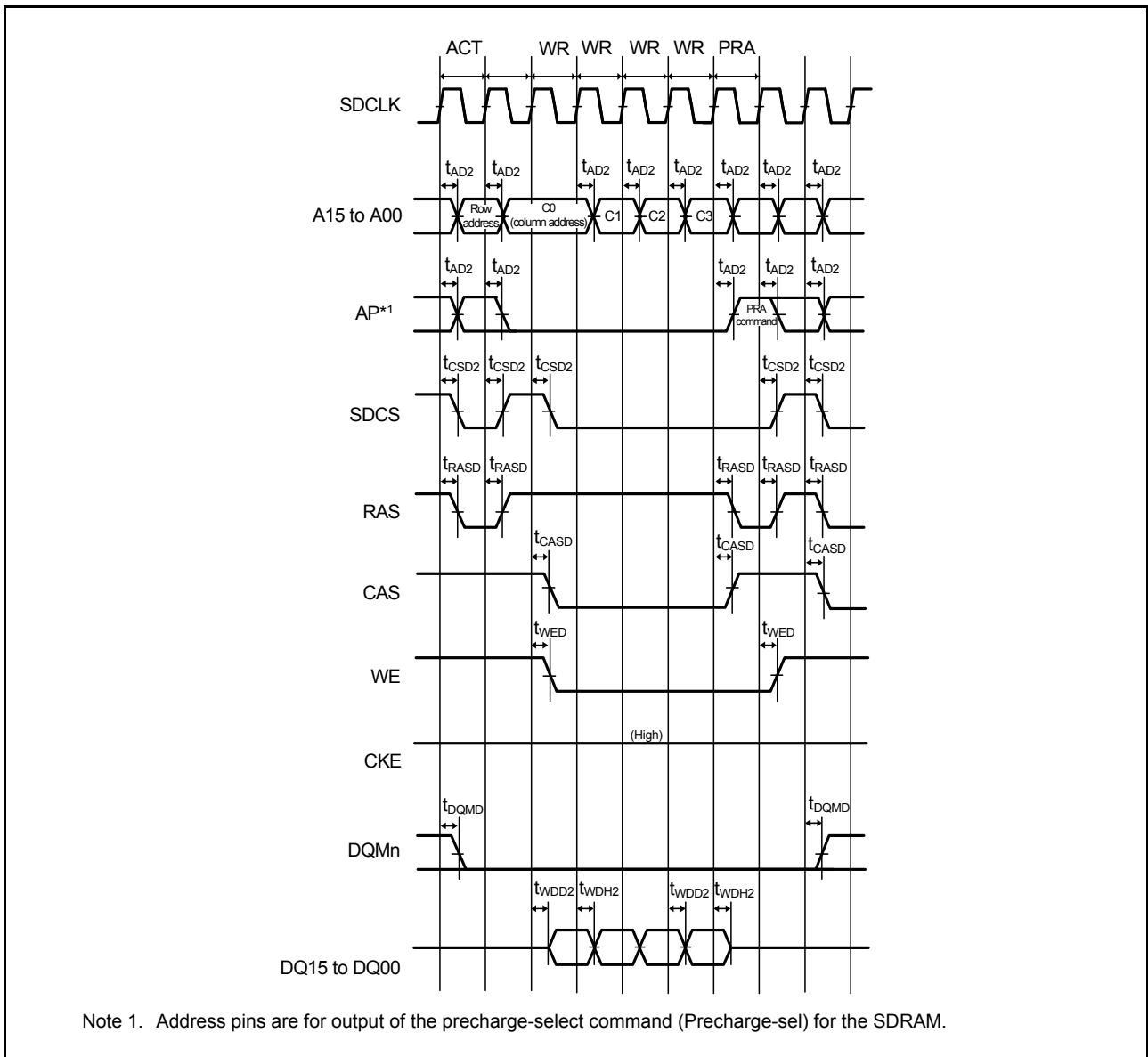


Figure 2.26 SDRAM multiple write timing

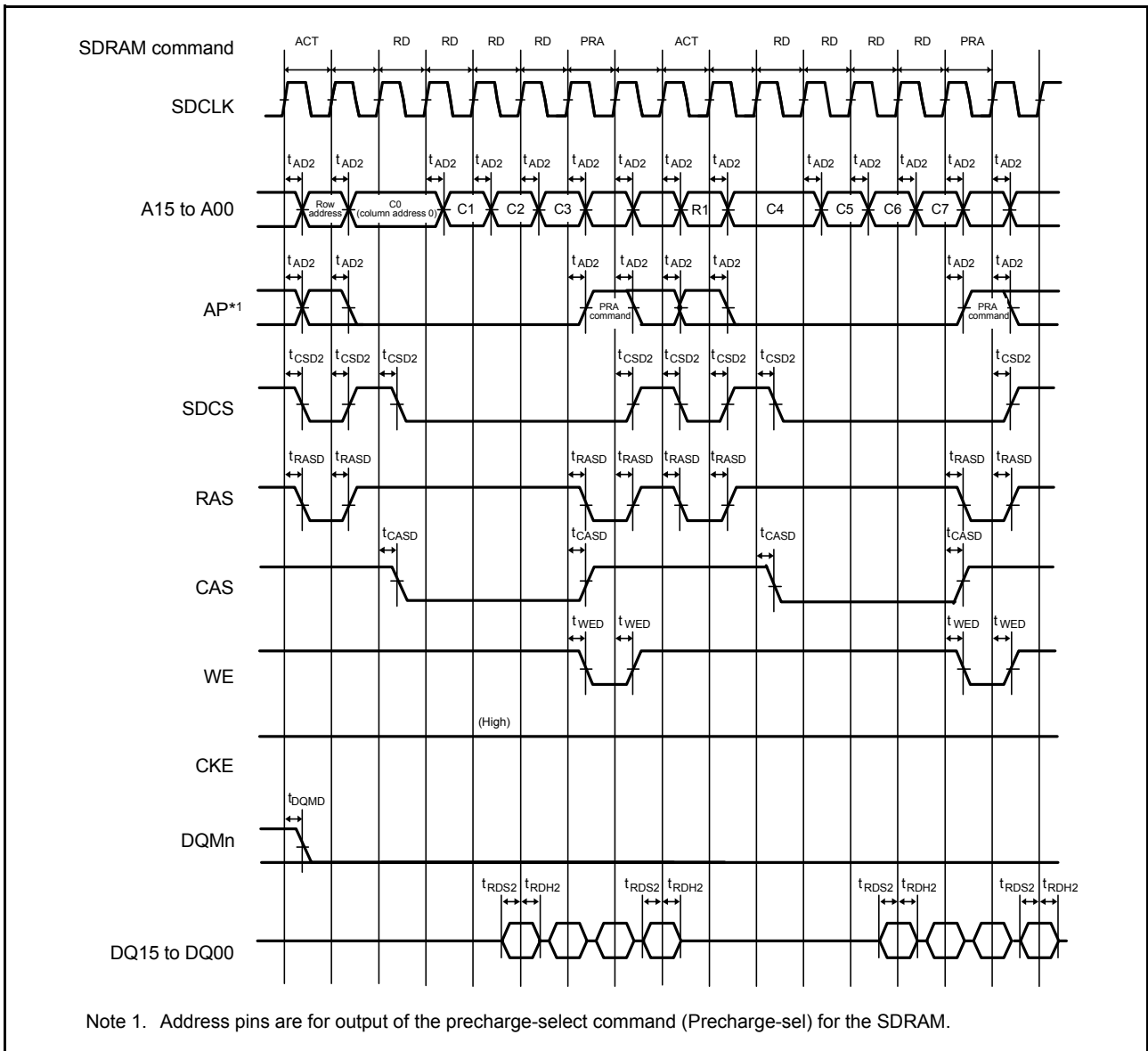


Figure 2.27 SDRAM multiple read line stride timing

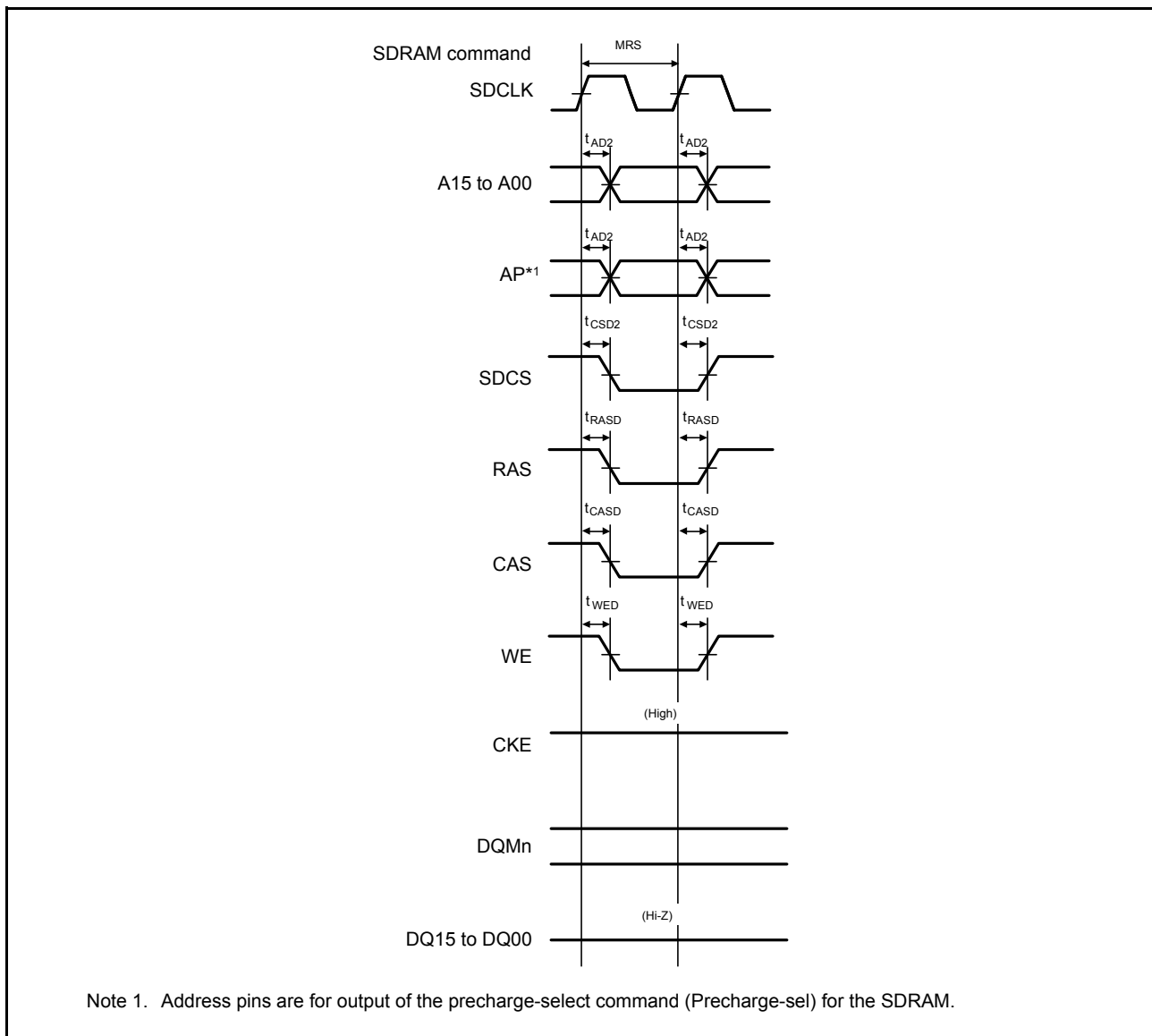


Figure 2.28 SDRAM mode register set timing

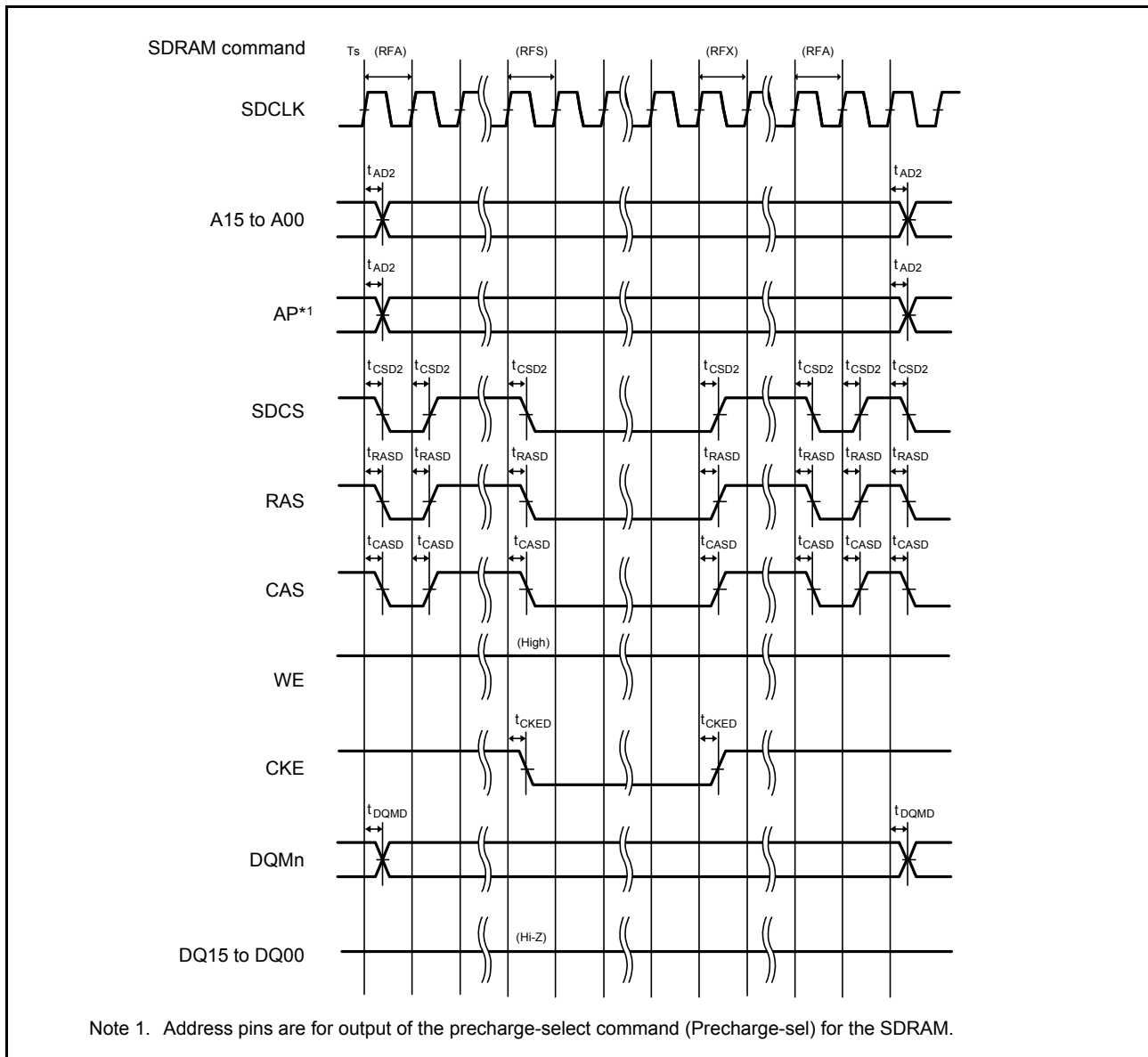


Figure 2.29 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)

GPT32 Conditions:

High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:

Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.30
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 2.31

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)

GPT32 Conditions:

High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:

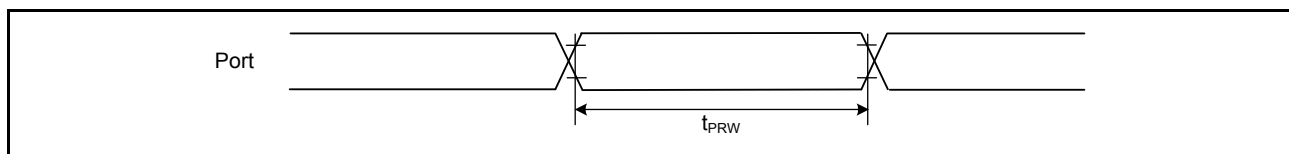
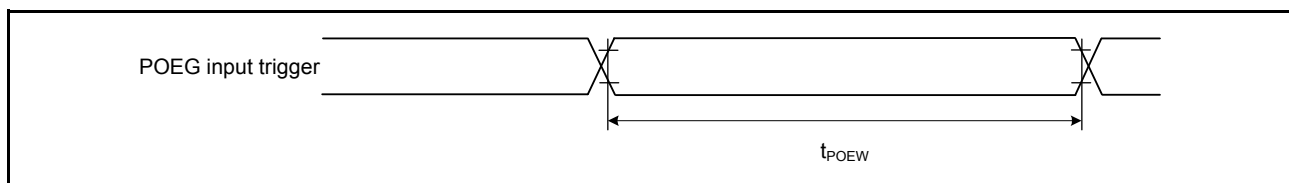
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions	
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.32
		Dual edge		2.5	-		
GPT32	GTIOCxY output skew (x = 0 to 7, Y = A or B)	Middle drive buffer	t_{GTISK}^{*2}	-	4	ns	Figure 2.33
		High drive buffer		-	4		
	GTIOCxY output skew (x = 8 to 13, Y = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 2.34	
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)	t_{HRSK}^{*3}	-	2.0	ns	Figure 2.35	
AGT	AGTIO, AGTEE input cycle	t_{ACYC}^{*4}	100	-	ns	Figure 2.36	
	AGTIO, AGTEE input high width, low width	t_{ACKWH} , t_{ACKWL}	40	-	ns		
	AGTIO, AGTO, AGTOA, AGTOB output cycle	t_{ACYC2}	62.5	-	ns		
ADC12	ADC12 trigger input pulse width	t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.37	
KINT	Key interrupt input low width	t_{KR}	250	-	ns	Figure 2.38	

Note 1. t_{Pcyc} : PCLKB cycle, t_{PDcyc} : PCLKD cycle.

Note 2. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.

Note 3. The load is 30 pF.

Note 4. Constraints on AGTIO input: $t_{Pcyc} \times 2$ (t_{Pcyc} : PCLKB cycle) < t_{ACYC} .**Figure 2.30 I/O ports input timing****Figure 2.31 POEG input trigger timing**

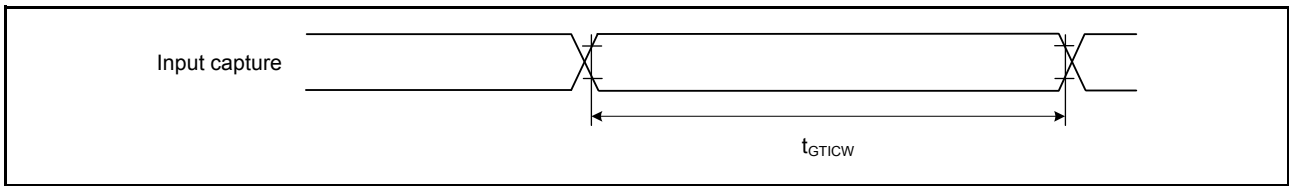


Figure 2.32 GPT32 input capture timing

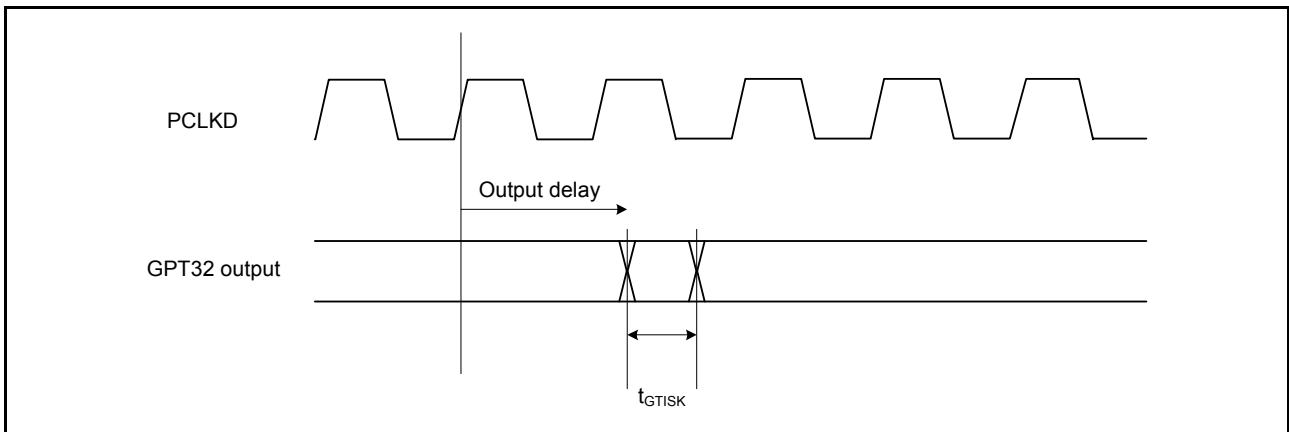


Figure 2.33 GPT32 output delay skew

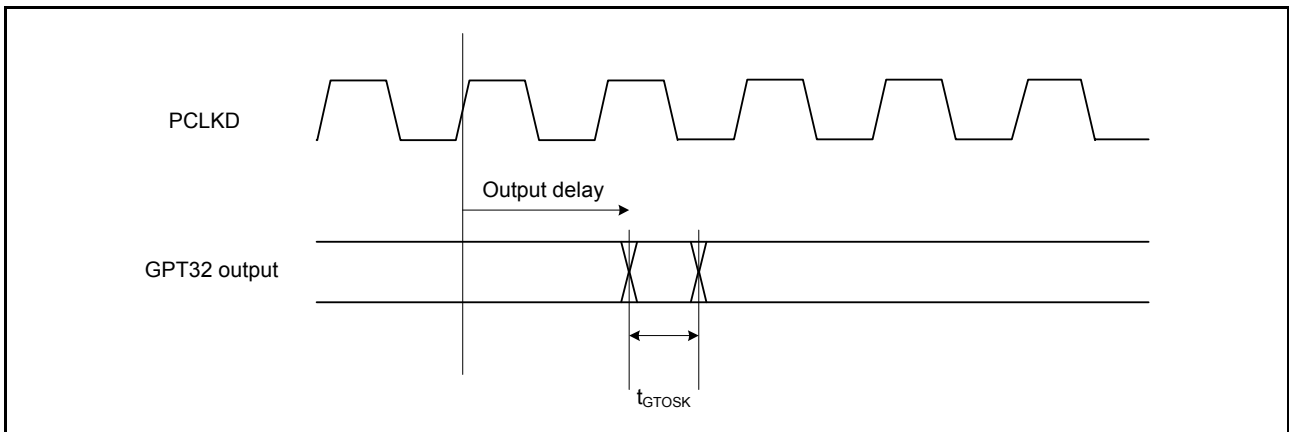


Figure 2.34 GPT32 output delay skew for OPS

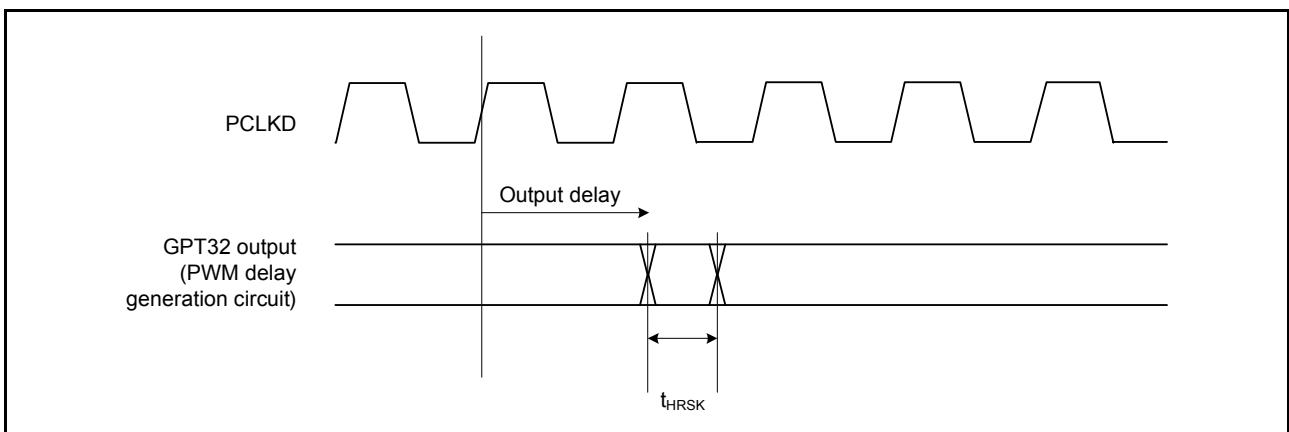


Figure 2.35 GPT32 (PWM Delay Generation Circuit) output delay skew

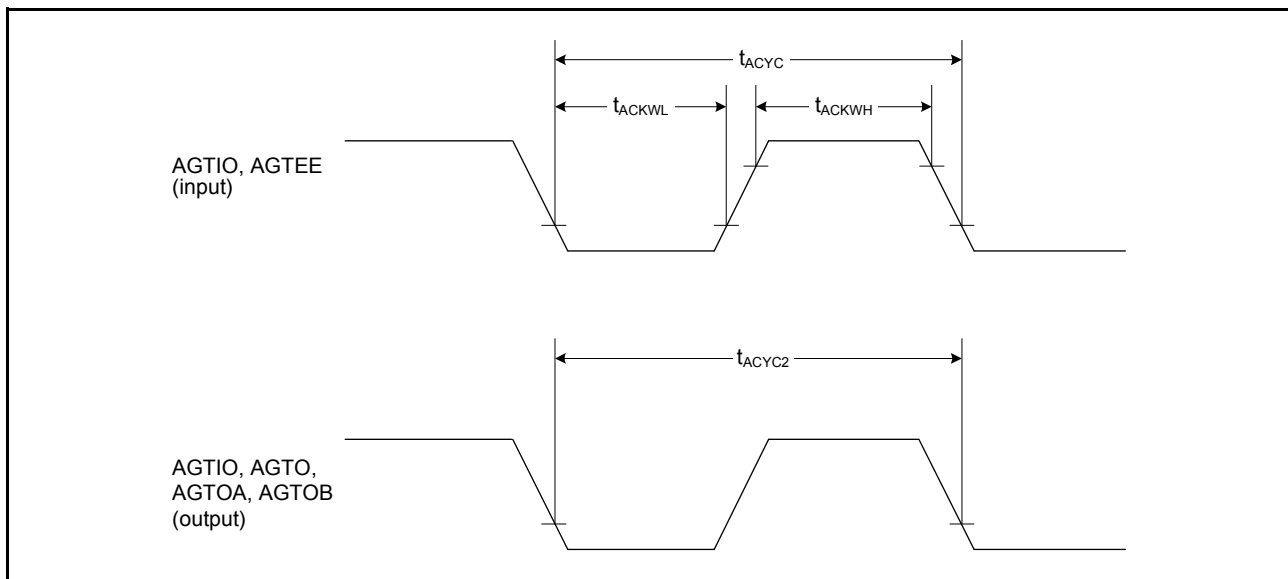


Figure 2.36 AGT input/output timing

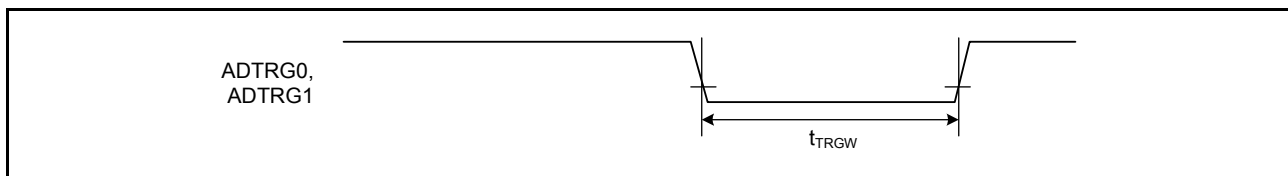


Figure 2.37 ADC12 trigger input timing

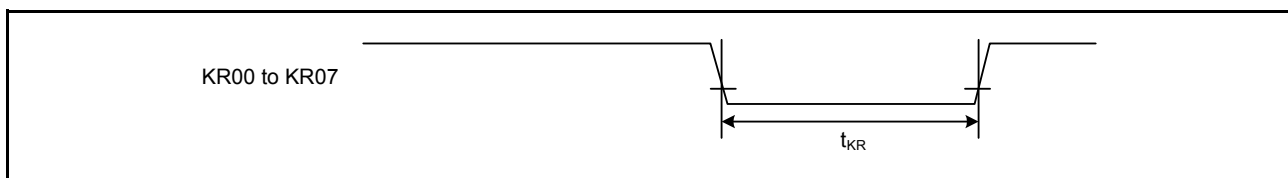


Figure 2.38 Key interrupt input timing

2.3.8 PWM Delay Generation Circuit Timing

Table 2.20 PWM Delay Generation Circuit timing

Item	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.9 CAC Timing

Table 2.21 CAC timing

Item	Symbol	Min	Typ	Max	Unit	Test conditions		
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac} * 2$	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > t_{cac} * 2$		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{pBcyc} : PCLKB cycle.

Note 2. t_{cac} : CAC count clock source cycle.

2.3.10 SCI Timing

Table 2.22 SCI timing (1)

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9. For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit*1	Test conditions		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.39	
		Clock synchronous		6	-			
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Input clock rise time		t_{SCKr}	-	5	ns		
	Input clock fall time		t_{SCKf}	-	5	ns		
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}		
		Clock synchronous		4	-			
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}		
	Output clock rise time		t_{SCKr}	-	5	ns		
	Output clock fall time		t_{SCKf}	-	5	ns		
	Transmit data delay	Clock synchronous	t_{TXD}	-	25	ns		Figure 2.40
	Receive data setup time	Clock synchronous	t_{RXS}	15	-	ns		
Receive data hold time	Clock synchronous	t_{RXH}	5	-	ns			

Note 1. t_{Pcyc} : PCLKA cycle.

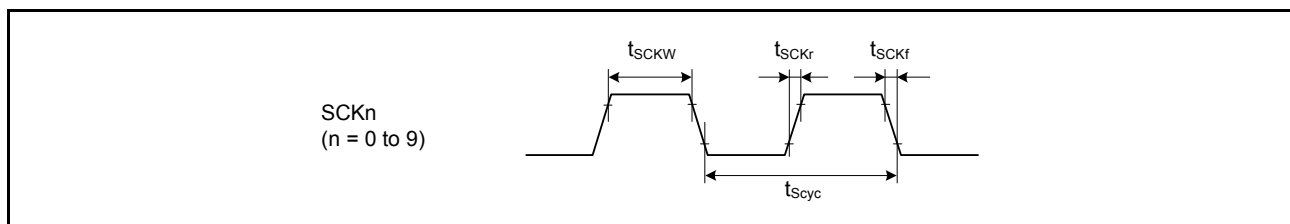


Figure 2.39 SCK clock input/output timing

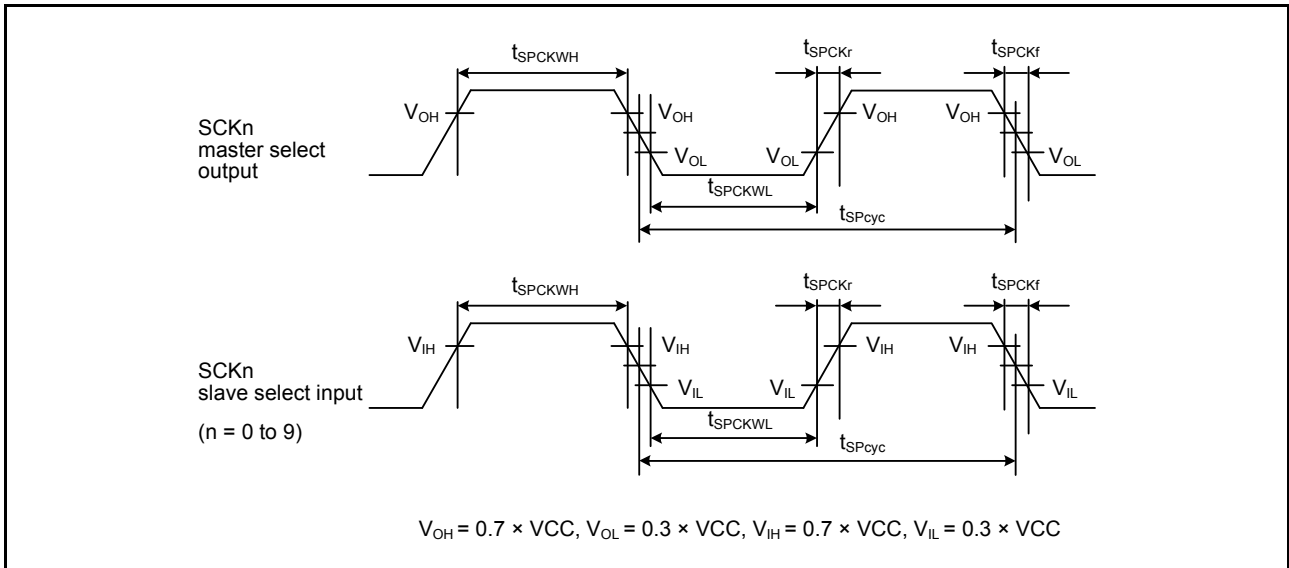


Figure 2.41 SCI simple SPI mode clock timing

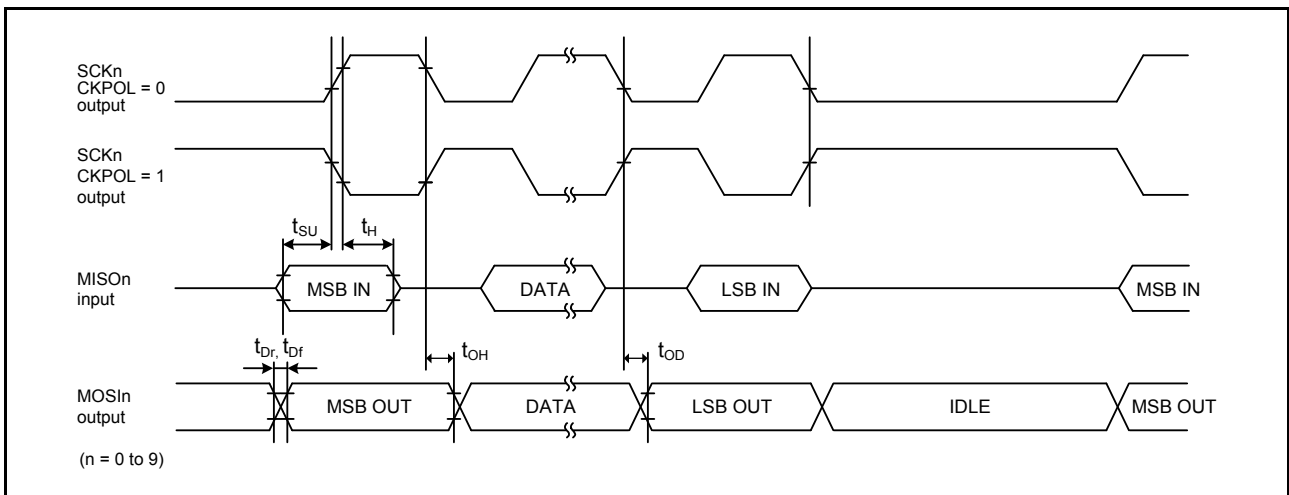


Figure 2.42 SCI simple SPI mode timing for master when CKPH = 1

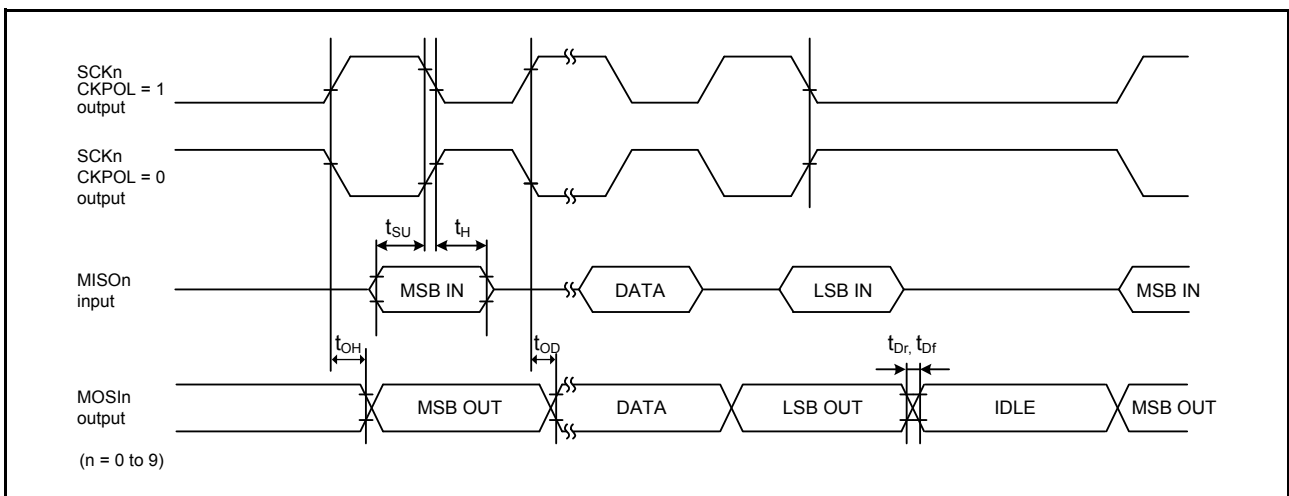


Figure 2.43 SCI simple SPI mode timing for master when CKPH = 0

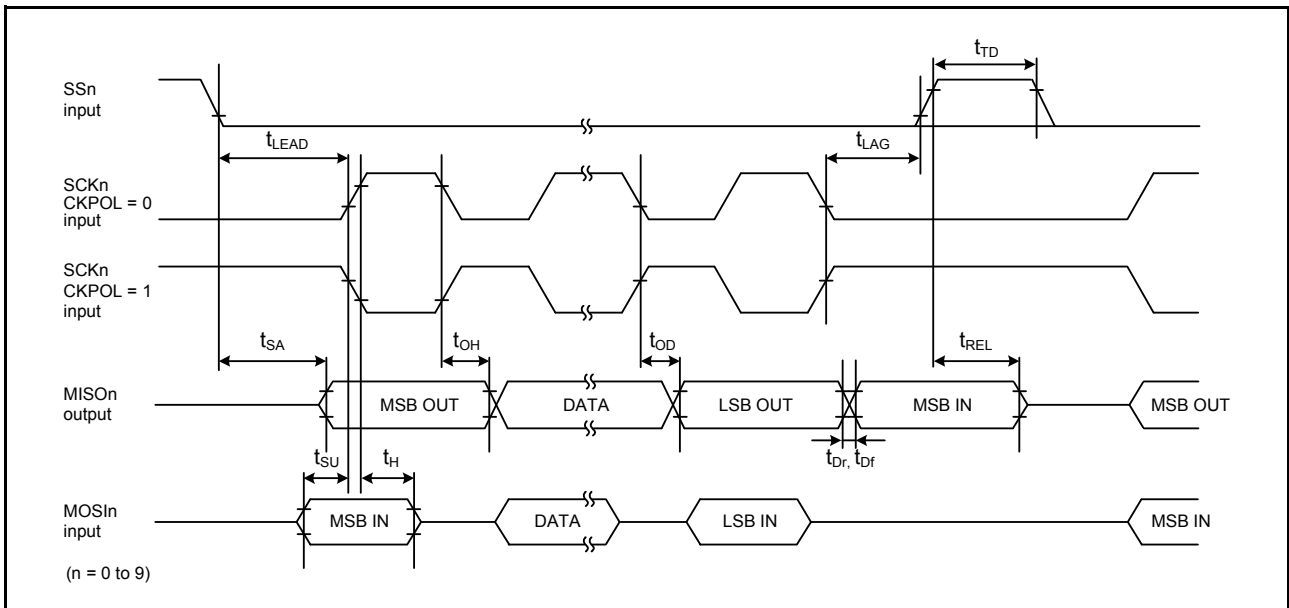


Figure 2.44 SCI simple SPI mode timing for slave when CKPH = 1

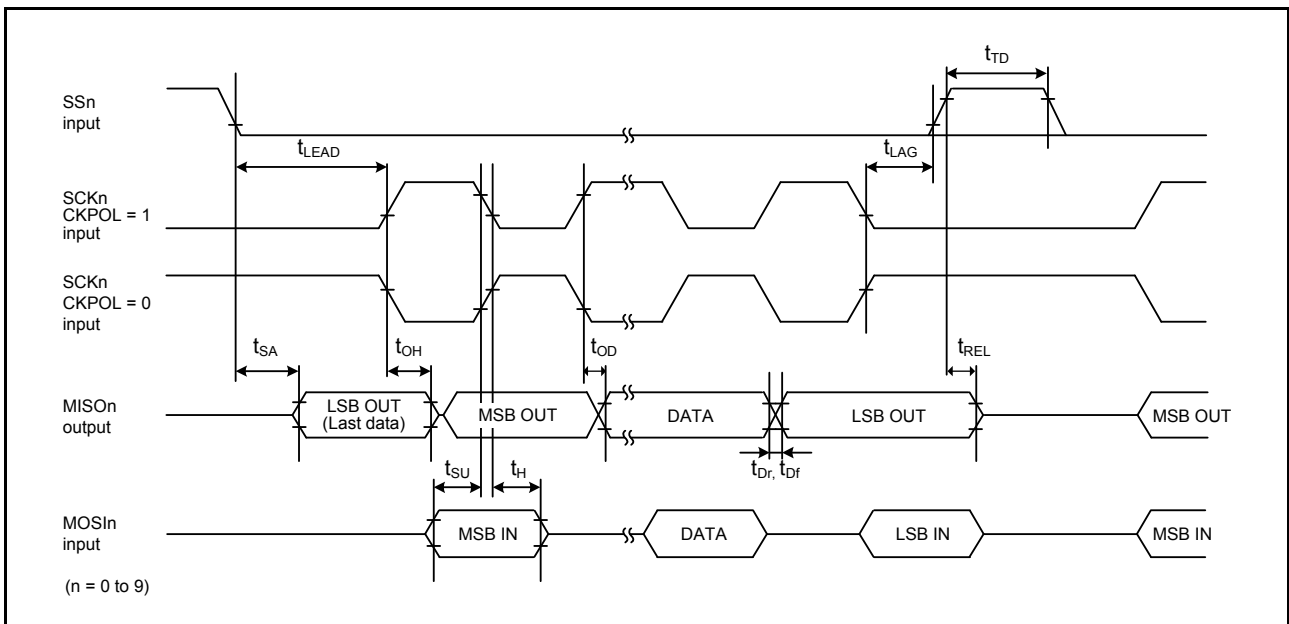


Figure 2.45 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1 of 2)

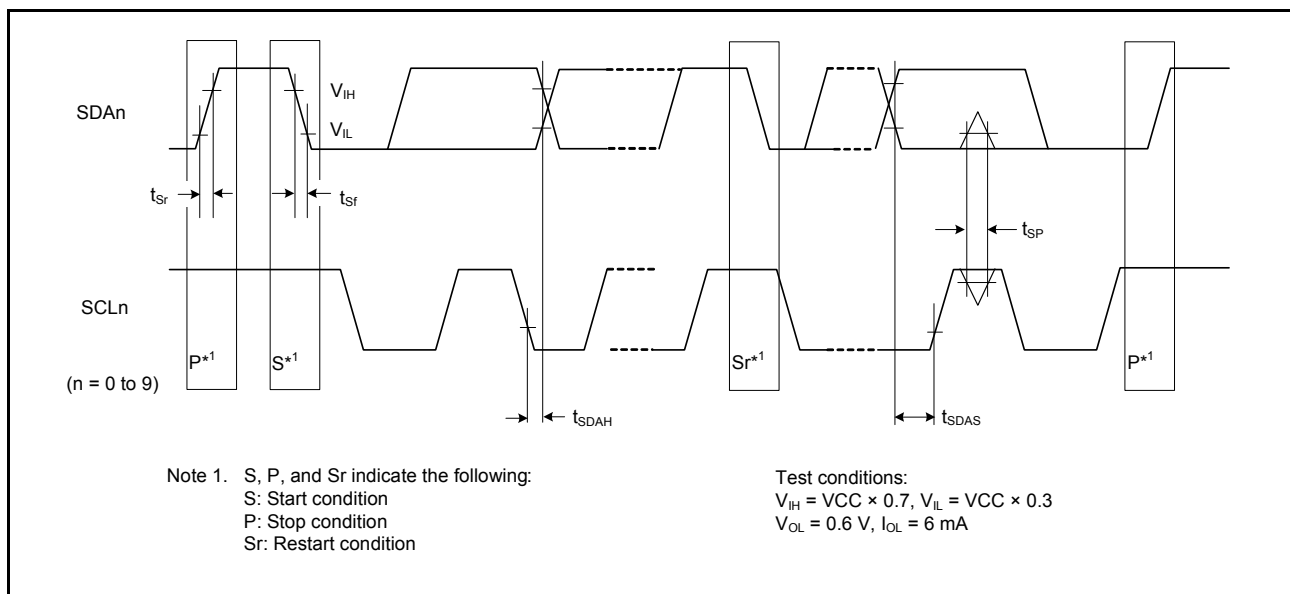
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.46
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IIcyc}$	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b^{*1}	-	400	pF	

Table 2.24 SCI timing (3) (2 of 2)

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.46
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b^{*1}	-	400	pF	

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKA cycle.Note 1. C_b indicates the total capacity of the bus line.**Figure 2.46 SCI simple IIC mode timing**

2.3.11 SPI Timing

Table 2.25 SPI timing

Conditions:

For RSPCKA and RSPCKB pins, high drive output is selected with the port drive capability bit in the PmnPFS register.

For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit*1	Test conditions*2	
SPI	RSPCK clock cycle	Master	t_{SPCyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{PCyc} Figure 2.47 C = 30 pF
		Slave		4	4096	
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns
		Slave		$2 \times t_{PCyc}$	-	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns
		Slave		$2 \times t_{PCyc}$	-	
	RSPCK clock rise and fall time	Master	t_{SPCKr}	-	5	ns
		Slave	t_{SPCKf}	-	1	
	Data input setup time	Master	t_{SU}	4	-	ns
		Slave		5	-	
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	-	ns
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{PCyc}	-	
		Slave	t_H	20	-	
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPCyc} - 10^{*3}$	$N \times t_{SPCyc} + 100^{*3}$	ns
		Slave		$6 \times t_{PCyc}$	-	
	SSL hold time	Master	t_{LAG}	$N \times t_{SPCyc} - 10^{*4}$	$N \times t_{SPCyc} + 100^{*4}$	ns
		Slave		$6 \times t_{PCyc}$	-	
	Data output delay	Master	t_{OD}	-	6.3	ns
		Slave		-	20	
	Data output hold time	Master	t_{OH}	0	-	ns
		Slave		0	-	
	Successive transmission delay	Master	t_{TD}	$t_{SPCyc} + 2 \times t_{PCyc}$	$8 \times t_{SPCyc} + 2 \times t_{PCyc}$	ns
		Slave		$6 \times t_{PCyc}$		
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns
		Input		-	1	
	SSL rise and fall time	Output	t_{SSLr}	-	5	ns
		Input	t_{SSLf}	-	1	
	Slave access time	t_{SA}	-	$2 \times t_{PCyc} + 28$	ns	Figure 2.52 and Figure 2.53 C = 30 pF
	Slave output release time	t_{REL}	-	$2 \times t_{PCyc} + 28$		

Note 1. t_{PCyc} : PCLKA cycle.

- Note 2. Must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
- Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
- Note 4. N is set to an integer from 1 to 8 by the SSLND register.

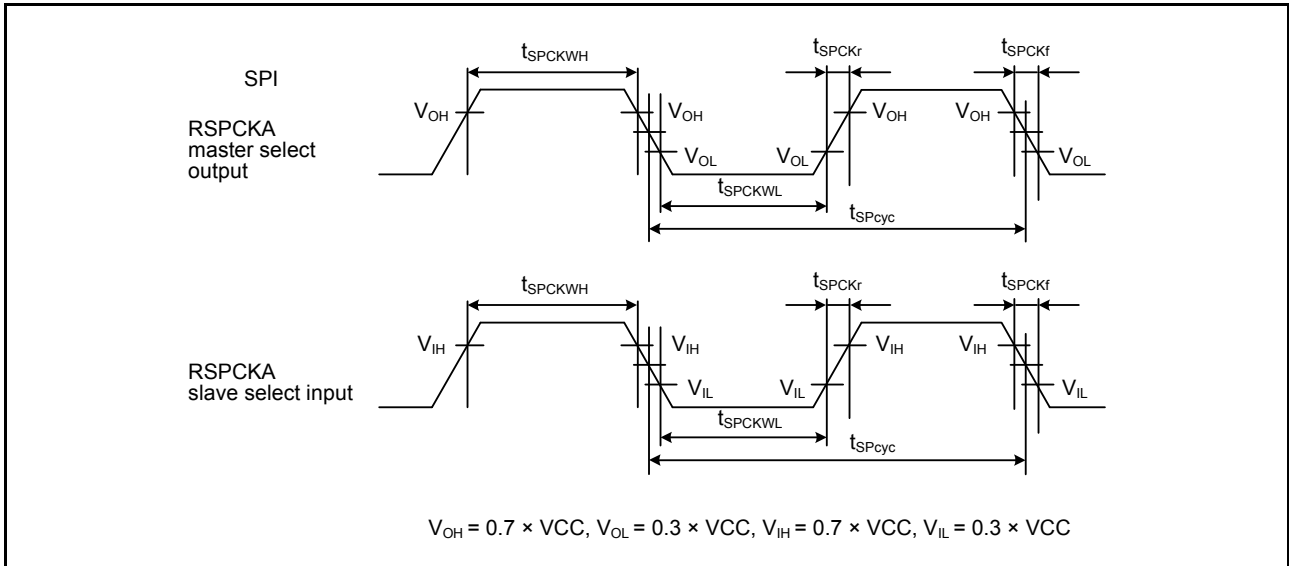


Figure 2.47 SPI clock timing

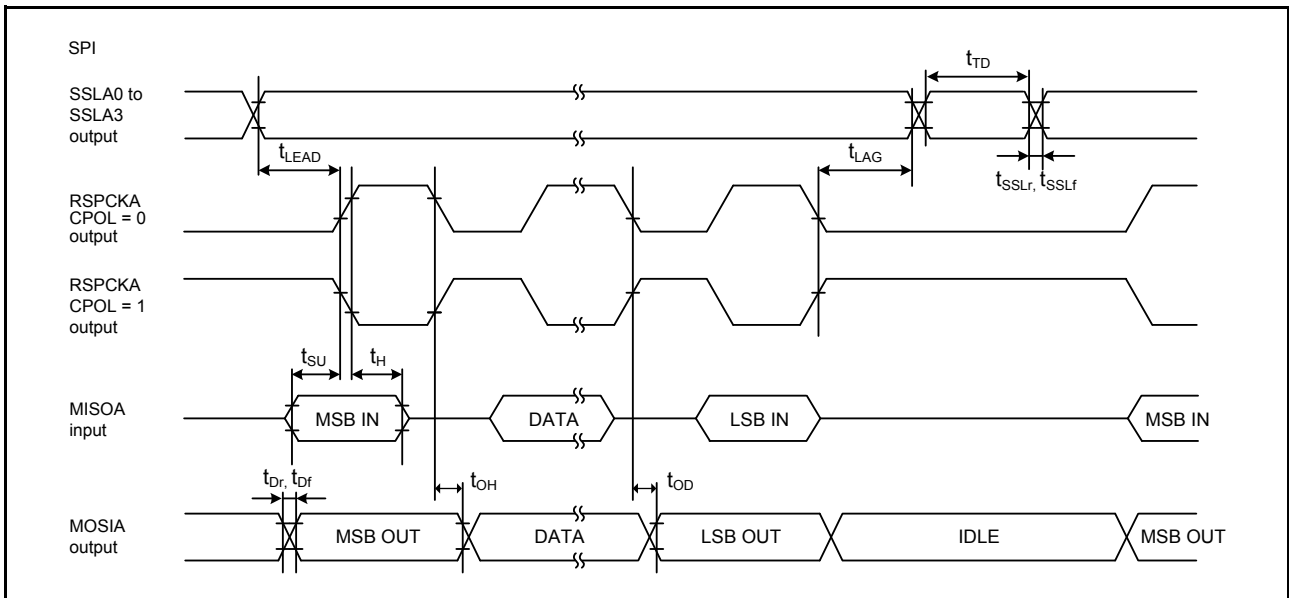


Figure 2.48 SPI timing for master when CPHA = 0

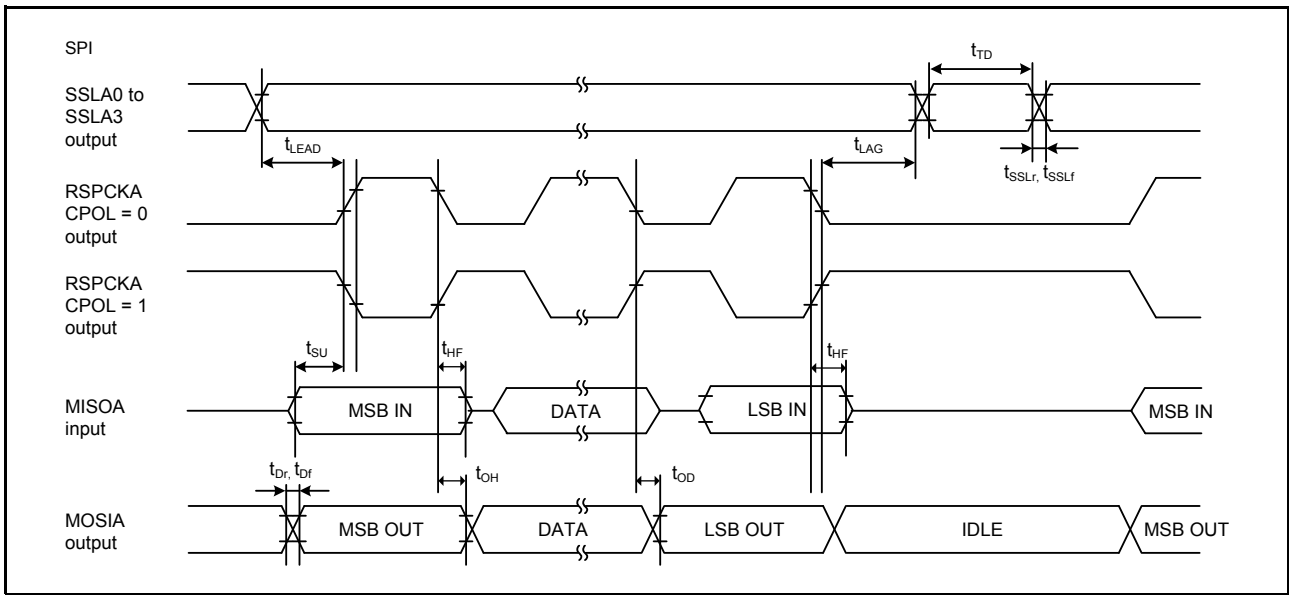


Figure 2.49 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

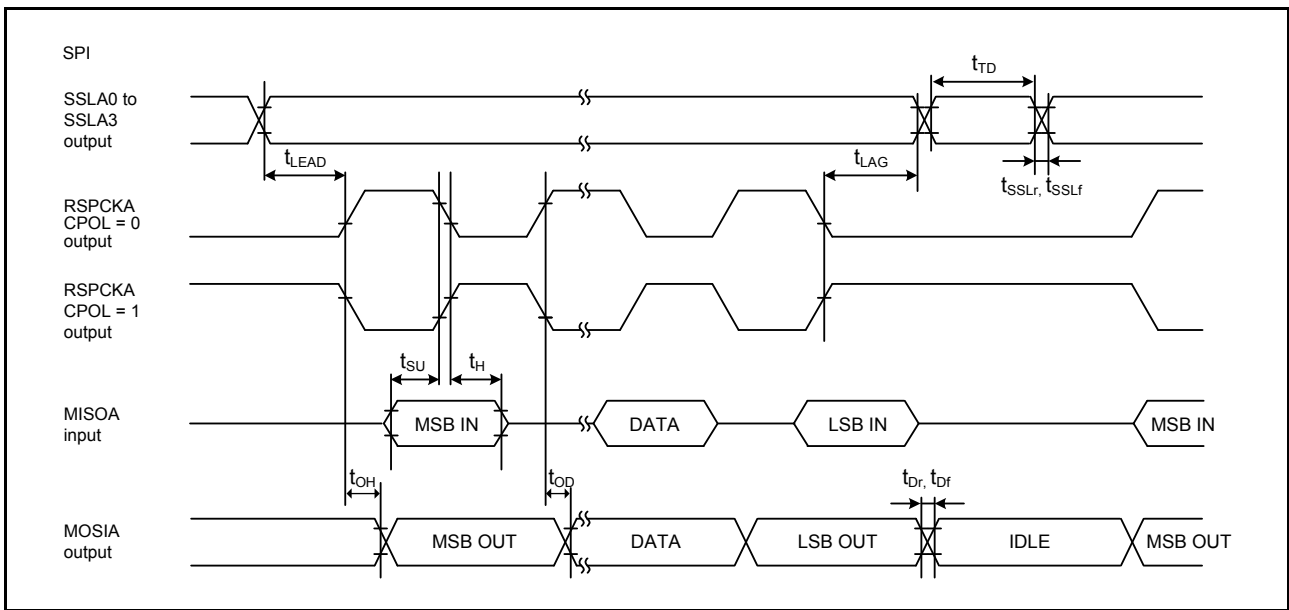


Figure 2.50 SPI timing for master when CPHA = 1

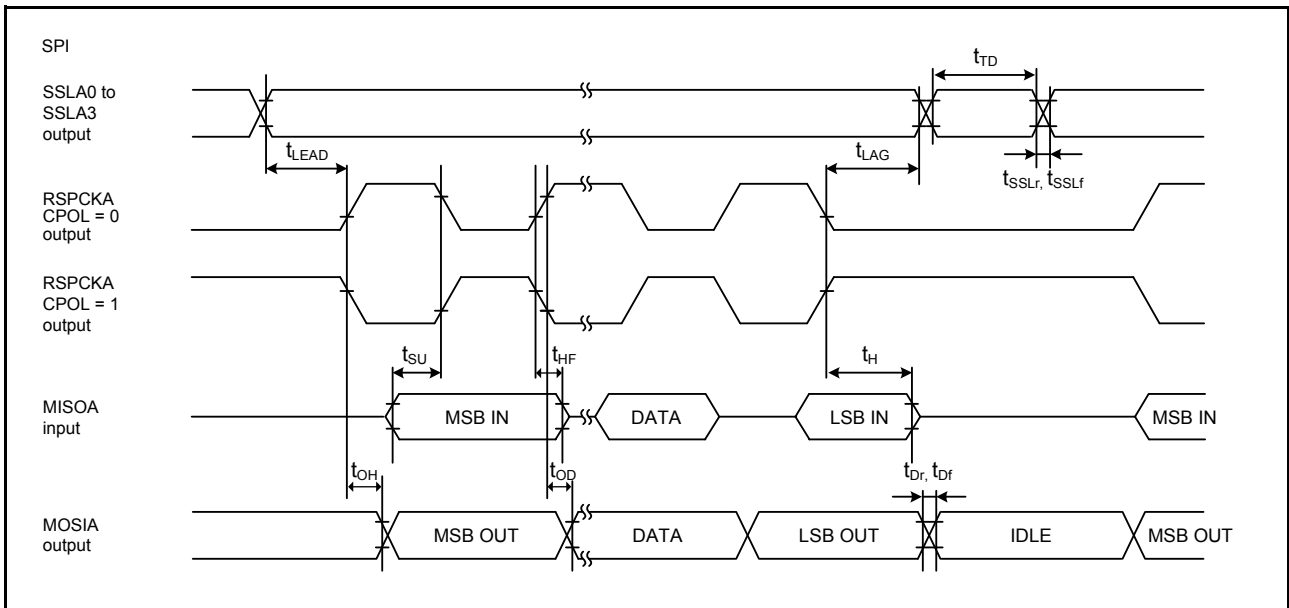


Figure 2.51 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

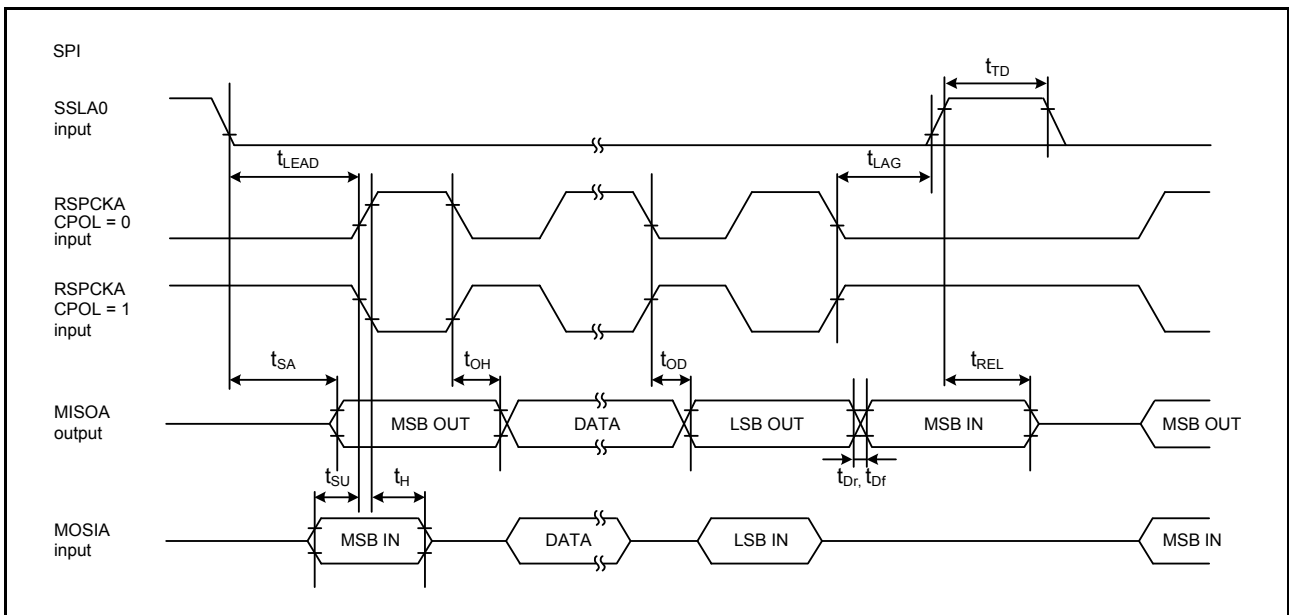


Figure 2.52 SPI timing for slave when CPHA = 0

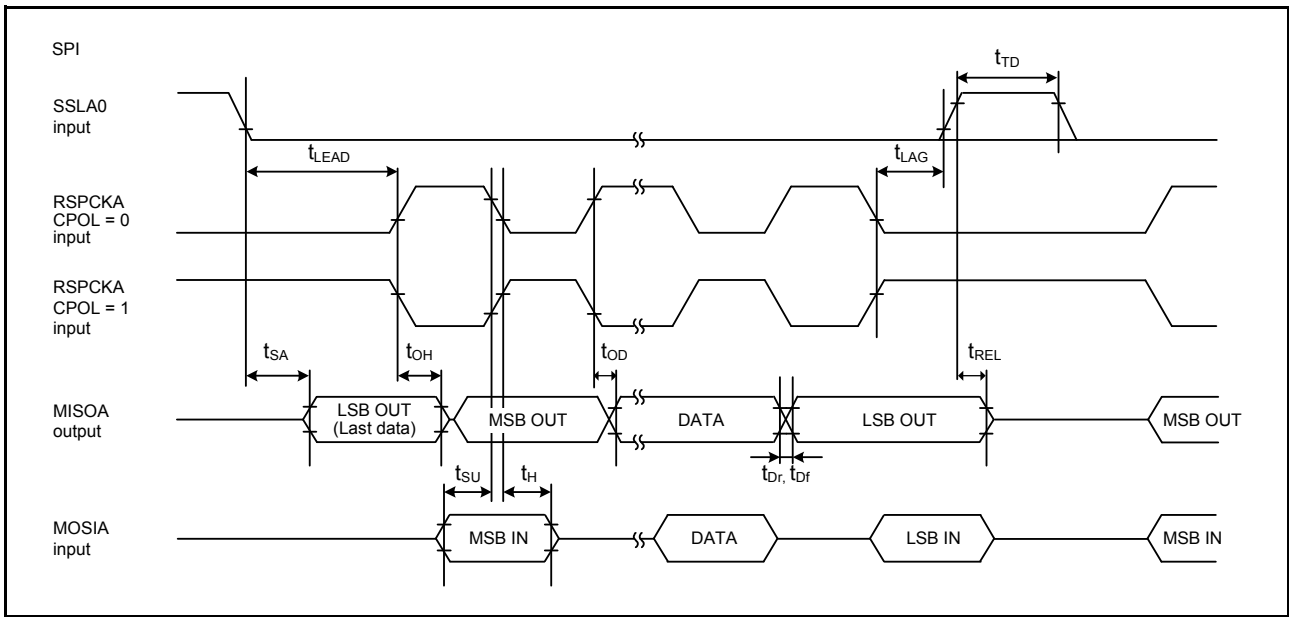


Figure 2.53 SPI timing for slave when CPHA = 1

2.3.12 QSPI Timing

Table 2.26 QSPI timing

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit*1	Test conditions	
QSPI	QSPCK clock cycle	t_{QScyc}	48	t_{Pcyc}	Figure 2.54	
	QSPCK clock high pulse width	t_{QSWH}	$t_{QScyc} \times 0.4$	ns		
	QSPCK clock low pulse width	t_{QSWL}	$t_{QScyc} \times 0.4$	ns		
QSPI	Data input setup time	t_{Su}	8	ns	Figure 2.55	
	Data input hold time	t_{IH}	0	ns		
	QSSL setup time	t_{LEAD}	$(N+0.5) \times t_{QScyc} - 5 *2$	$(N+0.5) \times t_{QScyc} + 100 *2$		ns
	QSSL hold time	t_{LAG}	$(N+0.5) \times t_{QScyc} - 5 *3$	$(N+0.5) \times t_{QScyc} + 100 *3$		ns
	Data output delay	t_{OD}	-	4		ns
	Data output hold time	t_{OH}	-3.3	-		ns
	Successive transmission delay	t_{TD}	1	16		t_{QScyc}

Note 1. t_{Pcyc} : PCLKA cycle.

Note 2. N is set to 0 or 1 in SFMSLD.

Note 3. N is set to 0 or 1 in SFMSHD.

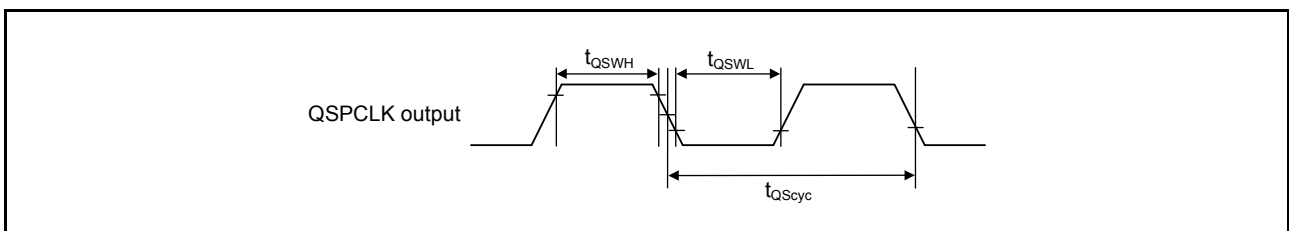


Figure 2.54 QSPI clock timing

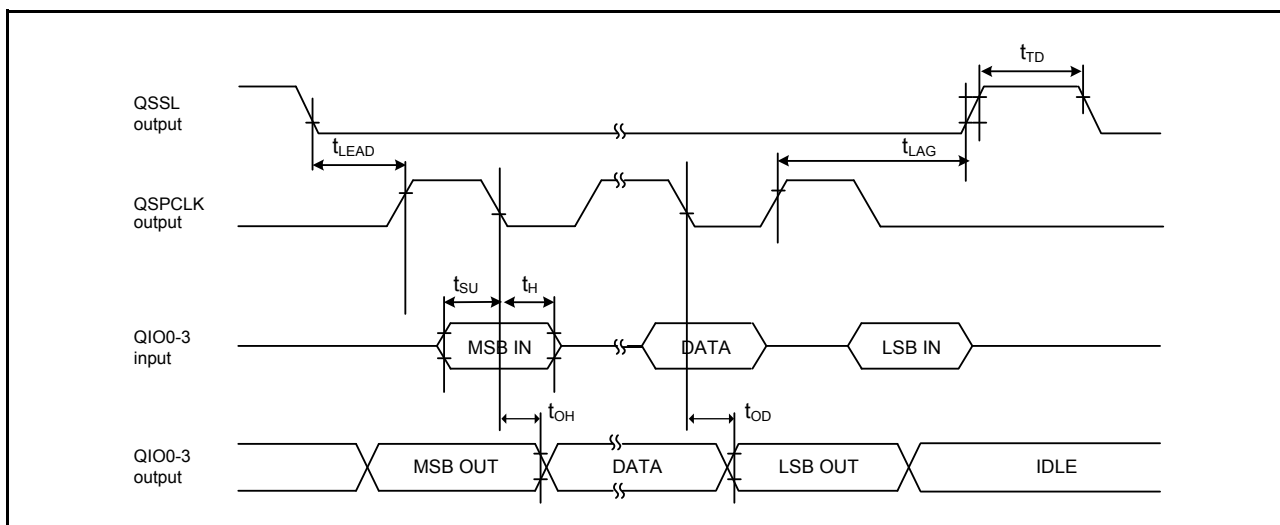


Figure 2.55 Transmit and receive timing

2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1 of 2)

- (1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
- (2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.
- (3) Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Item	Symbol	Min*1	Max	Unit	Test conditions*3	
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 1300$	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Table 2.27 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.

(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

(3) Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Item	Symbol	Min*1	Max	Unit	Test conditions*3	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 600$	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	t_{Sr}	$20 \times (\text{external pullup voltage}/5.5V)^2$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 \times (\text{external pullup voltage}/5.5V)^2$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
SCL, SDA capacitive load	C_b	-	400	pF		

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.

Note 3. Must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

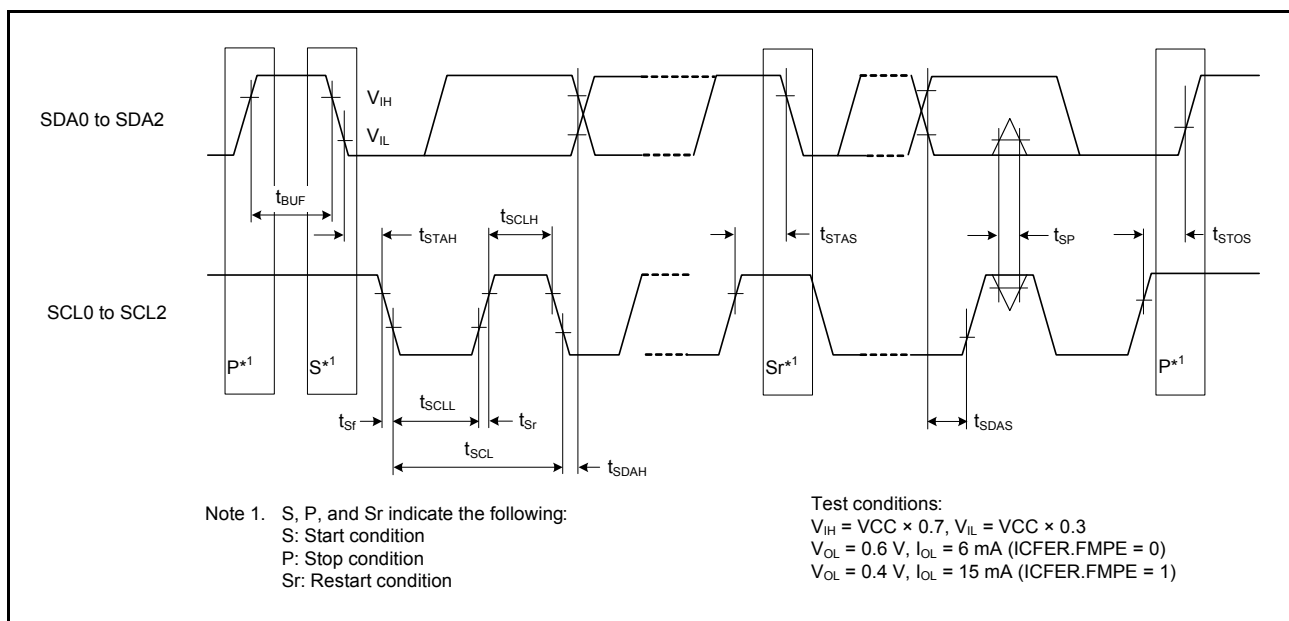
Table 2.28 IIC timing (2)

Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.

Item	Symbol	Min ^{*1,*2}	Max	Unit	Test conditions	
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 240$	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 120$	-	ns	
	SCL input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 120$	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	$3 (6) \times t_{IICcyc} + 120$	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 120$	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	$t_{IICcyc} + 120$	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 120$	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 30$	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle.

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Note 2. C_b indicates the total capacity of the bus line.**Figure 2.56 IIC bus interface input/output timing**

2.3.14 SSIE Timing

Table 2.29 SSIE timing

(1) High drive output is selected with the port drive capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance “_A” or “_B” to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Item		Symbol	Target specification		Unit	Comments	
			Min.	Max.			
SSIBCK	Cycle	Master	t_O	80	-	ns	Figure 2.57
		Slave	t_I	80	-	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	Rising time/falling time	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK/SSIFS, SSITXD0, SSIRXD0, SSIDATA1	Input set up time	Master	t_{SR}	12	-	ns	Figure 2.59, Figure 2.60
		Slave		12	-	ns	
	Input hold time	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	Figure 2.59, Figure 2.60
		Slave		0	20	ns	
	Output delay time from SSILRCK/SSIFS change	Slave	t_{DTRW}	-	20	ns	Figure 2.61*1
GTIOC1A, AUDIO_CLK	Cycle	t_{EXcyc}	20	-	ns	Figure 2.58	
	High level/ low level	$t_{EXL}/$ t_{EXH}	0.4	0.6	t_{EXcyc}		

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK/SSIFS pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA1 pin.

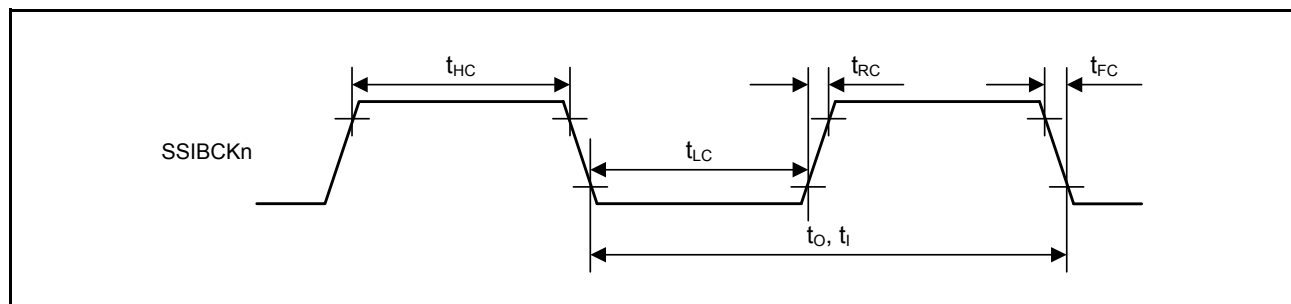


Figure 2.57 SSIE clock input/output timing

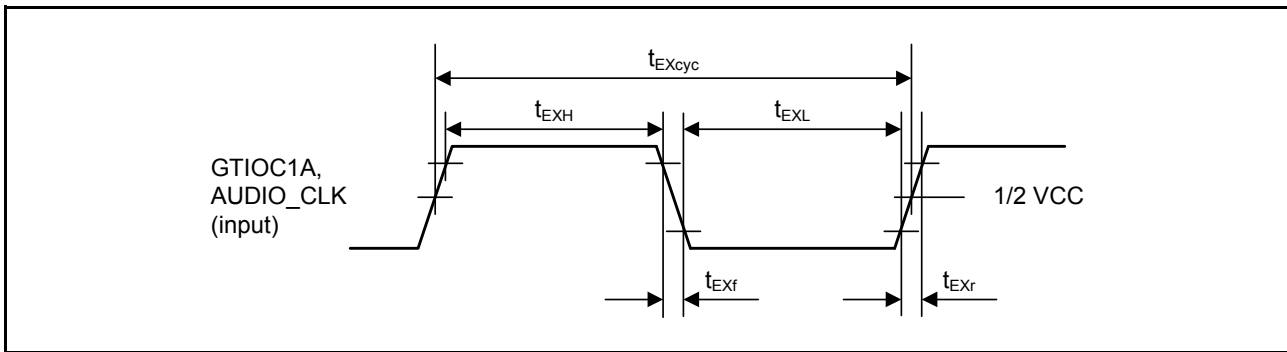


Figure 2.58 Clock input timing

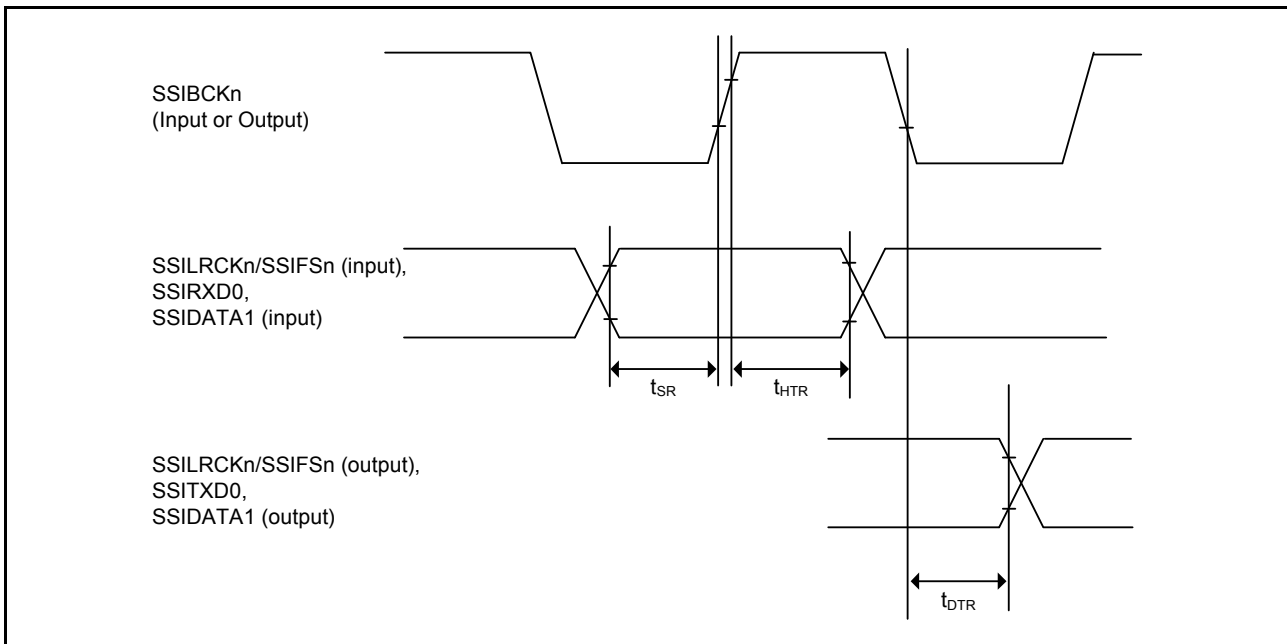


Figure 2.59 SSIE data transmit and receive timing when SSICR.BCKP = 0

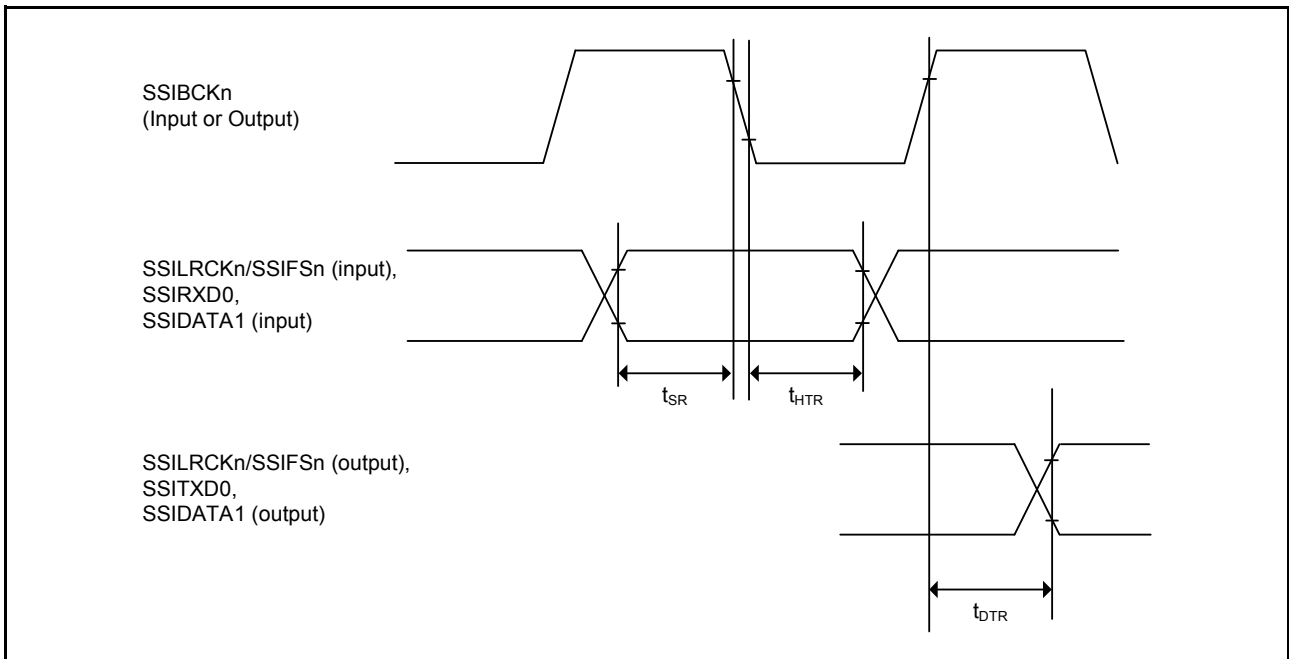


Figure 2.60 SSIE data transmit and receive timing when SSICR.BCKP = 1

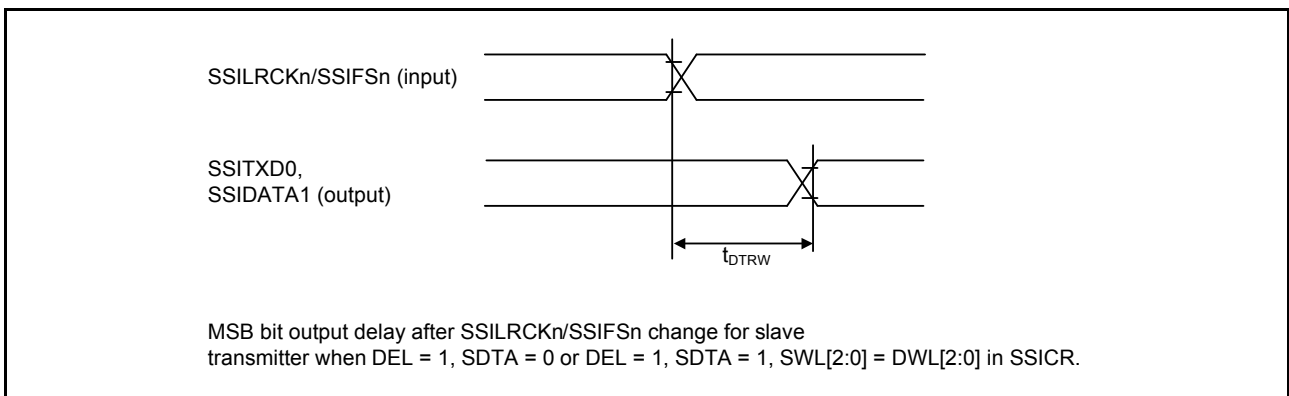


Figure 2.61 SSIE data output delay after SSILRCKn/SSIFSn change

2.3.15 SD/MMC Host Interface Timing

Table 2.30 SD/MMC Host Interface signal timing

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.
Clock duty ratio is 50%.

Item	Symbol	Min	Max	Unit	Test conditions*1
SDCLK clock cycle	T_{SDCYC}	20	-	ns	Figure 2.62
SDCLK clock high pulse width	T_{SDWH}	6.5	-	ns	
SDCLK clock low pulse width	T_{SDWL}	6.5	-	ns	
SDCLK clock rise time	T_{SDLH}	-	3	ns	
SDCLK clock fall time	T_{SDHL}	-	3	ns	
SDCMD/SDDAT output data delay	T_{SDODLY}	-6	5	ns	
SDCMD/SDDAT input data setup	T_{SDIS}	4	-	ns	
SDCMD/SDDAT input data hold	T_{SDIH}	2	-	ns	

Note 1. Must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For

the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

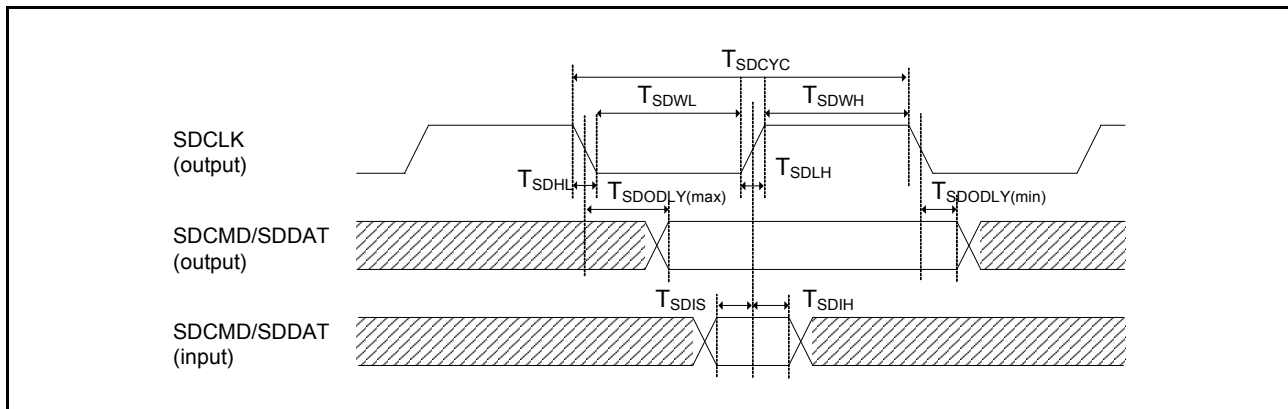


Figure 2.62 SD/MMC Host Interface signal timing

2.3.16 ETHERC Timing

Table 2.31 ETHERC timing

Conditions: ETHERC (RMII): Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO.

For other pins, high drive output is selected in the port drive capability bit in the PmnPFS register.

ETHERC (MII): Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit	Test conditions*3	
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	-	ns	Figure 2.63 to Figure 2.66
	REF50CK frequency, typical 50 MHz	-	-	50 + 100 ppm	MHz	
	REF50CK duty	-	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_XXXX*1 output delay	T_{co}	2.5	12.0	ns	
	RMII_XXXX*2 setup time	T_{su}	3	-	ns	
	RMII_XXXX*2 hold time	T_{hd}	1	-	ns	
	RMII_XXXX*1, *2 rise/fall time	T_r/T_f	0.5	4	ns	
	ET_WOL output delay	t_{WOLd}	1	23.5	ns	
ETHERC (MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	-	ns	-
	ET_TX_EN output delay	t_{TENd}	1	20	ns	Figure 2.68
	ET_ETXD0 to ET_ETXD3 output delay	t_{MTDd}	1	20	ns	Figure 2.69
	ET_CRs setup time	t_{CRSs}	10	-	ns	
	ET_CRs hold time	t_{CRSh}	10	-	ns	
	ET_COL setup time	t_{COLs}	10	-	ns	Figure 2.69
	ET_COL hold time	t_{COLh}	10	-	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	-	ns	
	ET_RX_DV setup time	t_{RDVs}	10	-	ns	Figure 2.70
	ET_RX_DV hold time	t_{RDVh}	10	-	ns	Figure 2.70
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	-	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	-	ns	
	ET_RX_ER setup time	t_{RERs}	10	-	ns	Figure 2.71
	ET_RX_ER hold time	t_{RESh}	10	-	ns	Figure 2.71
	ET_WOL output delay	t_{WOLd}	1	23.5	ns	

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.

Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER.

Note 3. The following pins, must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group. REF50CK0_A, REF50CF0_B, RMII0_xxxx_A, RMII0_xxxx_B

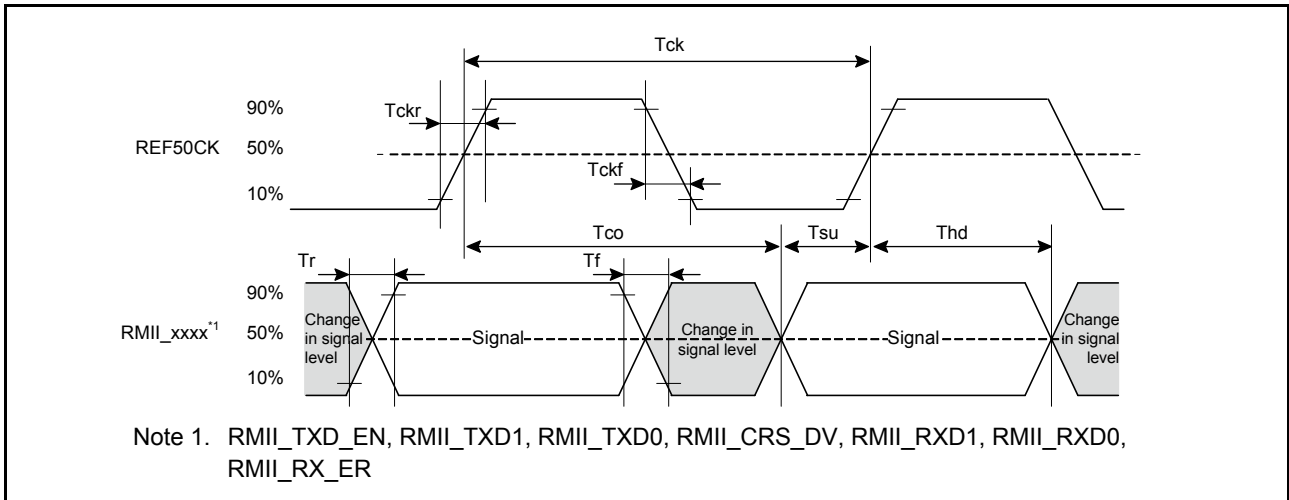


Figure 2.63 REF50CK and RMII signal timing

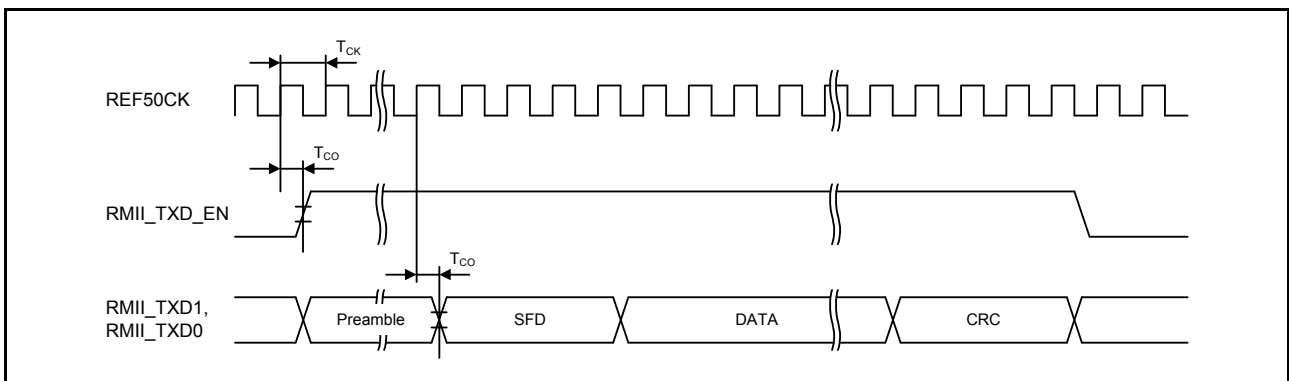


Figure 2.64 RMII transmission timing

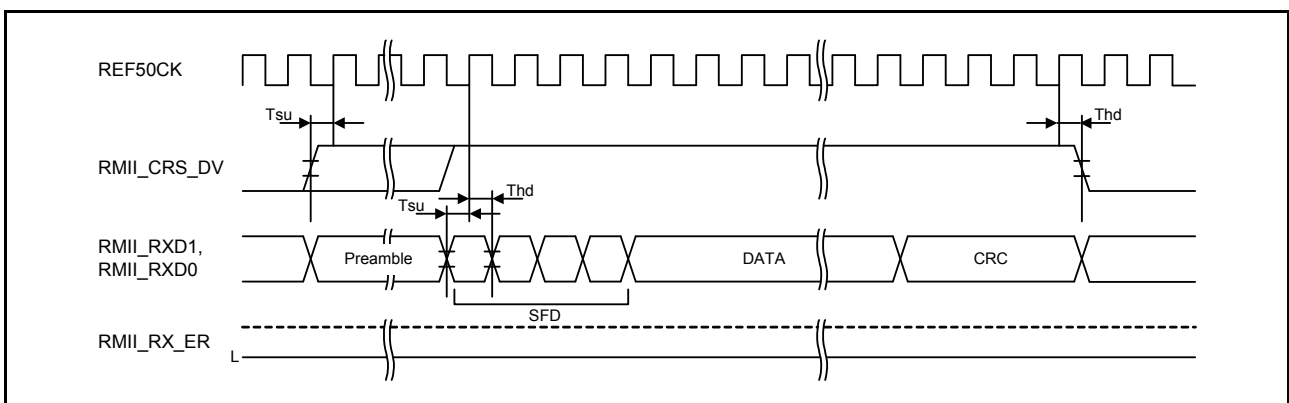


Figure 2.65 RMII reception timing in normal operation

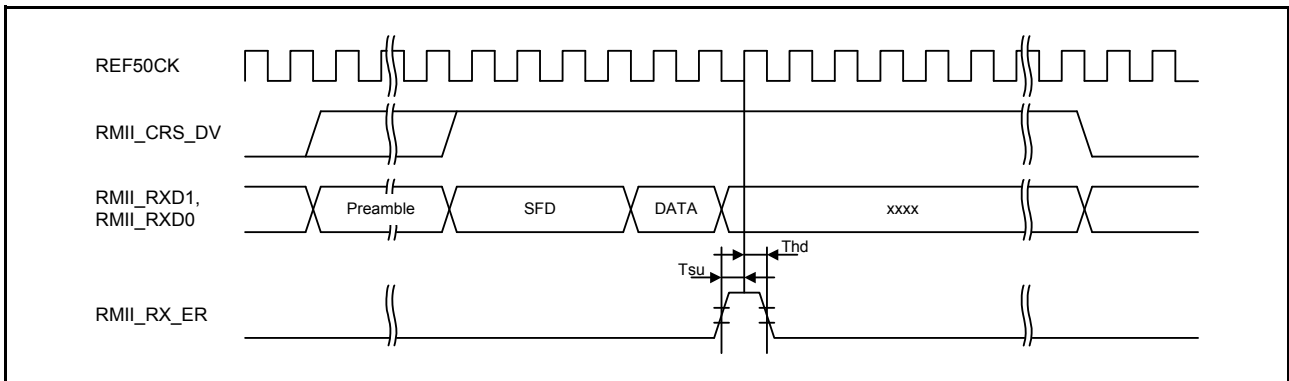


Figure 2.66 RMI reception timing when an error occurs

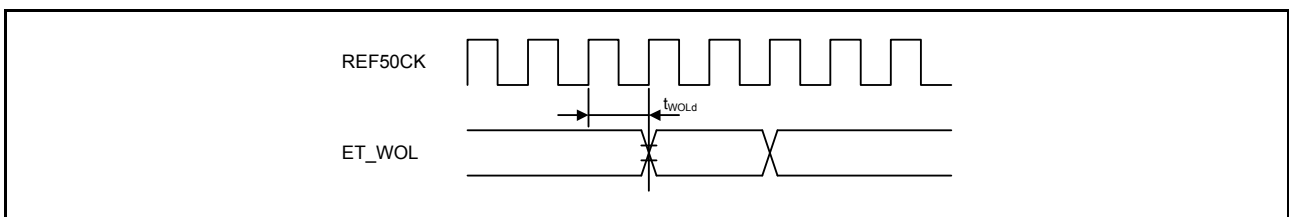


Figure 2.67 WOL output timing for RMI

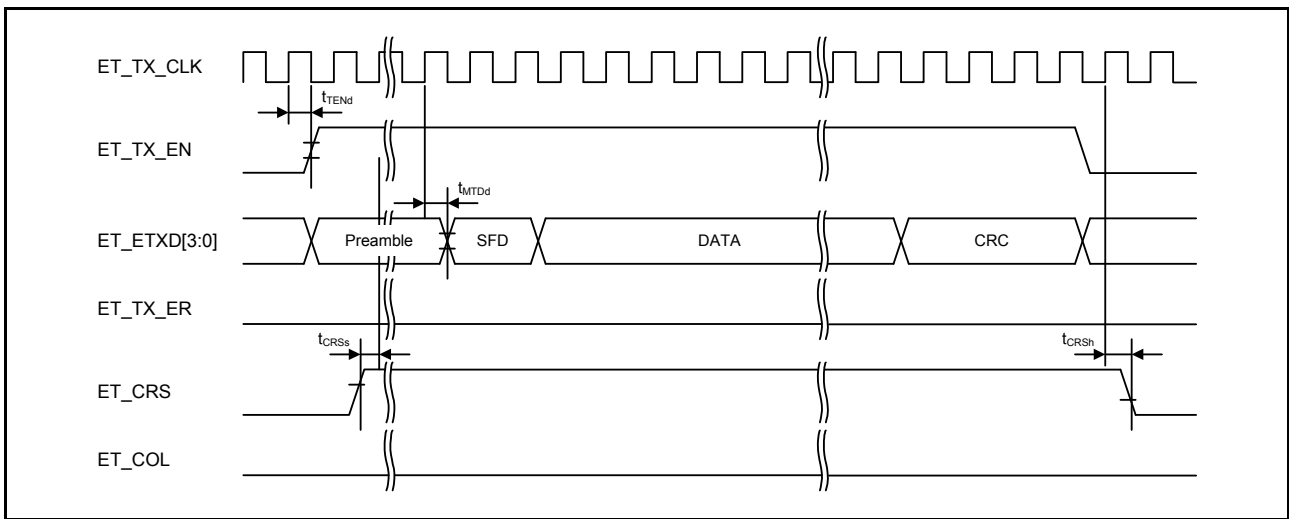


Figure 2.68 MII transmission timing in normal operation

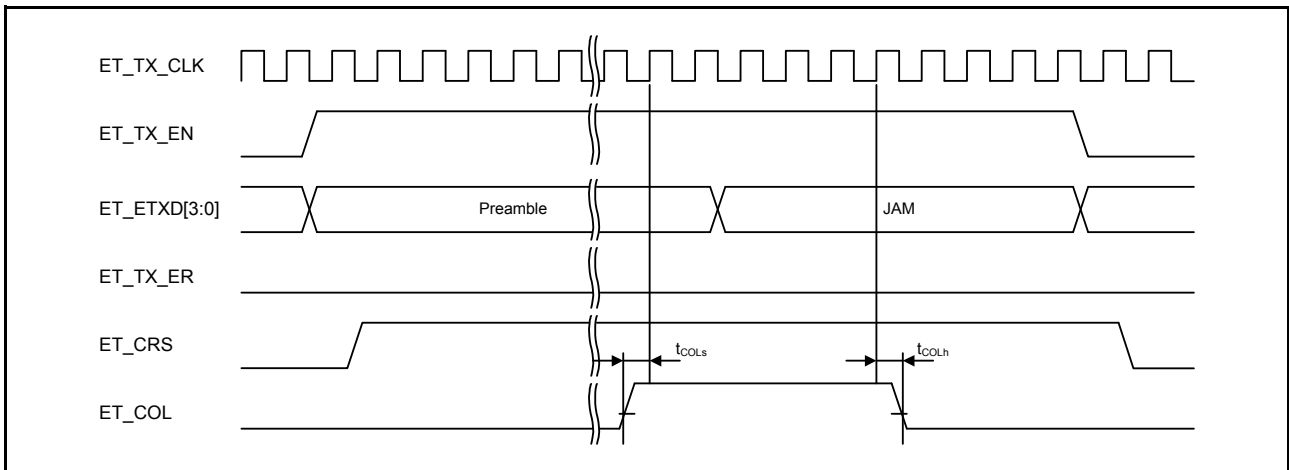


Figure 2.69 MII transmission timing when a conflict occurs

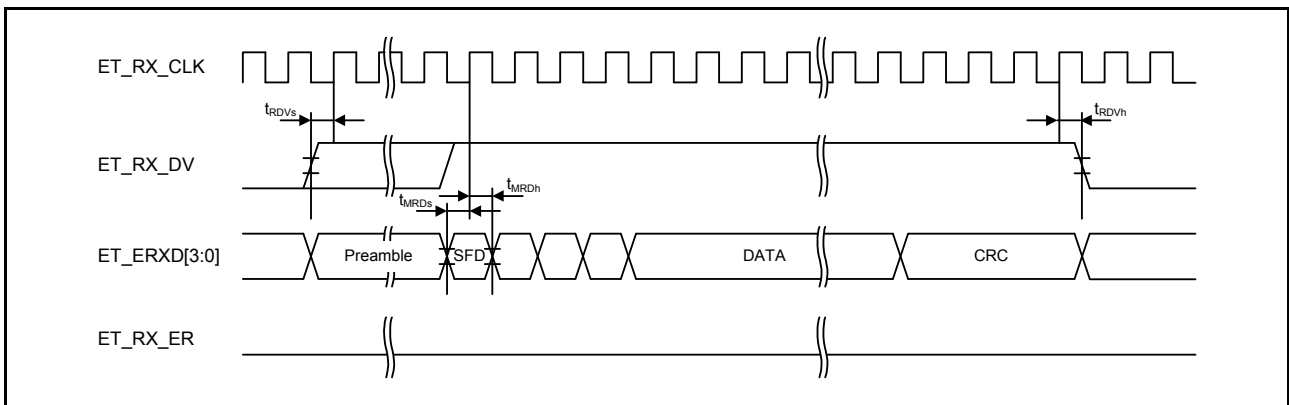


Figure 2.70 MII reception timing in normal operation

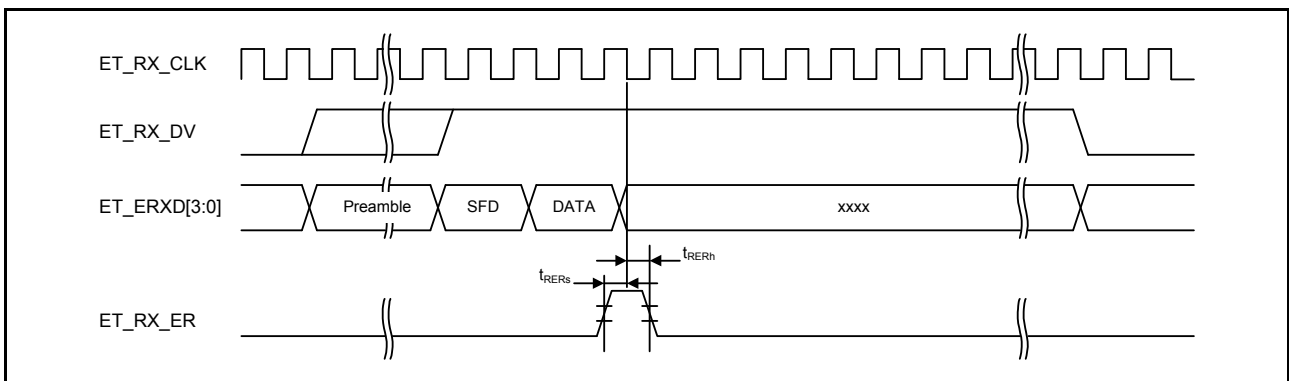


Figure 2.71 MII reception timing when an error occurs

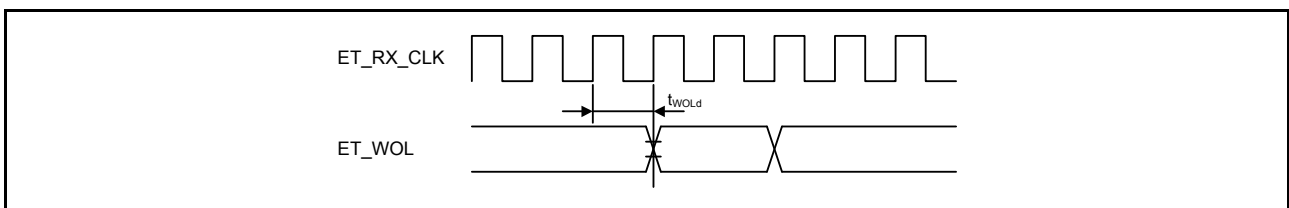


Figure 2.72 WOL output timing for MII

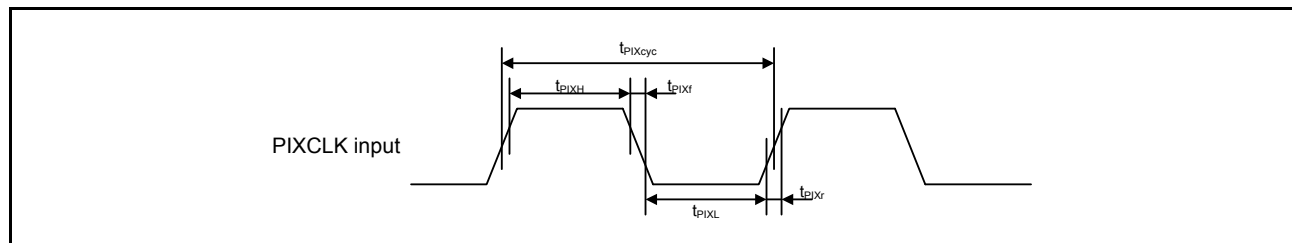
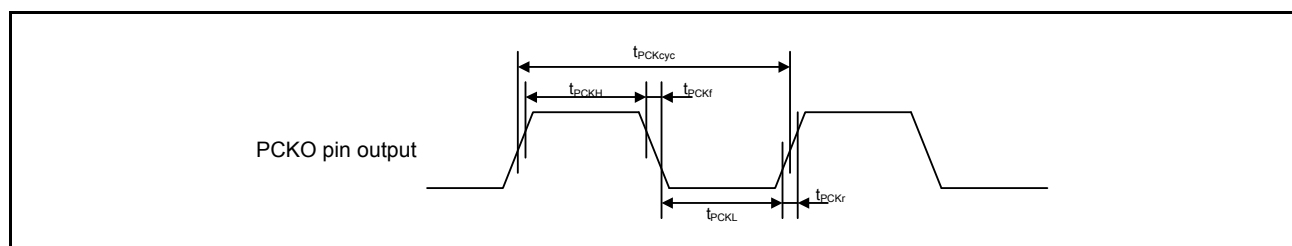
2.3.17 PDC Timing

Table 2.32 PDC timing

Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF

Item	Symbol	Min	Max	Unit	Test conditions	
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	-	ns	Figure 2.73
	PIXCLK input high pulse width	t_{PIXH}	10	-	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	-	ns	
	PIXCLK rise time	t_{PIXr}	-	5	ns	
	PIXCLK fall time	t_{PIXf}	-	5	ns	
PDC	PCKO output cycle time	t_{PCKcyc}	$2 \times t_{PBcyc}$	-	ns	Figure 2.74
	PCKO output high pulse width	t_{PCKH}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	-	ns	
	PCKO output low pulse width	t_{PCKL}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	-	ns	
	PCKO rise time	t_{PCKr}	-	5	ns	
	PCKO fall time	t_{PCKf}	-	5	ns	
PDC	VSYNV/HSYNC input setup time	t_{SYNCS}	10	-	ns	Figure 2.75
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	-	ns	
	PIXD input setup time	t_{PIXDS}	10	-	ns	
	PIXD input hold time	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc} : PCLKB cycle.

**Figure 2.73 PDC input clock timing****Figure 2.74 PDC output clock timing**

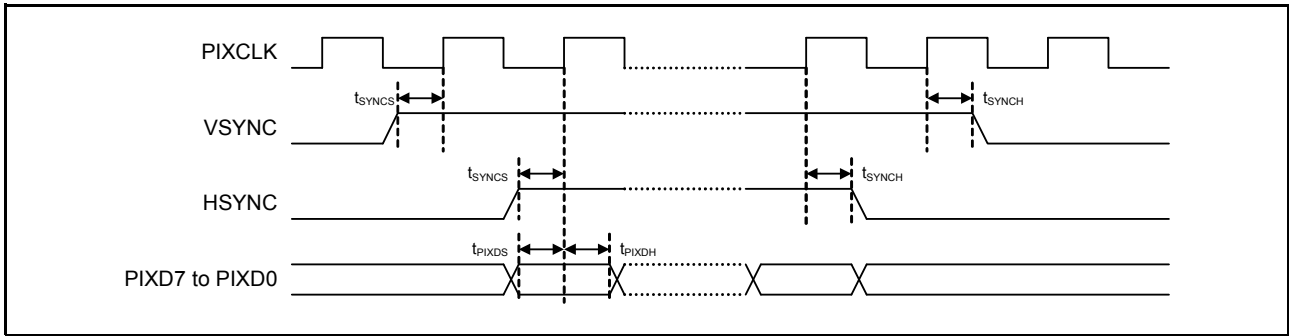


Figure 2.75 PDC AC timing

2.3.18 GLCDC Timing

Table 2.33 GLCDC timing

Conditions:

LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.

LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
LCD_EXTCLK input clock frequency	$t_{E_{cyc}}$	-	-	60*1	MHz	Figure 2.76	
LCD_EXTCLK input clock low pulse width	t_{WL}	0.45	-	0.55	$t_{E_{cyc}}$		
LCD_EXTCLK input clock high pulse width	t_{WH}	0.45	-	0.55			
LCD_CLK output clock frequency	$t_{L_{cyc}}$	-	-	60*1	MHz	Figure 2.77	
LCD_CLK output clock low pulse width	t_{LOL}	0.4	-	0.6	$t_{L_{cyc}}$	Figure 2.77	
LCD_CLK output clock high pulse width	t_{LOH}	0.4	-	0.6	$t_{L_{cyc}}$	Figure 2.77	
LCD data output delay timing	_A or _B combinations*2	t_{DD}	-3.5	-	4	ns	Figure 2.78
	_A and _B combinations*3		-5.0	-	5.5		

Note 1. Parallel RGB888, 666,565: Maximum 54 MHz

Serial RGB888: Maximum 60 MHz (4x speed)

Note 2. Use pins that have a letter appended to their names, for instance, “_A” or “_B”, to indicate

Note 3. Pins of group “_A” and “_B” combinations are used.

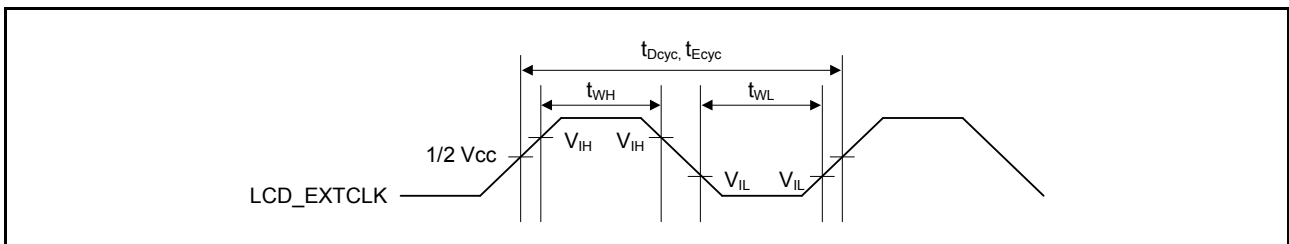


Figure 2.76 LCD_EXTCLK clock input timing

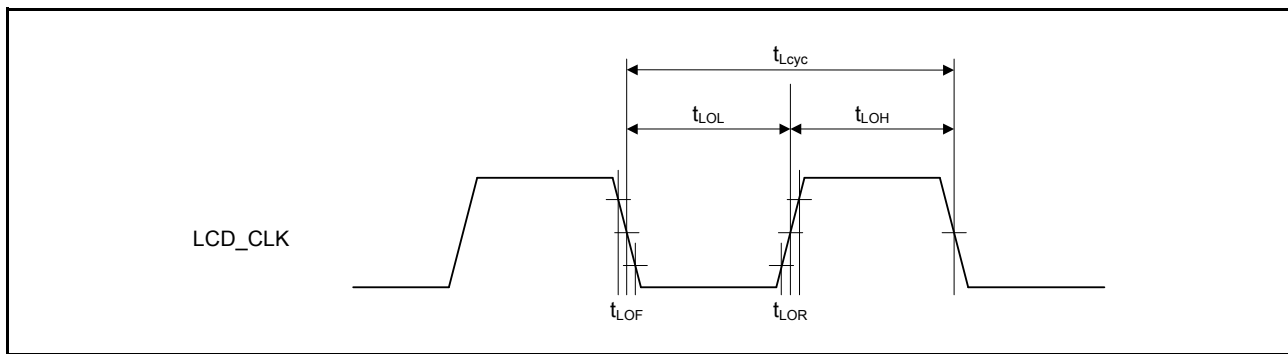


Figure 2.77 LCD_CLK clock output timing

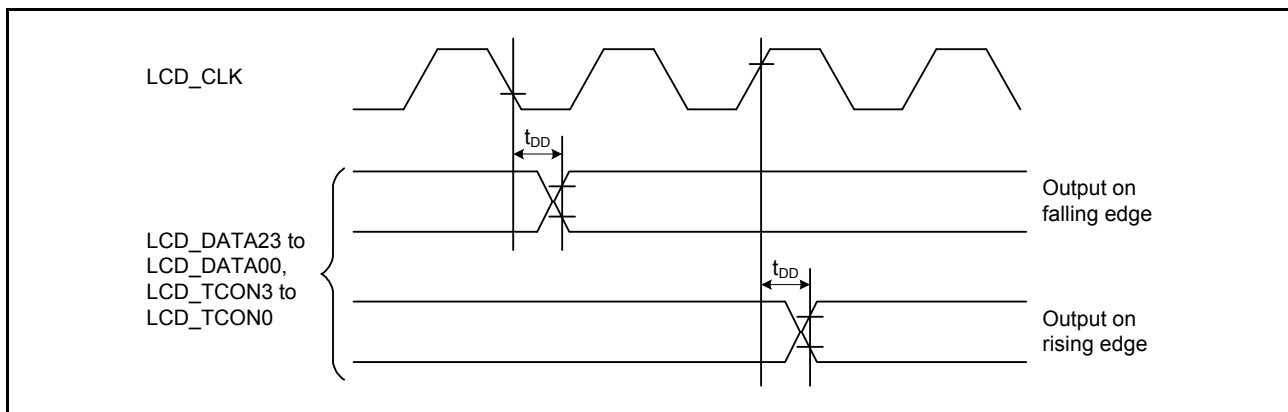


Figure 2.78 Display output timing

2.4 USB Characteristics

2.4.1 USBHS Timing

Table 2.34 USBHS low-speed characteristics for host only (USBHS_DP and USBHS_DM pin characteristics)
 Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	
	Input low voltage	V_{IL}	-	-	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	-	-	V	$ USBHS_DP - USBHS_DM $
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	$I_{OH} = -200 \mu A$
	Output low voltage	V_{OL}	0.0	-	0.3	V	$I_{OL} = 2 \text{ mA}$
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-
	Rise time	t_{LR}	75	-	300	ns	-
	Fall time	t_{LF}	75	-	300	ns	-
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR} / t_{LF}
Pull-up, Pull-down characteristics	USBHS_DP and USBHS_DM pull-down resistors (Host)	R_{pd}	14.25	-	24.80	kΩ	-

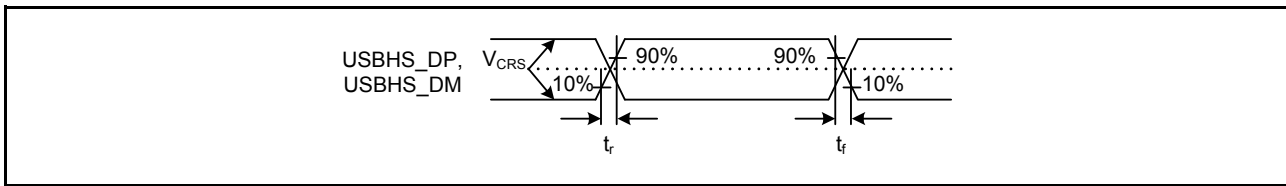


Figure 2.79 USBHS_DP and USBHS_DM output timing in low-speed mode

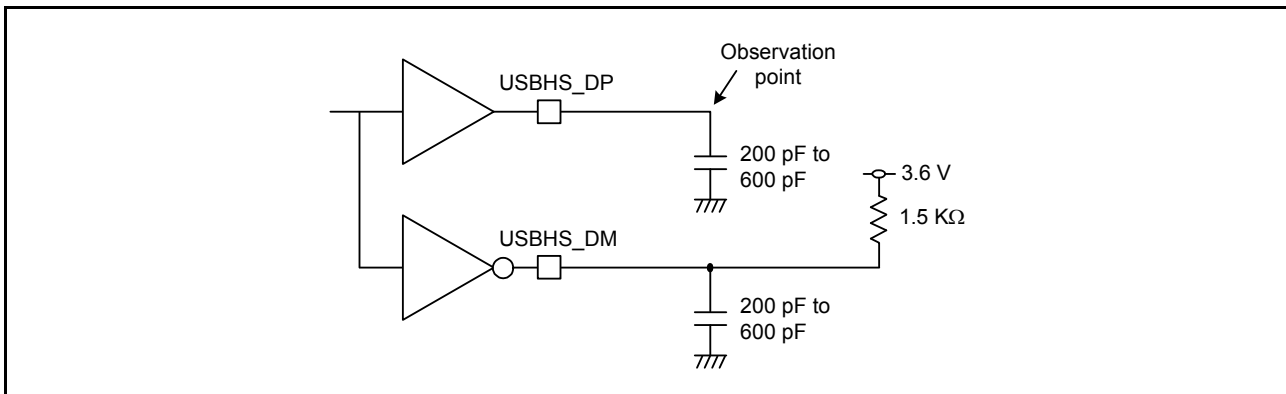


Figure 2.80 Test circuit in low-speed mode

Table 2.35 USBHS full-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	$ USBHS_DP - USBHS_DM $
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	$I_{OH} = -200 \mu A$
	Output low voltage	V_{OL}	0.0	-	0.3	V	$I_{OL} = 2 \text{ mA}$
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-
	Rise time	t_{LR}	4	-	20	ns	-
	Fall time	t_{LF}	4	-	20	ns	-
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR} / t_{FF}
DC characteristics	USBHS_DM pull-up resistor (device)	R_{pu}	0.900	-	1.575	kΩ	During idle state
			1.425	-	3.090	kΩ	During transmission and reception
	USBHS_DP/USBHS_DM pull-down resistor (host)	R_{pd}	14.25	-	24.80	kΩ	-

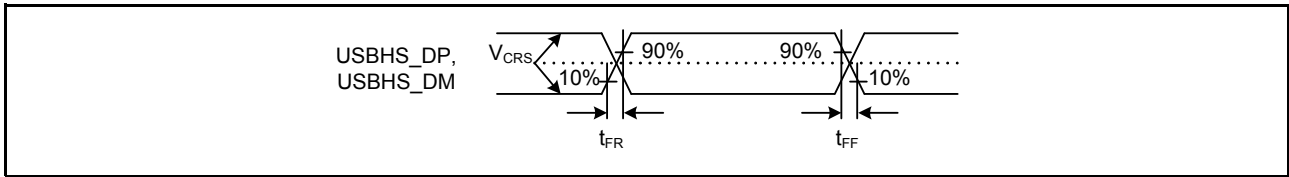


Figure 2.81 USBHS_DP and USBHS_DM output timing in full-speed mode

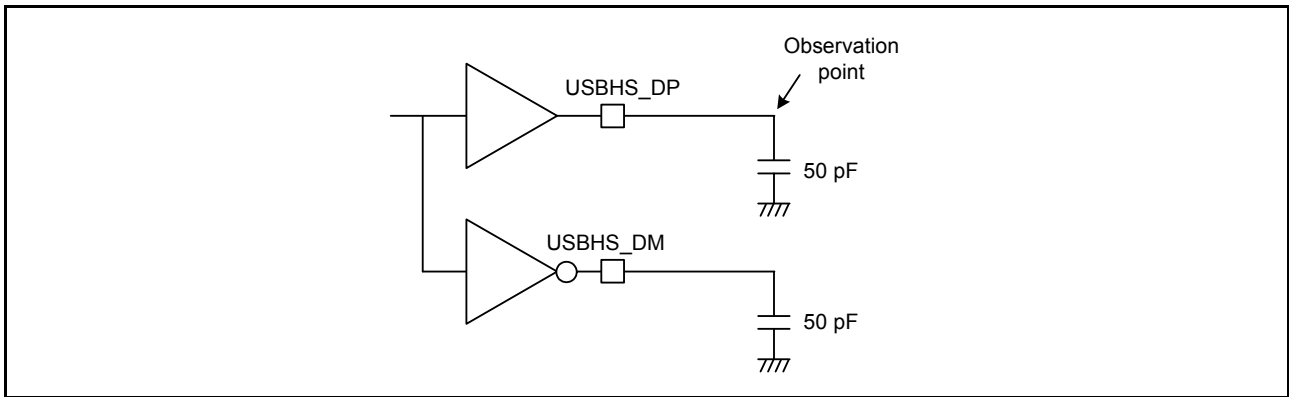


Figure 2.82 Test circuit in full-speed mode

Table 2.36 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
 Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Squelch detect sensitivity	V _{HSSQ}	100	-	150	mV	Figure 2.83
	Disconnect detect sensitivity	V _{HSDSC}	525	-	625	mV	Figure 2.84
	Common-mode voltage	V _{HSCM}	-50	-	500	mV	-
Output characteristics	Idle state	V _{HSOI}	-10.0	-	10	mV	-
	Output high voltage	V _{HSOH}	360	-	440	mV	
	Output low voltage	V _{H SOL}	-10.0	-	10	mV	
	Chirp J output voltage (difference)	V _{CHIRPJ}	700	-	1100	mV	
	Chirp K output voltage (difference)	V _{CHIRPK}	-900	-	-500	mV	
AC characteristics	Rise time	t _{HSR}	500	-	-	ps	Figure 2.85
	Fall time	t _{HSF}	500	-	-	ps	
	Output resistance	Z _{HSDRV}	40.5	-	49.5	Ω	-

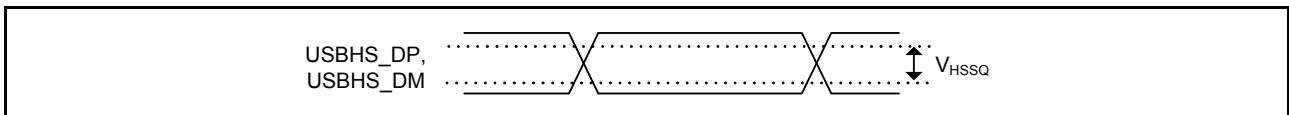


Figure 2.83 USBHS_DP and USBHS_DM squelch detect sensitivity in high-speed mode

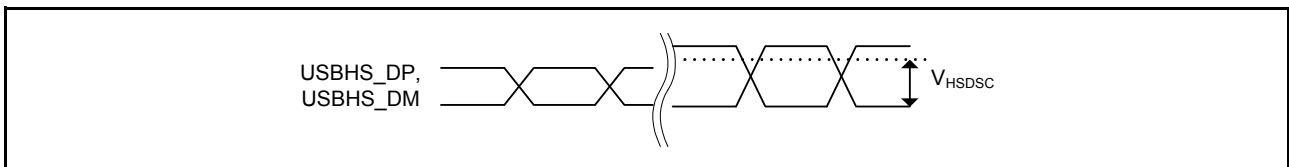


Figure 2.84 USBHS_DP and USBHS_DM disconnect detect sensitivity in high-speed mode

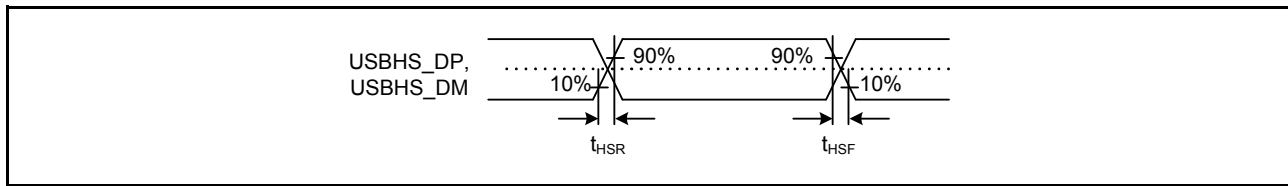


Figure 2.85 USBHS_DP and USBHS_DM output timing in high-speed mode

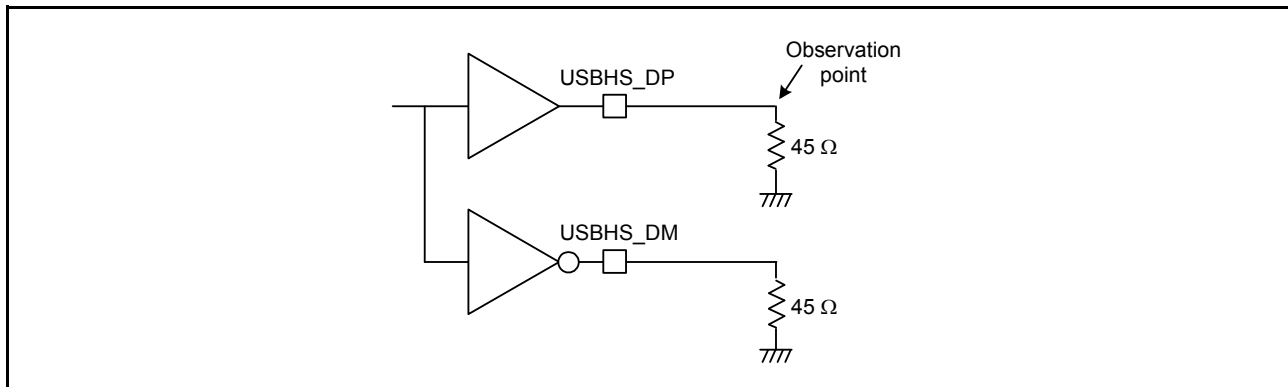


Figure 2.86 Test circuit in high-speed mode

Table 2.37 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)

Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Item		Symbol	Min	Max	Unit	Test conditions
Battery Charging Specification	D+ sink current	I_{DP_SINK}	25	175	μA	-
	D- sink current	I_{DM_SINK}	25	175	μA	-
	DCD source current	I_{DP_SRC}	7	13	μA	-
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V	-
	D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
	D- source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

2.4.2 USBFS Timing

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (1 of 2)

Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, $2.7 \leq V_{REFH0}/V_{REFH} \leq AVCC0$, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	USB_DP - USB_DM
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	$I_{OH} = -200 \mu A$
	Output low voltage	V_{OL}	0.0	-	0.3	V	$I_{OL} = 2 \text{ mA}$
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.87
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR} / t_{LF}

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (2 of 2)
 Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $2.7 \leq V_{REFH0}/V_{REFH} \leq AV_{CC0}$, $V_{CC_USBHS} = AV_{CC_USBHS} = 3.0$ to 3.6 V, $U_{CLK} = 48$ MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	k Ω	-

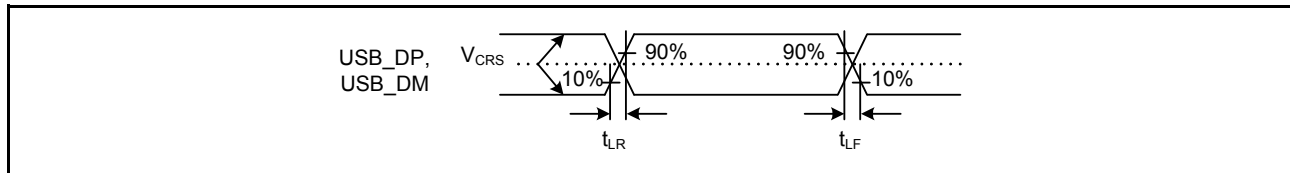


Figure 2.87 USB_DP and USB_DM output timing in low-speed mode

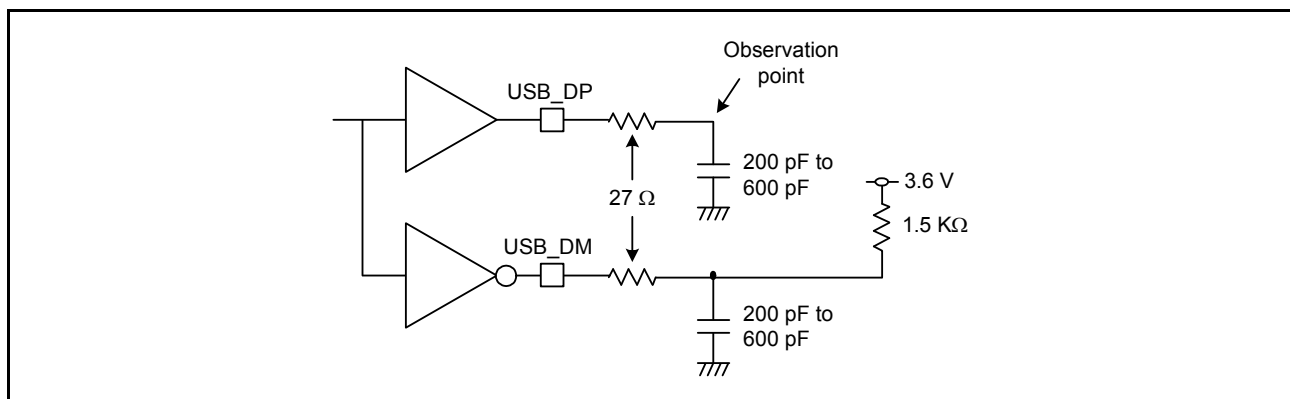


Figure 2.88 Test circuit in low-speed mode

Table 2.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $2.7 \leq V_{REFH0}/V_{REFH} \leq AV_{CC0}$, $V_{CC_USBHS} = AV_{CC_USBHS} = 3.0$ to 3.6 V, $U_{CLK} = 48$ MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	$ USB_DP - USB_DM $
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	$I_{OH} = -200 \mu A$
	Output low voltage	V_{OL}	0.0	-	0.3	V	$I_{OL} = 2$ mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.89
	Rise time	t_{LR}	4	-	20	ns	
	Fall time	t_{LF}	4	-	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR} / t_{FF}
	Output resistance	Z_{DRV}	28	-	44	Ω	USBFS: $R_s = 27 \Omega$ included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	-	1.575	k Ω	During idle state
			1.425	-	3.090	k Ω	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	k Ω	-

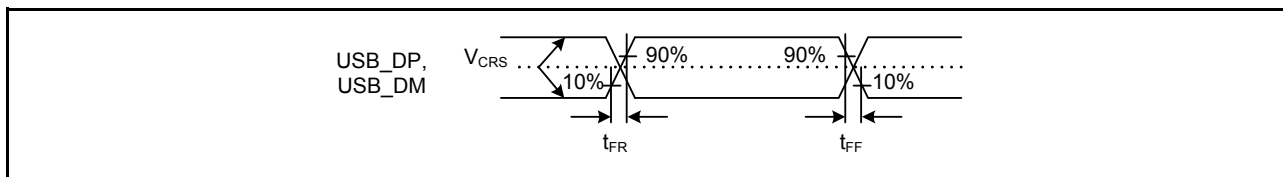


Figure 2.89 USB_DP and USB_DM output timing in full-speed mode

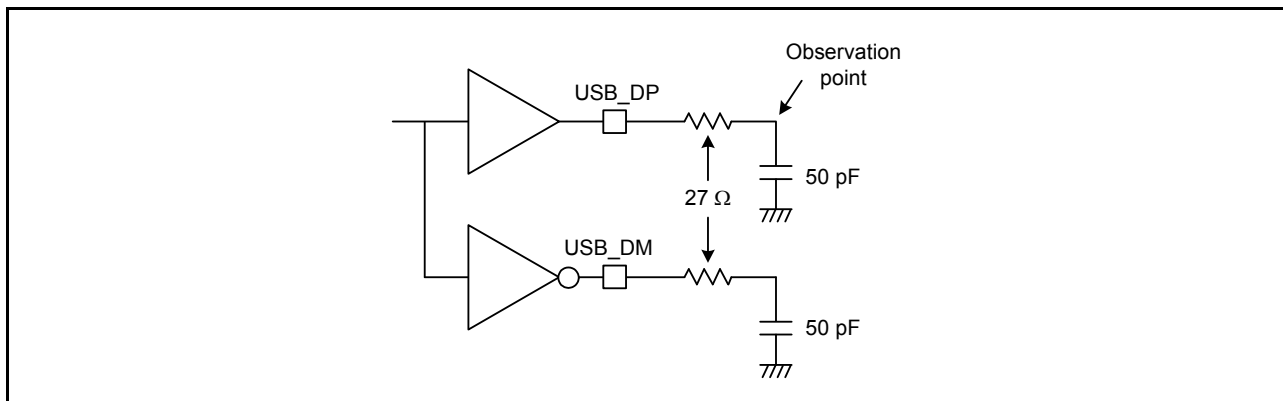


Figure 2.90 Test circuit in full-speed mode

2.5 ADC12 Characteristics

[Normal-precision channel]

Table 2.40 A/D conversion characteristics for unit 0 (1 of 2)

Conditions: PCLKC = 1 to 60 MHz

Item	Min	Typ	Max	Unit	Test conditions		
Frequency	1	-	60	MHz	-		
Analog input capacitance	-	-	30	pF	-		
Quantization error	-	±0.5	-	LSB	-		
Resolution	-	-	12	Bits	-		
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	<ul style="list-style-type: none"> • Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error	-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V	
	Full-scale error	-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V	
	Absolute accuracy	-	±2.5	±5.5	LSB	-	
	DNL differential nonlinearity error	-	±1.0	±2.0	LSB	-	
	INL integral nonlinearity error	-	±1.5	±3.0	LSB	-	
	Holding characteristics of sample-and hold circuits	-	-	20	μs	-	
Dynamic range	0.25	-	VREFH0 - 0.25	V	-		
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
	Offset error	-	±1.0	±2.5	LSB	-	
	Full-scale error	-	±1.0	±2.5	LSB	-	
	Absolute accuracy	-	±2.0	±4.5	LSB	-	
	INL integral nonlinearity error	-	±1.0	±2.5	LSB	-	

Table 2.40 A/D conversion characteristics for unit 0 (2 of 2)

Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
High-precision channels (AN003 to AN007)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN016 to AN020)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	μs	Sampling in 40 states
		Offset error		-	±1.0	±5.5	LSB
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.

The use of pins AN000 to AN007 as digital outputs is not allowed when the 12-Bit A/D converter is used.

The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.41 A/D conversion characteristics for unit 1 (1 of 2)

Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
		Offset error		-	±1.5	±3.5	LSB
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	μs	-
	Dynamic range		0.25	-	VREFH - 0.25	V	-

Table 2.41 A/D conversion characteristics for unit 1 (2 of 2)

Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN103, AN105 to AN107)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	μs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	μs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
INL integral nonlinearity error		-	±1.0	±2.5	LSB	-	
Normal-precision channels (AN116 to AN119)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	μs	Sampling in 40 states
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of pins AN100 to AN103, AN105 to AN107 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.42 A/D conversion characteristics for simultaneous using of channel-dedicated sample-and-hold circuits in unit0 and unit1

Conditions: PCLKC = 30/60 MHz

Item	Min	Typ	Max	Test conditions
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±5.0
	Full-scale error	-	±2.5	±5.0
	Absolute accuracy	-	±4.0	±8.0
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±5.0
	Full-scale error	-	±2.5	±5.0
	Absolute accuracy	-	±4.0	±8.0
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±3.5
	Full-scale error	-	±1.5	±3.5
	Absolute accuracy	-	±3.0	±5.5
Channel-dedicated sample-and-hold circuits in use with continuous sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±3.5
	Full-scale error	-	±1.5	±3.5
	Absolute accuracy	-	±3.0	±5.5

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit0 and unit1, setting the ADSHMSR.SHMD bit to 1 is recommended.

Table 2.43 A/D internal reference voltage characteristics

Item	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	-
Sampling time	4.15	-	-	μs	-

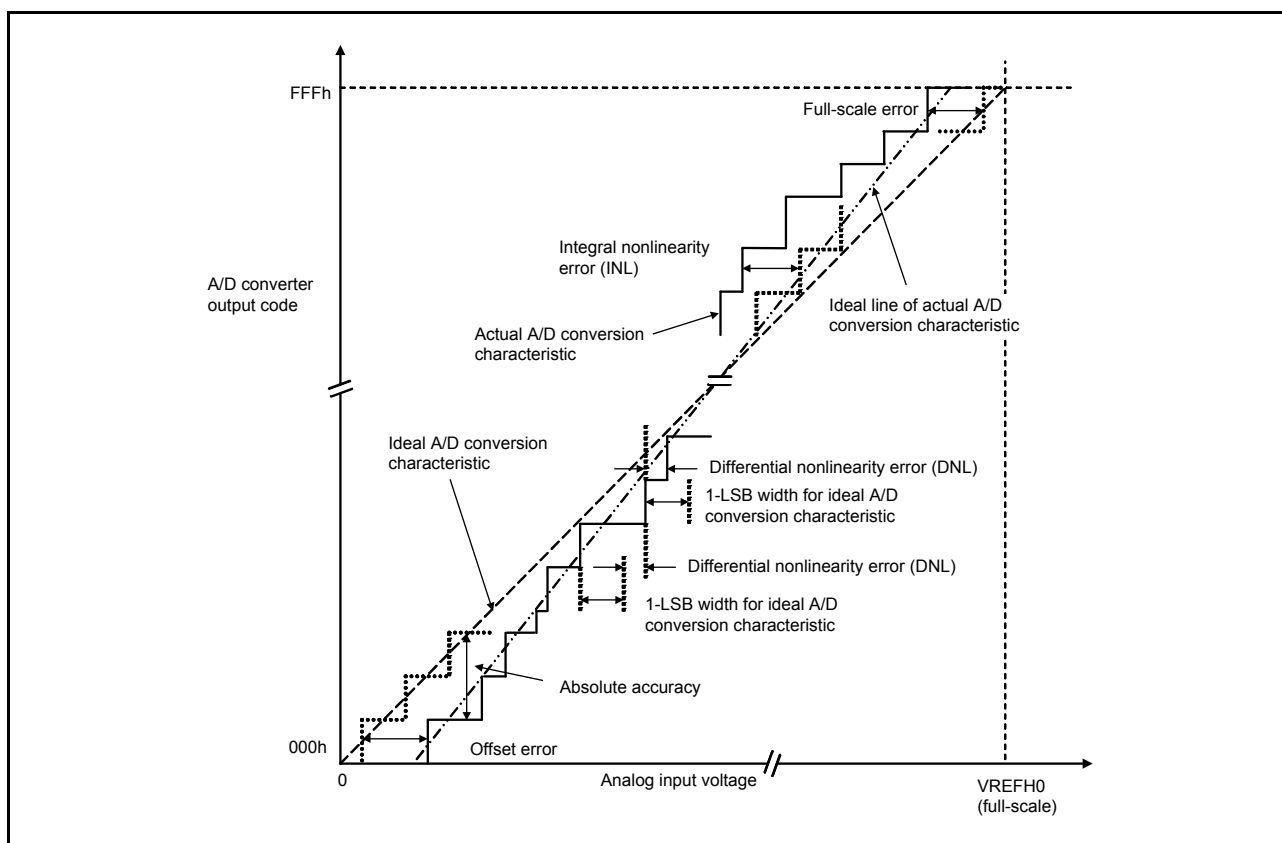


Figure 2.91 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage $V_{REFH0} = 3.072$ V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ± 5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics**Table 2.44 D/A conversion characteristics**

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
INL	-	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	-	±1.0	±2.0	LSB	-
Output impedance	-	8.5	-	kΩ	-
Conversion time	-	-	3.0	μs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	-	VREFH	V	-
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	μs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH - 0.2	V	-

2.7 TSN Characteristics**Table 2.45 TSN characteristics**

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.0	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t _{START}	-	-	30	μs	-
Sampling time	-	4.15	-	-	μs	-

2.8 OSC Stop Detect Characteristics**Table 2.46 Oscillation stop detection circuit characteristics**

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t _{dr}	-	-	1	ms	Figure 2.92

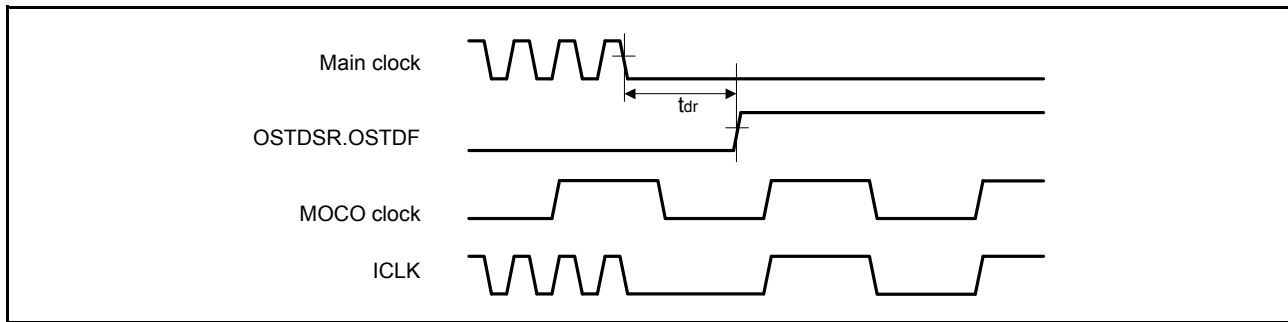


Figure 2.92 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.47 Power-on reset circuit and voltage detection circuit characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions		
Voltage detection level	Power-on reset (POR)	Module-stop function disabled*2	V_{POR}	2.5	2.6	2.7	V	Figure 2.93
				Module-stop function enabled*3	1.8	2.25		
	Voltage detection circuit (LVD0)	V_{det0_1}	2.84	2.94	3.04		Figure 2.94	
		V_{det0_2}	2.77	2.87	2.97			
		V_{det0_3}	2.70	2.80	2.90			
	Voltage detection circuit (LVD1)	V_{det1_1}	2.89	2.99	3.09		Figure 2.95	
		V_{det1_2}	2.82	2.92	3.02			
		V_{det1_3}	2.75	2.85	2.95			
	Voltage detection circuit (LVD2)	V_{det2_1}	2.89	2.99	3.09		Figure 2.96	
		V_{det2_2}	2.82	2.92	3.02			
		V_{det2_3}	2.75	2.85	2.95			
	Internal reset time	Power-on reset time	t_{POR}	-	4.5	-	ms	Figure 2.93
LVD0 reset time		t_{LVD0}	-	0.51	-	Figure 2.94		
LVD1 reset time		t_{LVD1}	-	0.38	-	Figure 2.95		
LVD2 reset time		t_{LVD2}	-	0.38	-	Figure 2.96		
Minimum VCC down time*1	t_{VOFF}	200	-	-	μ s	Figure 2.93, Figure 2.94		
Response delay	t_{det}	-	-	200	μ s	Figure 2.93 to Figure 2.96		
LVD operation stabilization time (after LVD is enabled)	$t_{d(E-A)}$	-	-	10	μ s	Figure 2.95, Figure 2.96		
Hysteresis width (LVD1 and LVD2)	V_{LVH}	-	70	-	mV			

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for POR and LVD.

Note 2. The low-power function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 3. The low-power function is enabled and DEEPCUT[1:0] = 11b.

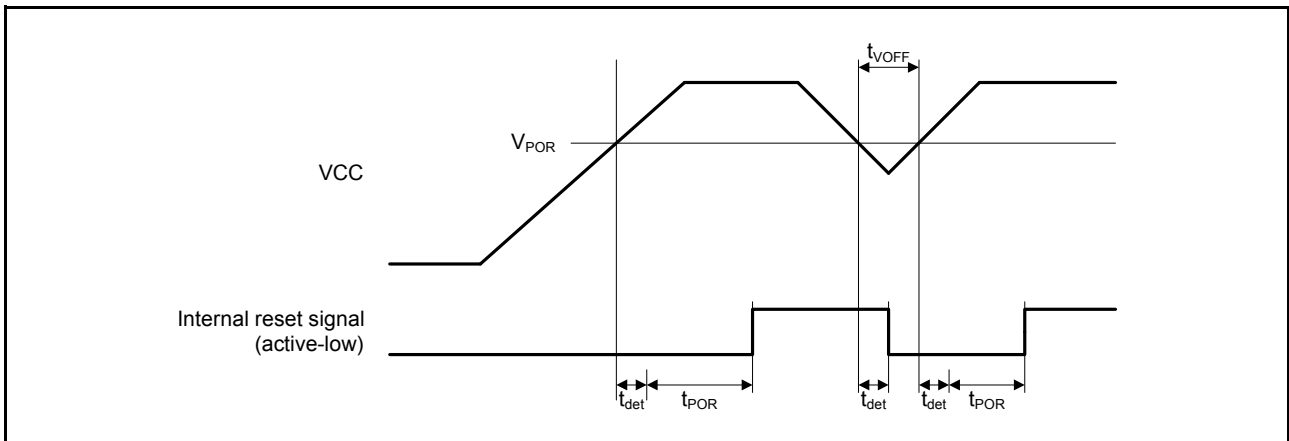


Figure 2.93 Power-on reset timing

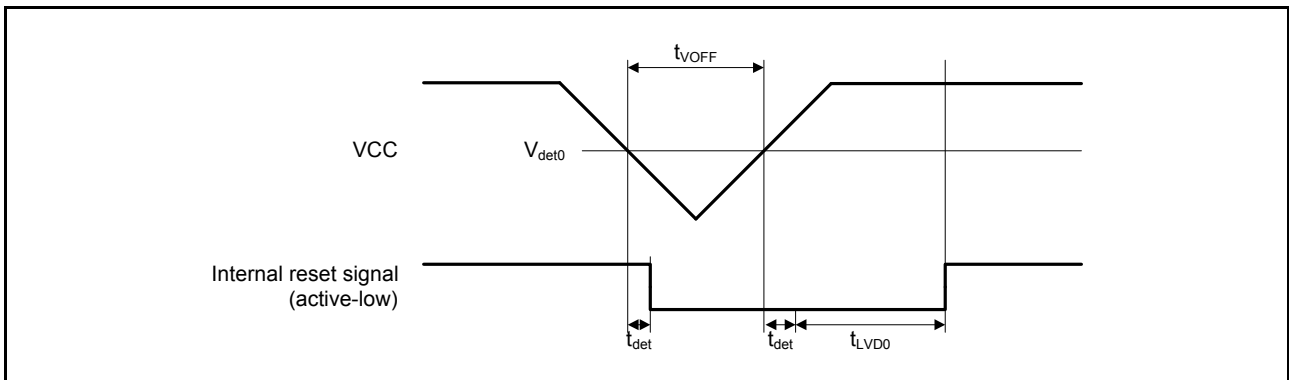


Figure 2.94 Voltage detection circuit timing (V_{det0})

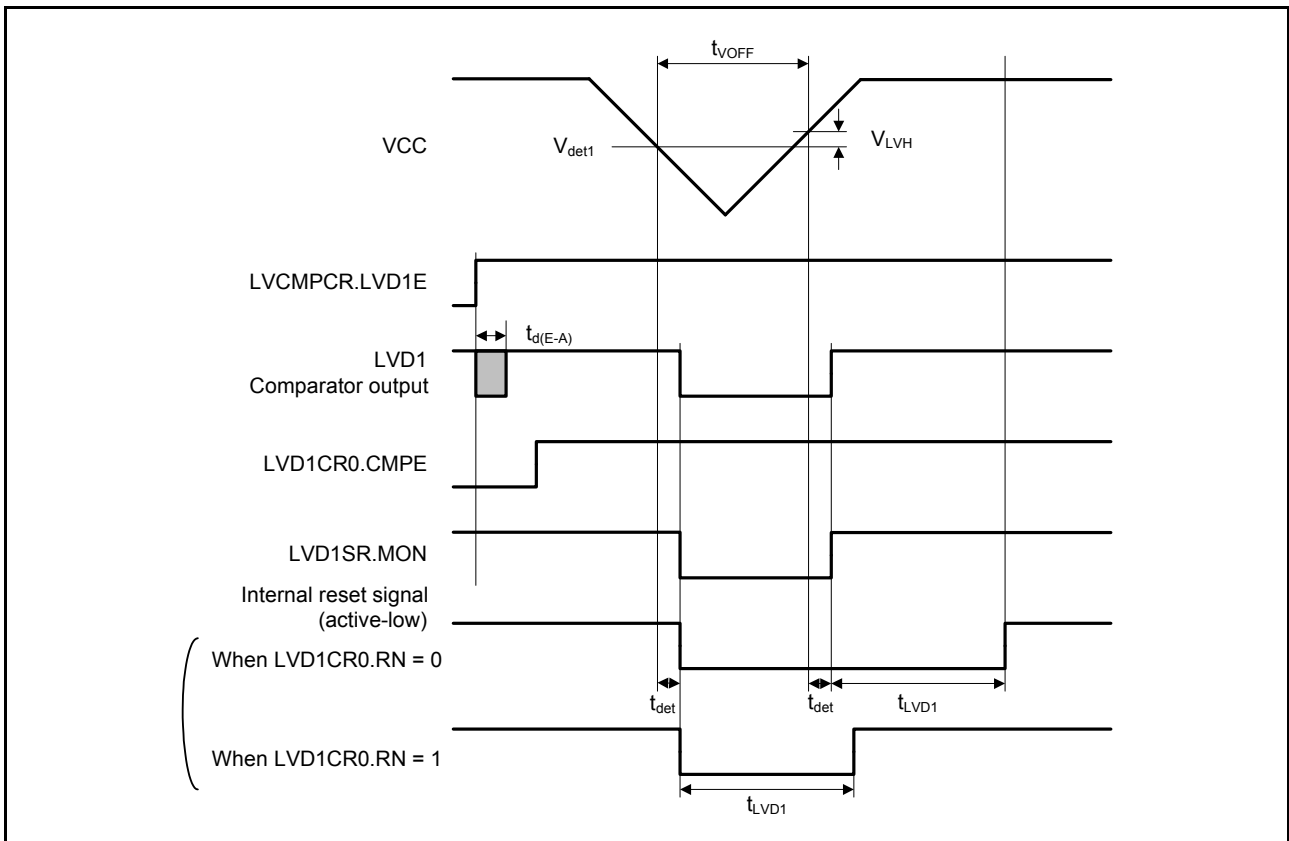


Figure 2.95 Voltage detection circuit timing (V_{det1})

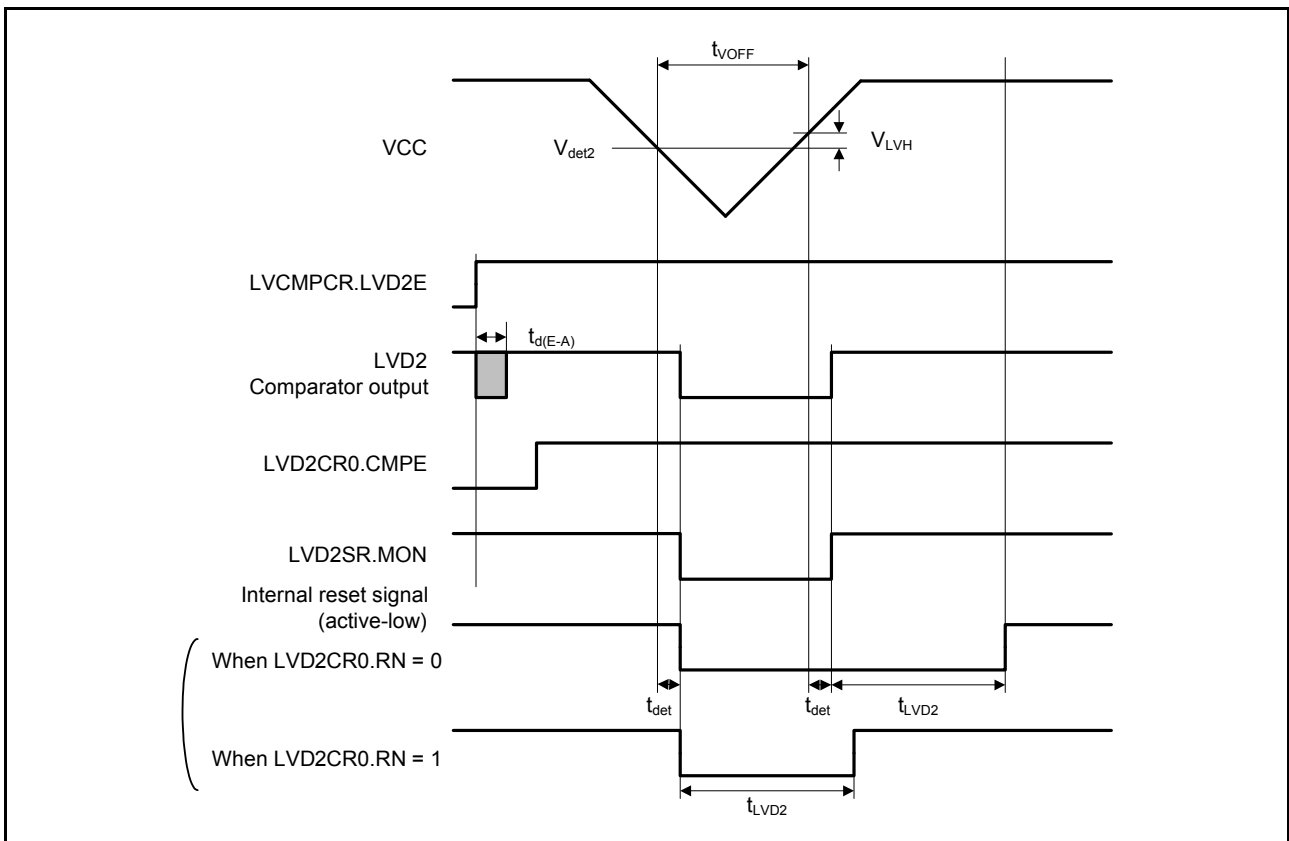


Figure 2.96 Voltage detection circuit timing (V_{det2})

2.10 VBATT Characteristics

Table 2.48 Battery backup function characteristics

Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0}/V_{REFH} \leq AV_{CC0}$, $V_{BATT} = 1.8$ to 3.6 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DET\text{BATT}}$	2.50	2.60	2.70	V	Figure 2.97
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	$V_{BATT\text{SW}}$	2.70	-	-	V	
VCC-off period for starting power supply switching	$t_{V\text{OFFBATT}}$	200	-	-	μs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DET\text{BATT}}$).

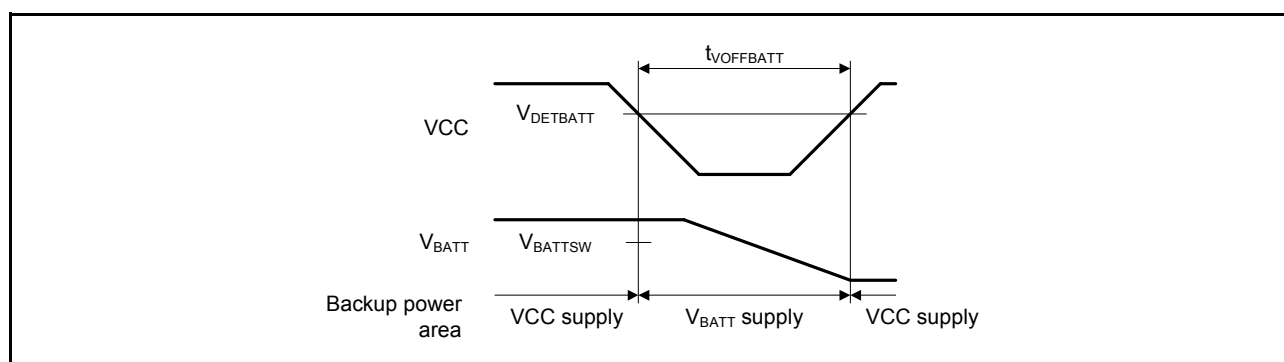


Figure 2.97 Battery backup function characteristics

2.11 CTSU Characteristics

Table 2.49 CTSU characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣI_{OH}	-	-	-40	mA	When the mutual capacitance method is applied

2.12 ACPHPS Characteristics

Table 2.50 ACPHPS characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	V_{REF}	0	-	AV_{CC0}	V	-
Input voltage range	V_{I}	0	-	AV_{CC0}	V	-
Output delay*1	T_{d}	-	50	100	ns	$V_{\text{I}} = V_{\text{REF}} \pm 100$ mV
Internal reference voltage	V_{ref}	1.13	1.18	1.23	V	-

Note 1. This value is the internal propagation delay.

2.13 PGA Characteristics

Table 2.51 PGA characteristics in single mode

Item	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	$0.050 \times AVCC0$	-	$0.45 \times AVCC0$	V
	AIN1 (G = 2.500)	$0.047 \times AVCC0$	-	$0.360 \times AVCC0$	V
	AIN2 (G = 2.667)	$0.046 \times AVCC0$	-	$0.337 \times AVCC0$	V
	AIN3 (G = 2.857)	$0.046 \times AVCC0$	-	$0.32 \times AVCC0$	V
	AIN4 (G = 3.077)	$0.045 \times AVCC0$	-	$0.292 \times AVCC0$	V
	AIN5 (G = 3.333)	$0.044 \times AVCC0$	-	$0.265 \times AVCC0$	V
	AIN6 (G = 3.636)	$0.042 \times AVCC0$	-	$0.247 \times AVCC0$	V
	AIN7 (G = 4.000)	$0.040 \times AVCC0$	-	$0.212 \times AVCC0$	V
	AIN8 (G = 4.444)	$0.036 \times AVCC0$	-	$0.191 \times AVCC0$	V
	AIN9 (G = 5.000)	$0.033 \times AVCC0$	-	$0.17 \times AVCC0$	V
	AIN10 (G = 5.714)	$0.031 \times AVCC0$	-	$0.148 \times AVCC0$	V
	AIN11 (G = 6.667)	$0.029 \times AVCC0$	-	$0.127 \times AVCC0$	V
	AIN12 (G = 8.000)	$0.027 \times AVCC0$	-	$0.09 \times AVCC0$	V
	AIN13 (G = 10.000)	$0.025 \times AVCC0$	-	$0.08 \times AVCC0$	V
AIN14 (G = 13.333)	$0.023 \times AVCC0$	-	$0.06 \times AVCC0$	V	
Gain error	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
Offset error	Voff	-8	-	8	mV

Table 2.52 PGA characteristics in differential mode (1 of 2)

Item	Symbol	Min	Typ	Max	Unit	
PGAVSS input voltage range	PGAVSS	-0.5	-	0.3	V	
Differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V

Table 2.52 PGA characteristics in differential mode (2 of 2)

Item	Symbol	Min	Typ	Max	Unit	
Gain error	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

2.14 Flash Memory Characteristics

2.14.1 Code Flash Memory Characteristics

Table 2.53 Code flash memory characteristics

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

Item	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions	
		Min	Typ	Max	Min	Typ	Max			
Programming time N _{PEC} ≤ 100 times	128-byte	t _{P128}	-	1.1	13.2	-	0.52	6.0	ms	
	8-KB	t _{P8K}	-	75	176	-	34	80	ms	
	32-KB	t _{P32K}	-	299	704	-	136	320	ms	
Programming time N _{PEC} > 100 times	128-byte	t _{P128}	-	1.4	15.8	-	0.62	7.2	ms	
	8-KB	t _{P8K}	-	90	212	-	41	96	ms	
	32-KB	t _{P32K}	-	359	848	-	163	384	ms	
Erasure time N _{PEC} ≤ 100 times	8-KB	t _{E8K}	-	92	216	-	51	120	ms	
	32-KB	t _{E32K}	-	329	864	-	183	480	ms	
Erasure time N _{PEC} > 100 times	8-KB	t _{E8K}	-	110	260	-	61	144	ms	
	32-KB	t _{E32K}	-	396	1040	-	220	576	ms	
Reprogramming/erase cycle*Note:	N _{PEC}	10000*1	-	-	-	10000*1	-	-	Times	
Suspend delay during programming	t _{SPD}	-	-	264	-	-	120	μs		
First suspend delay during erasure in suspend priority mode	t _{SESD1}	-	-	216	-	-	120	μs		
Second suspend delay during erasure in suspend priority mode	t _{SESD2}	-	-	1.7	-	-	1.7	ms		
Suspend delay during erasure in erasure priority mode	t _{SEED}	-	-	1.7	-	-	1.7	ms		
Forced stop command	t _{FD}	-	-	32	-	-	20	μs		
Data hold time*2	t _{DRP}	10*2, *3	-	-	-	10*2, *3	-	-	Years	Ta = +85°C
		30*2, *3	-	-	-	30*2, *3	-	-		

Note: The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

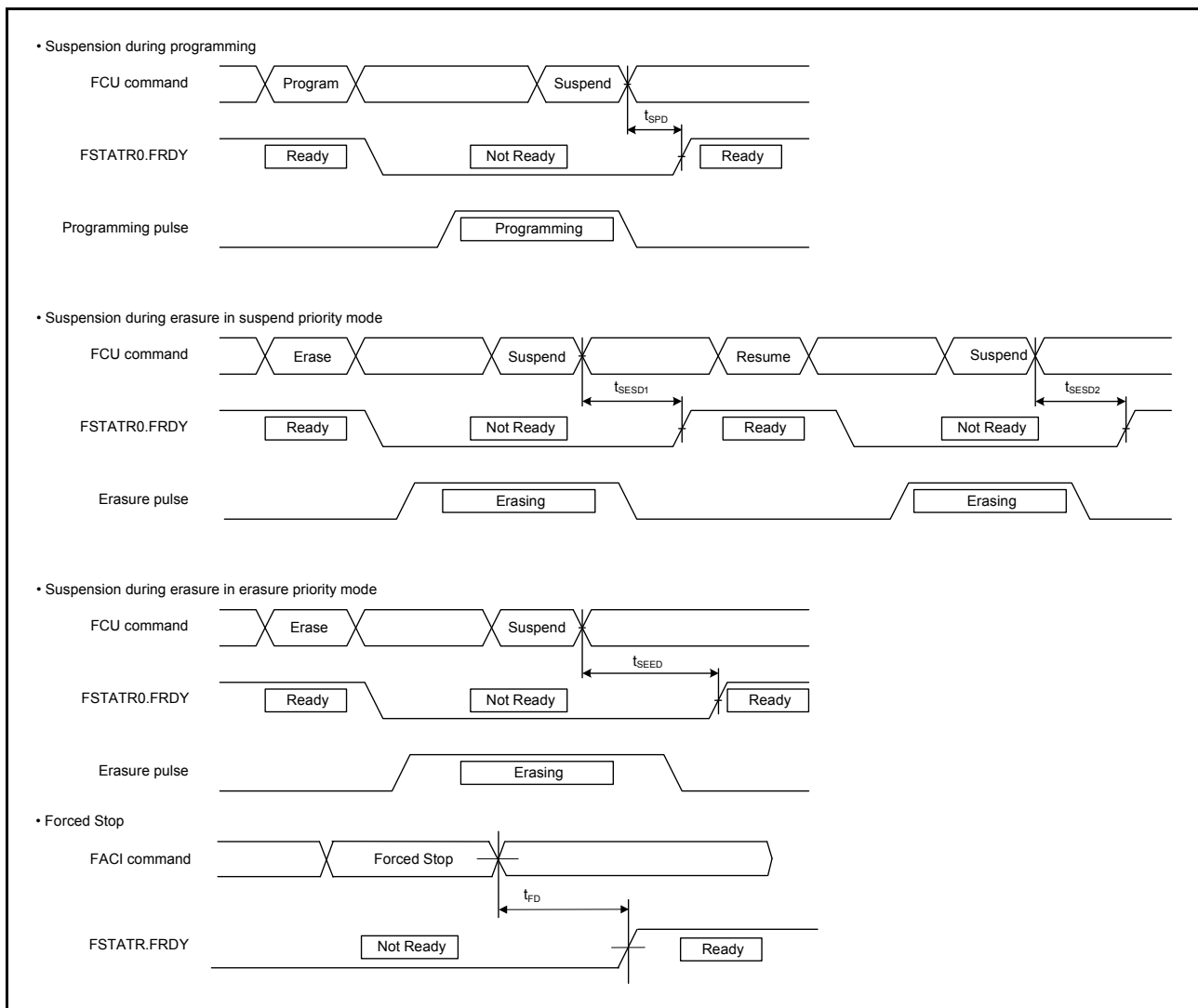


Figure 2.98 Suspension and forced stop timing for flash memory programming and erasure

2.14.2 Data Flash Memory Characteristics

Table 2.54 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

Item	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
		Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t_{DP4}	-	0.46	3.8	-	0.21	1.7	ms
	8-byte	t_{DP8}	-	0.48	4.0	-	0.22	1.8	
	16-byte	t_{DP16}	-	0.53	4.5	-	0.24	2.0	
Erasure time	64-byte	t_{DE64}	-	4.03	18	-	2.24	10	ms
	128-byte	t_{DE128}	-	6.2	27	-	3.4	15	
	256-byte	t_{DE256}	-	11.6	50	-	6.4	28	
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	μs
Reprogramming/erasure cycle*1	N_{DPEC}	125000*2	-	-	-	125000*2	-	-	-

Table 2.54 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Suspend delay during programming	4-byte	t_{DSPD}	-	-	264	-	-	120	μs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	-	-	216	-	-	120	μs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	-	-	300	-	-	300	μs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Forced stop command		t_{FD}	-	-	32	-	-	20	μs	
Data hold time*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	Ta = +85°C
			30*3,*4	-	-	30*3,*4	-	-		

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 4. This result is obtained from reliability testing.

2.15 Boundary Scan

Table 2.55 Boundary scan characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 2.99
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 2.100
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	40	ns	Figure 2.101
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	-	-	-	

Note 1. Boundary scan does not function until the power-on reset becomes negative.

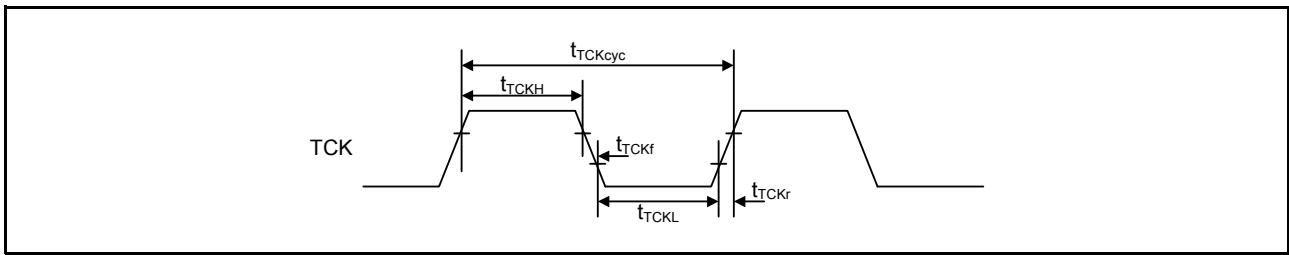


Figure 2.99 Boundary scan TCK timing

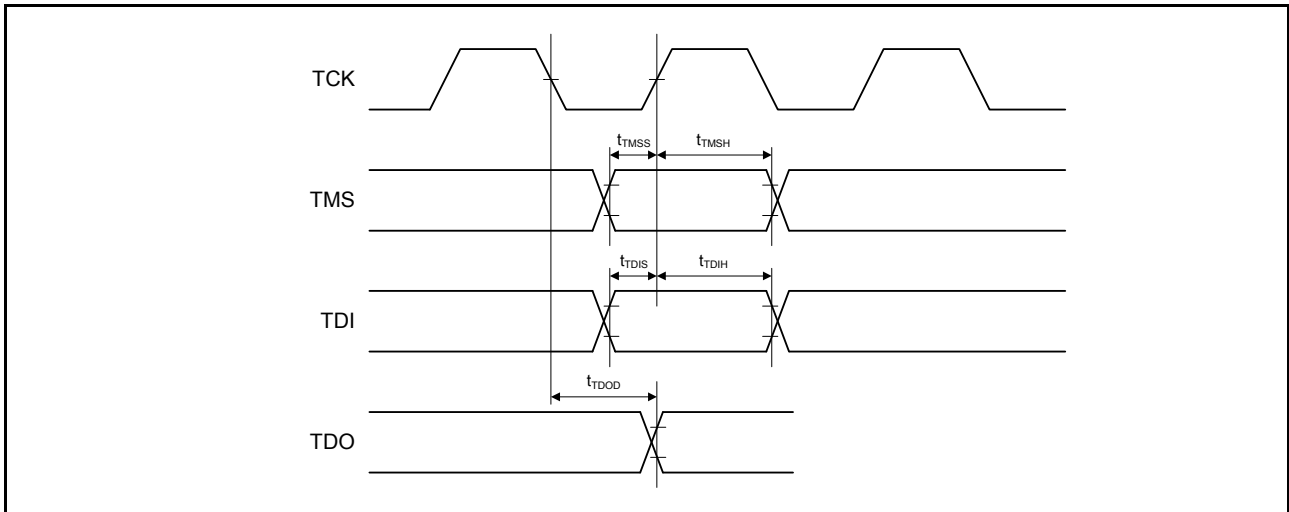


Figure 2.100 Boundary scan input/output timing

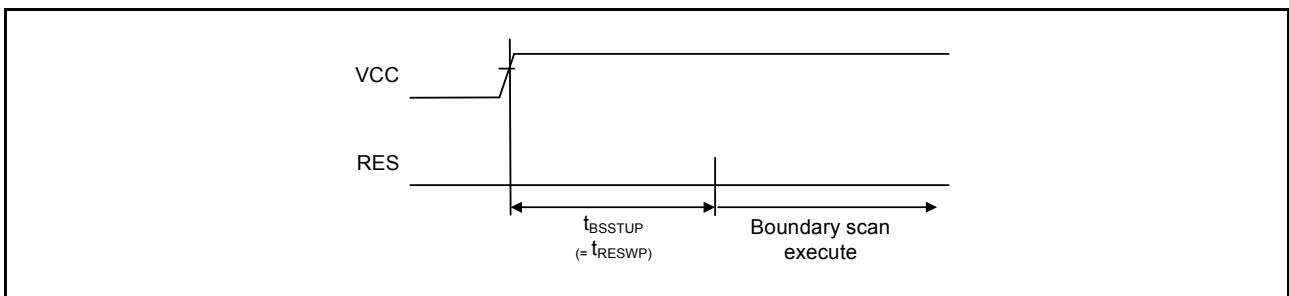


Figure 2.101 Boundary scan circuit startup timing

2.16 Joint European Test Action Group (JTAG)

Table 2.56 JTAG

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	-	-	ns	Figure 2.99
TCK clock high pulse width	t_{TCKH}	15	-	-	ns	
TCK clock low pulse width	t_{TCKL}	15	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	

Table 2.56 JTAG

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TMS setup time	t_{TMSS}	8	-	-	ns	Figure 2.100
TMS hold time	t_{TMSH}	8	-	-	ns	
TDI setup time	t_{TDIS}	8	-	-	ns	
TDI hold time	t_{TDIH}	8	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	20	ns	

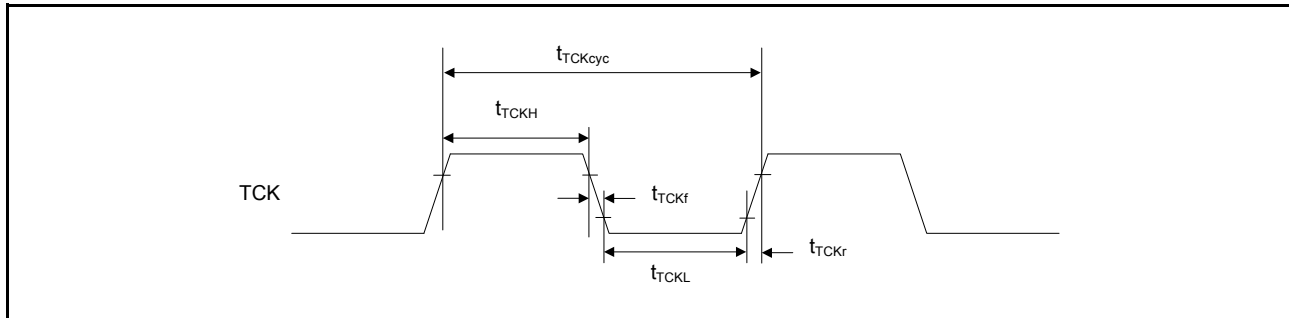


Figure 2.102 JTAG TCK timing

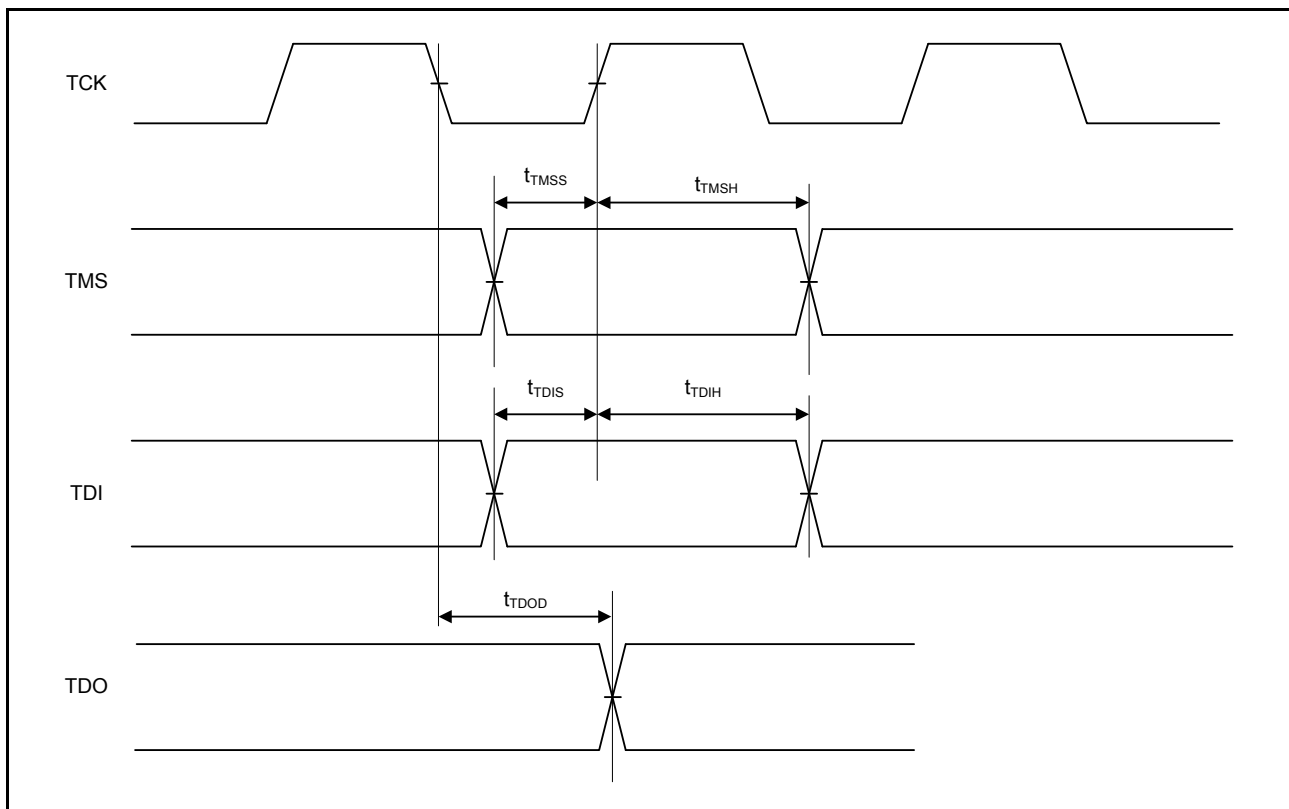


Figure 2.103 JTAG input/output timing

2.17 Serial Wire Debug (SWD)

Table 2.57 SWD

Item	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	t_{SWCKcyc}	40	-	-	ns	Figure 2.104
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 2.105
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	

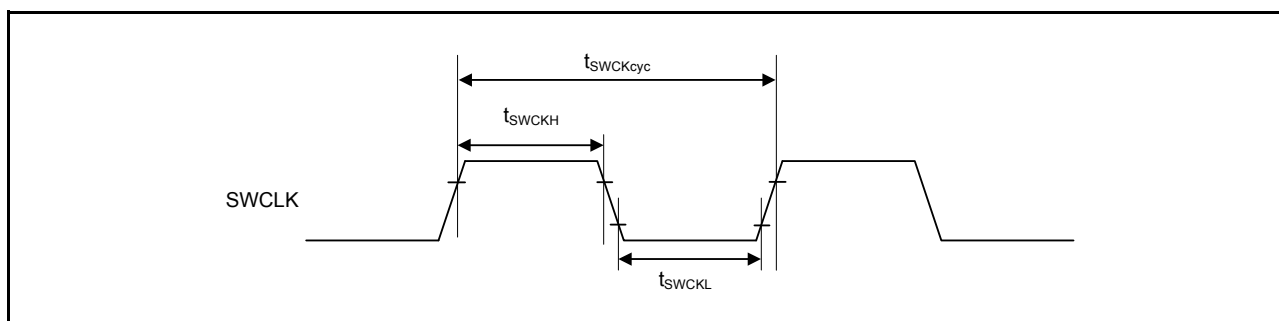


Figure 2.104 SWD SWCLK timing

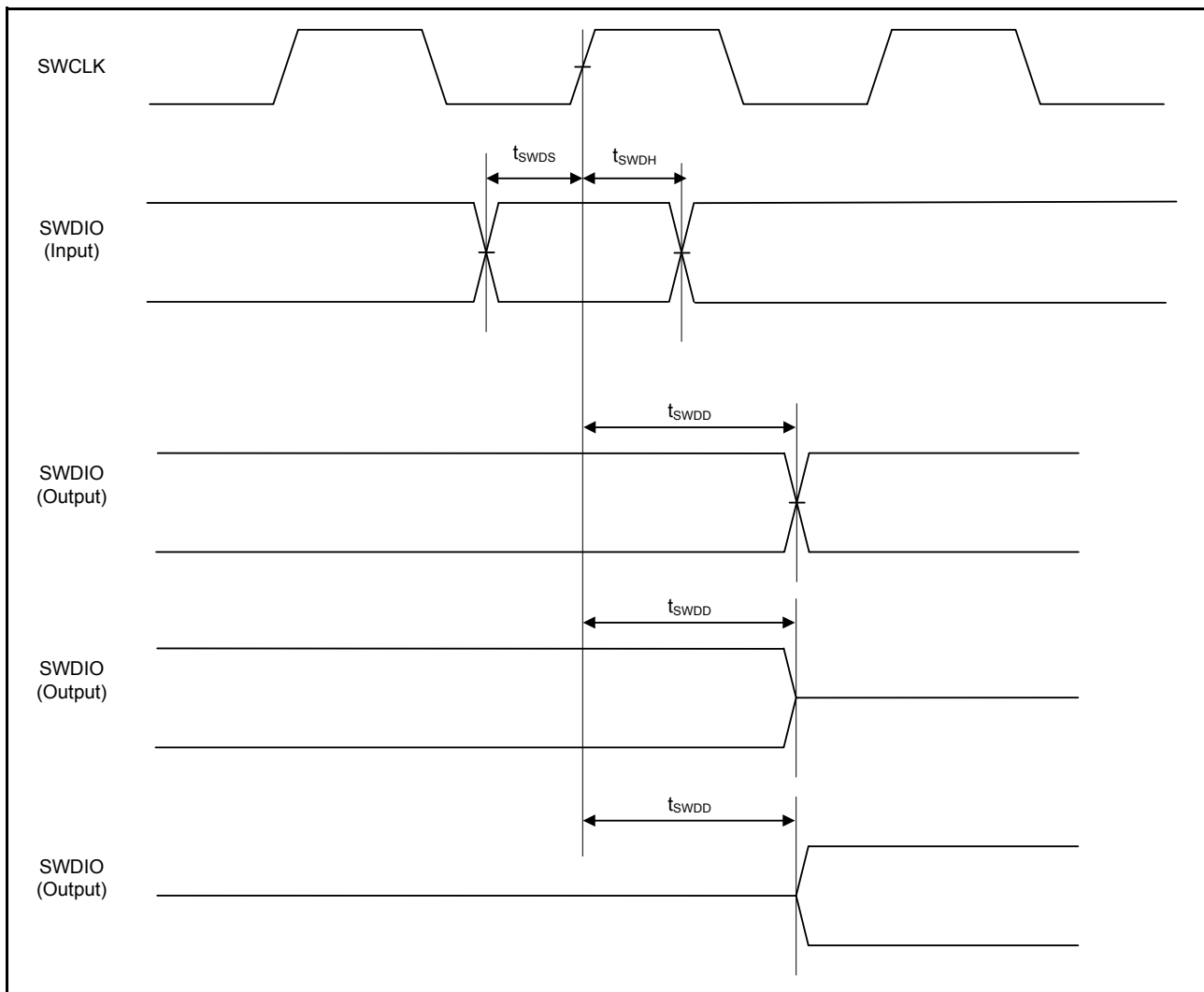


Figure 2.105 SWD input/output timing

2.18 Embedded Trace Macro Interface (ETM)

Table 2.58 ETM

Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 2.106
TCLK clock high pulse width	t_{TCLKH}	13.6	-	-	ns	
TCLK clock low pulse width	t_{TCLKL}	13.6	-	-	ns	
TCLK clock rise time	t_{TCLKr}	-	-	3	ns	
TCLK clock fall time	t_{TCLKf}	-	-	3	ns	
TDATA[3:0] output setup time	t_{TRDS}	3.5	-	-	ns	Figure 2.107
TDATA[3:0] output hold time	t_{TRDH}	2.5	-	-	ns	

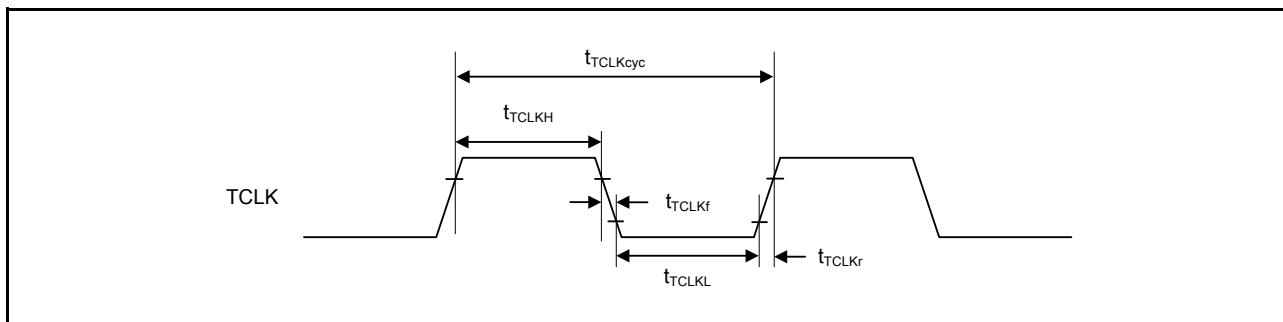


Figure 2.106 ETM TCLK timing

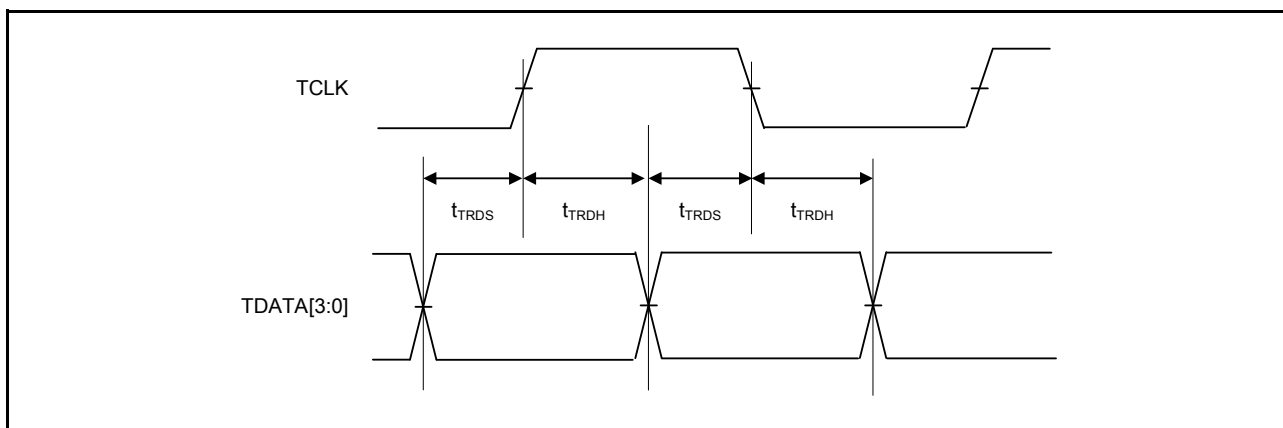


Figure 2.107 ETM output timing

Appendix 1.Package Dimensions

For information on the latest version of the package dimensions or mountings, go to “Packages” on the Renesas Electronics Corporation website.

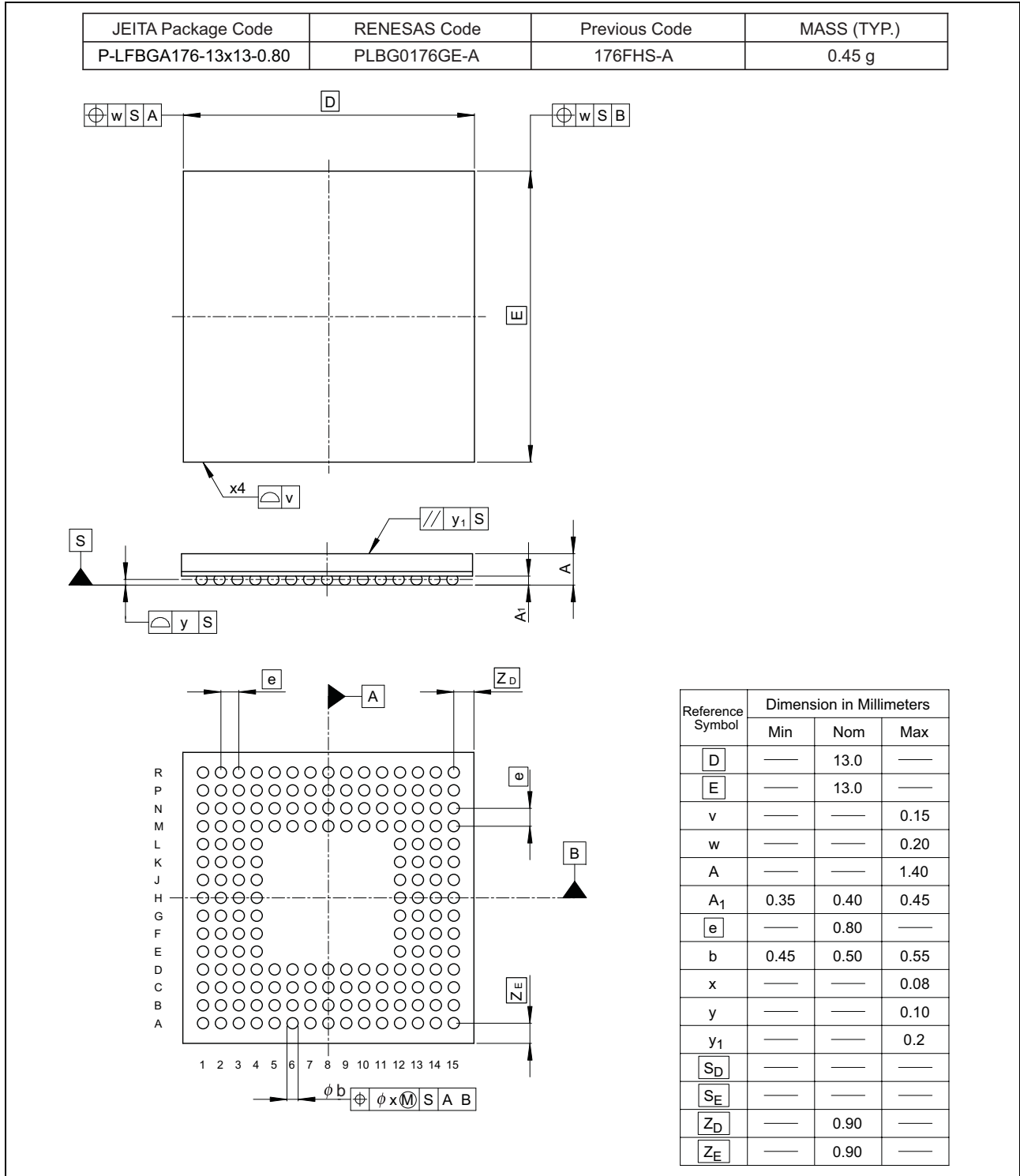


Figure 1.1 176-pin BGA

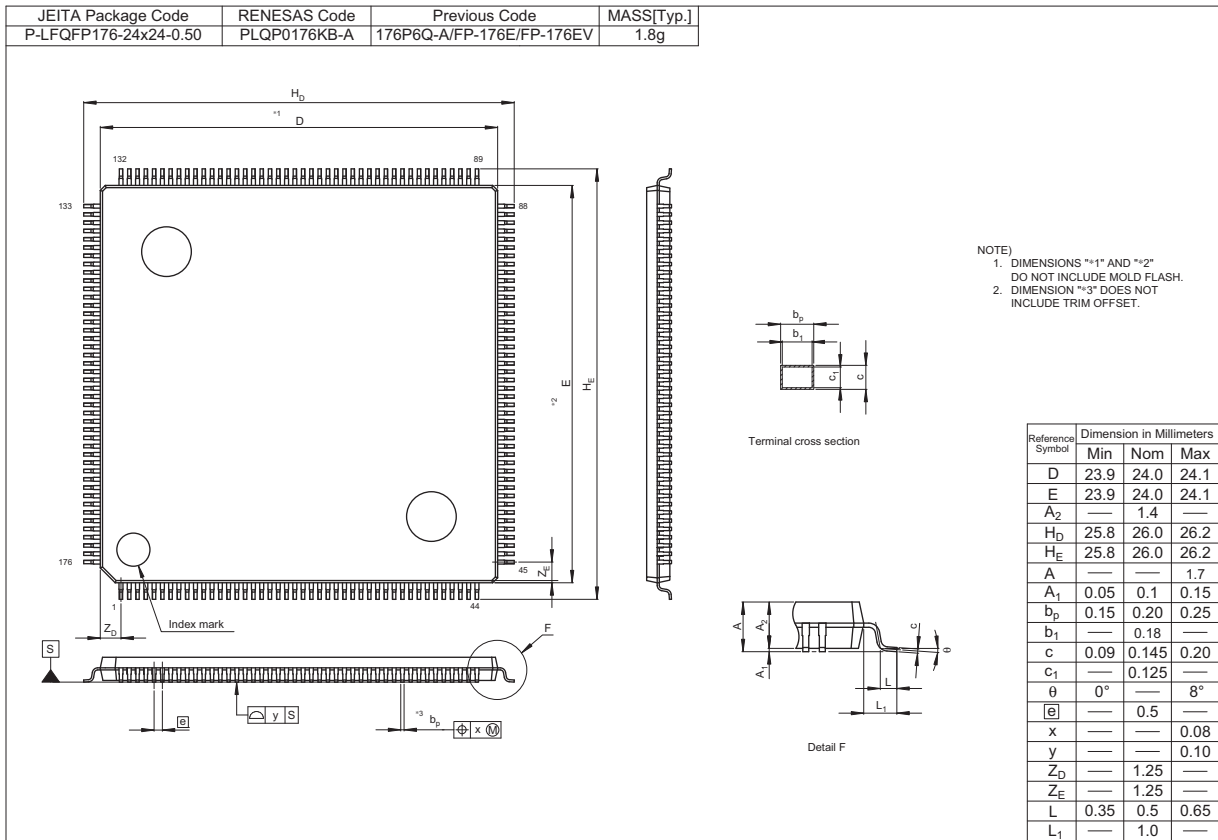


Figure 1.2 176-pin LQFP

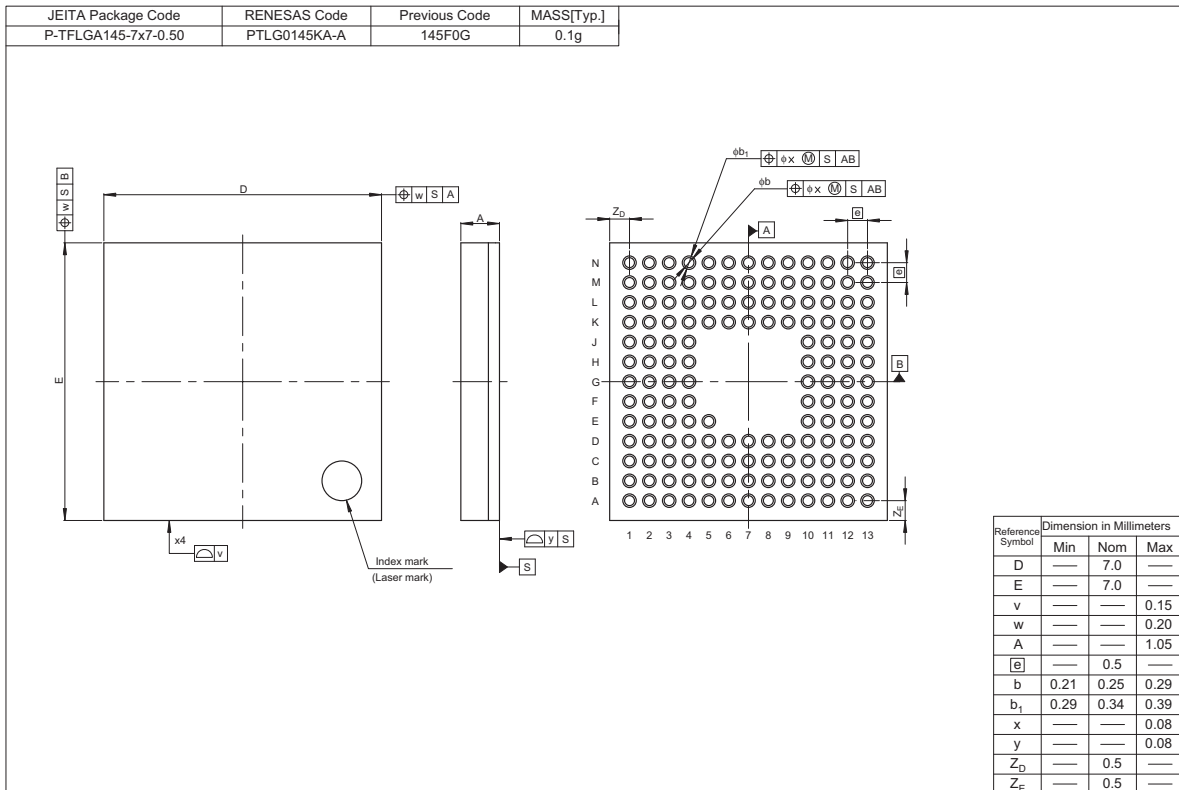


Figure 1.3 145-pin LGA

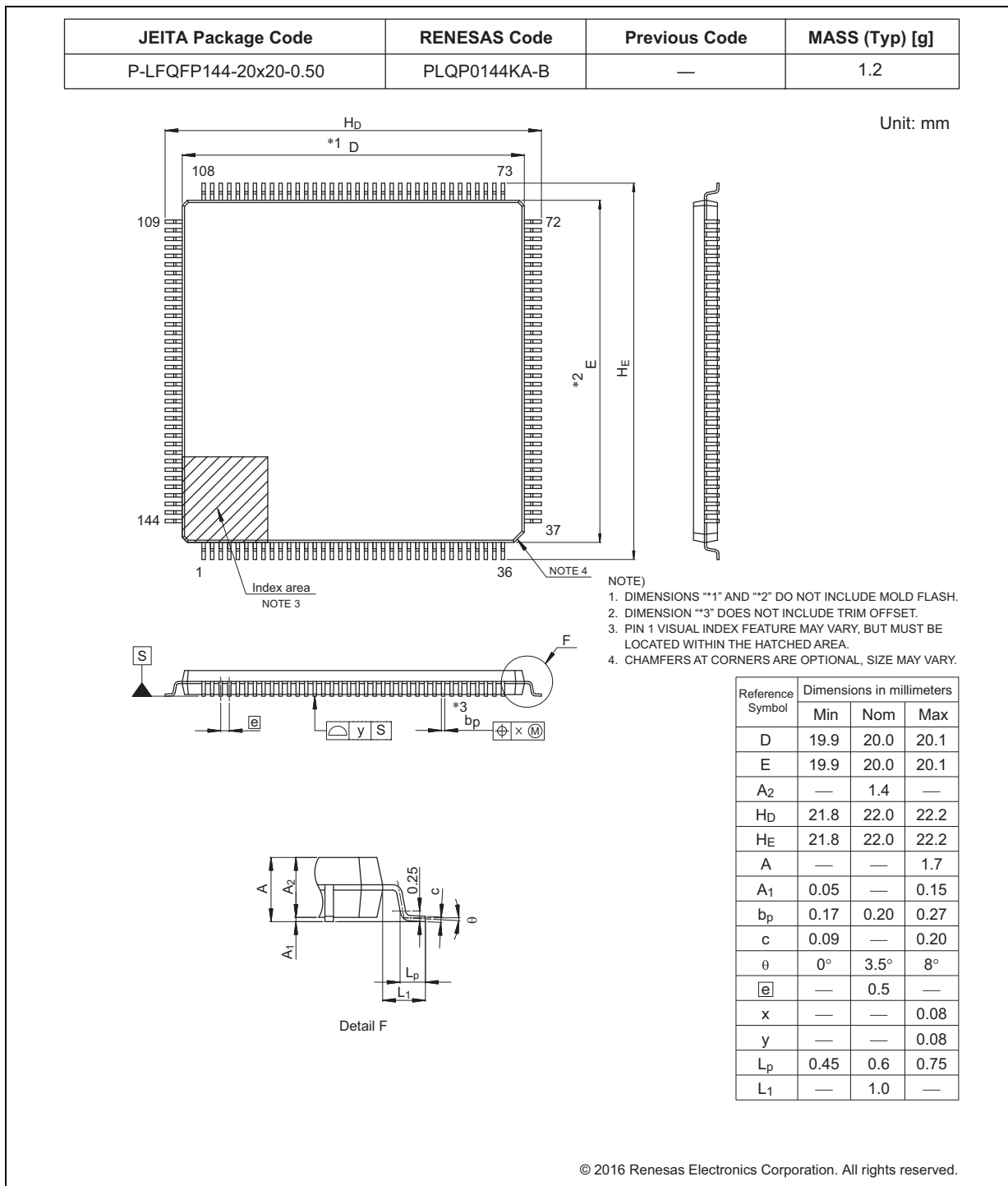
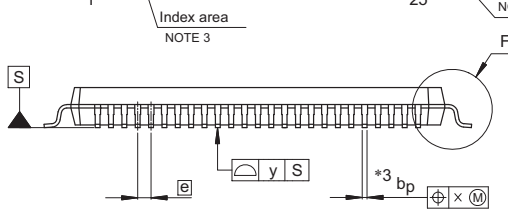
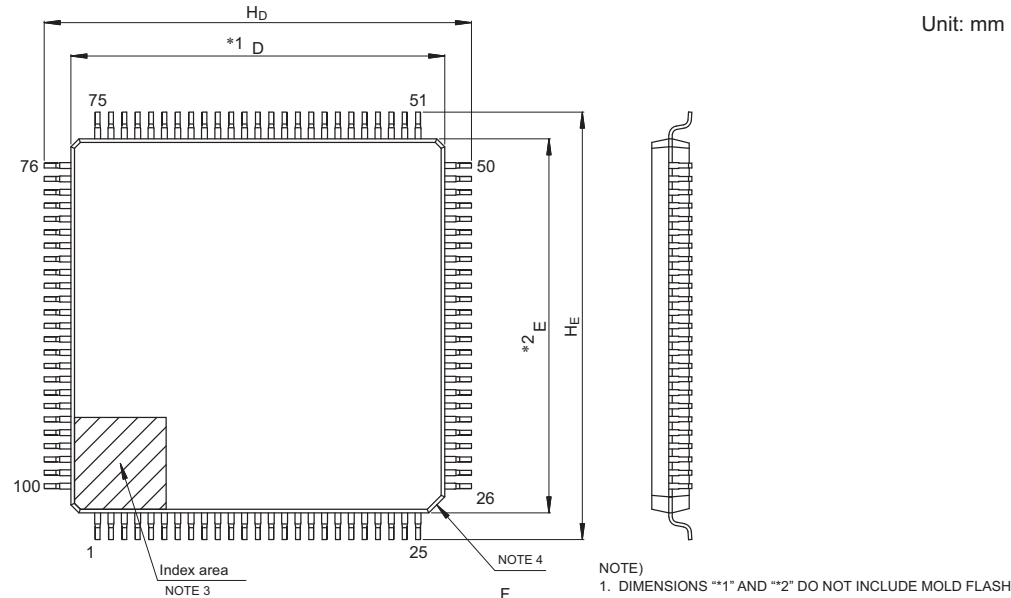


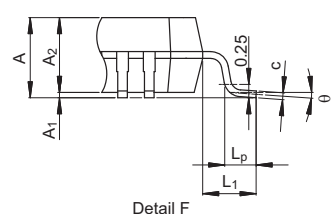
Figure 1.4 144-pin LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6



- NOTE)
1. DIMENSIONS **1" AND **2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—



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Figure 1.5 100-pin LQFP

Revision History	S5D9 Microcontroller Datasheet
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Rev.	Date	Chapter	Summary
1.00	Nov 3, 2016	—	First Edition issued

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S5D9 Microcontroller Datasheet

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