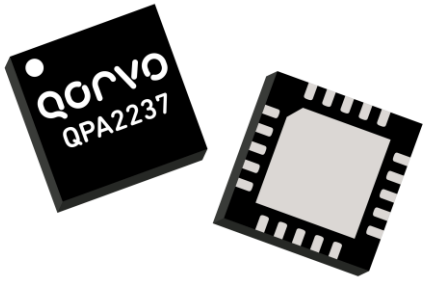
QPA2237

0.03 – 2.5 GHz 10 W GaN Power Amplifier

Applications

- Commercial and military radar
- Communications
- Electronic Warfare

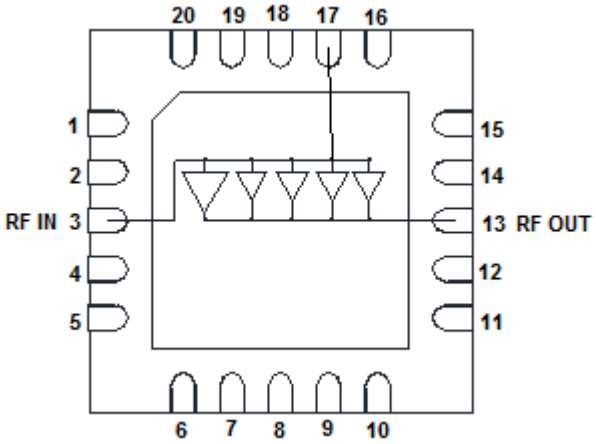


QFN 4x4 mm 20L

Product Features

- Frequency Range: 0.03 – 2.5 GHz
- P_{SAT}: >40 dBm at P_{IN} = 27 dBm
- PAE: >48%
- Large Signal Gain: >13 dB
- Small Signal Gain: >18.5 dB
- Input Return Loss: >9 dB
- Output Return Loss: >9.5 dB
- Bias: V_D = 32 V, I_{DQ} = 360 mA, V_G = -2.1 V Typical
- Wideband Flat Power
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Functional Block Diagram



General Description

Qorvo's QPA2237 is a wideband amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. The QPA2237 operates from 0.03 – 2.5 GHz and provides greater than 10W of saturated output power with greater than 13 dB of large signal gain and greater than 48% power-added efficiency.

The QPA2237 is available in a low-cost, surface-mount, 20 lead, 4x4 OVM QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The QPA2237 is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1, 2, 4 – 12, 14 – 16, 18 – 20	N/C
3	RF IN
13	RF OUT, V_D
17	V_G

Ordering Information

Part	ECCN	Description
QPA2237	EAR99	0.03 – 2.5 GHz 10 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_D)	1.2 A
Gate Current (I_G)	See plot on page 3
Power Dissipation (P_{DISS}), 85°C	19 W
Input Power (P_{IN}), CW, 50 Ω, 85°C	33 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 32V, 85°C	33 dBm
Max VSWR, CW, P_{IN} = 27dBm, V_D = 32V, 85°C (Load)	10:1
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	260°C
Storage Temperature	-55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	32 V
Drain Current (I_{DQ})	360 mA
Gate Voltage (V_G)	-2.1 V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25^{0}C, V_D = 32 V, I_{DQ} = 360 mA, V_G = -2.1 V Typical

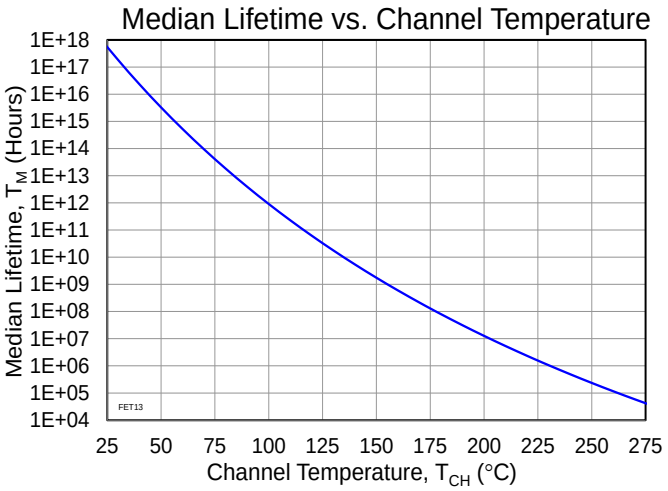
Parameter	Min	Typical	Max	Units
Operational Frequency Range	0.03		2.5	GHz
Small Signal Gain		> 18.5		dB
Input Return Loss		> 9		dB
Output Return Loss		> 9.5		dB
Output Power (Pin = 27 dBm)		> 40		dBm
Power Added Efficiency (Pin = 27 dBm)		> 48		%
Small Signal Gain Temperature Coefficient		-0.017		dB/°C
Output Power Temperature Coefficient		-0.004		dBm/°C
Recommended Operating Voltage:		32	36	V

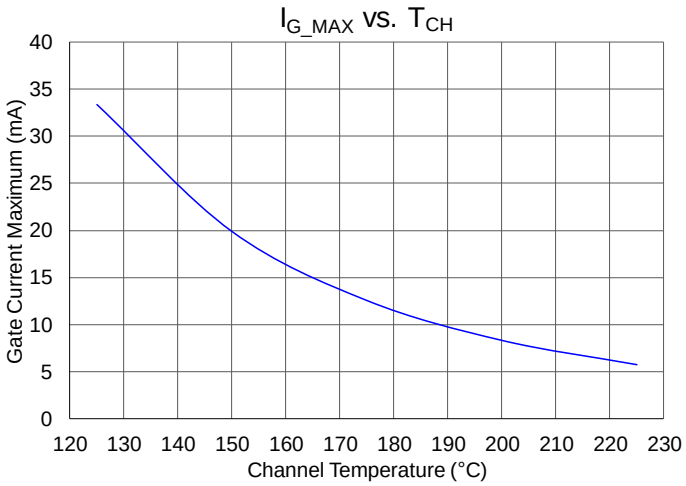
Thermal and Reliability Information

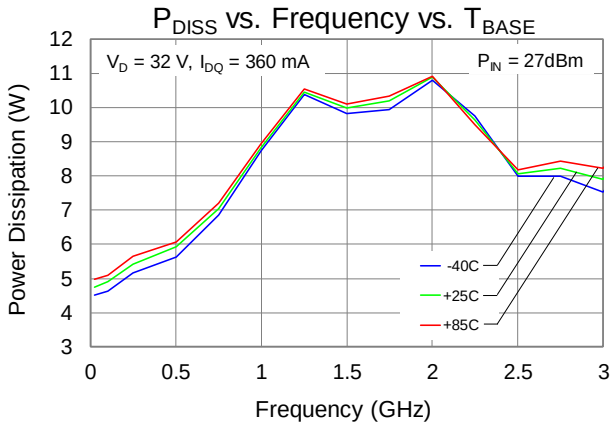
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 32 V	7.8	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	I_{DQ} = 360 mA, $I_{D\ Drive}$ = 648 mA	173	°C
Median Lifetime (T_M)	Freq. = 2.0 GHz: P_{IN} = 27 dBm, P_{OUT} = 40 dBm, P_{DISS} = 10.9 W	1.58 x 10^8	Hrs

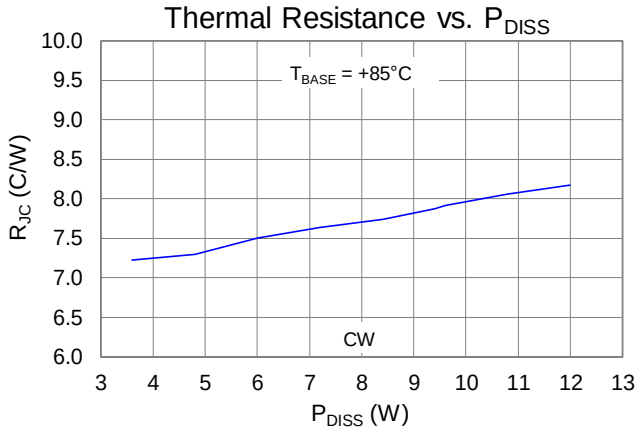
Notes:
1. Thermal resistance measured to back of package.

Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in I_{D_MAX}





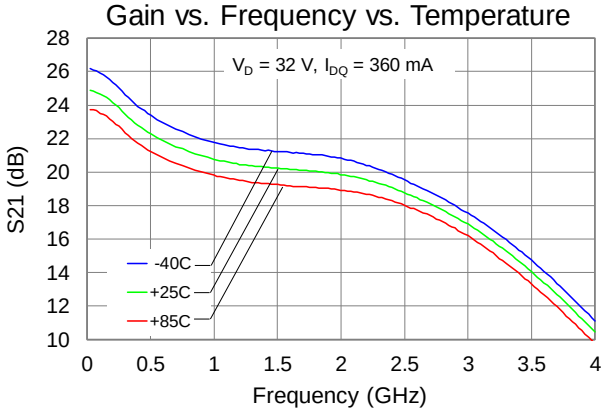




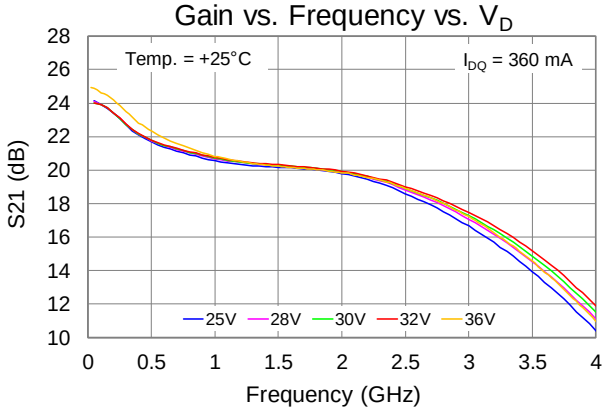
Typical Performance: Small Signal

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

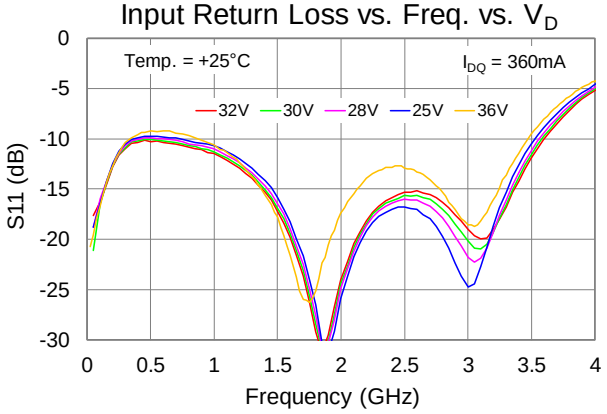
Gain vs. Frequency vs. Temperature



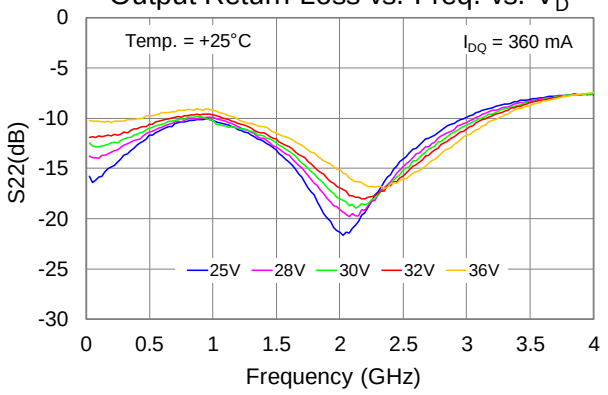
Gain vs. Frequency vs. V_D



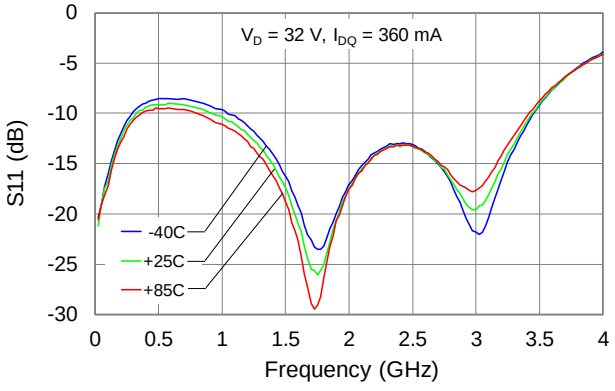
Input Return Loss vs. Freq. vs. V_D



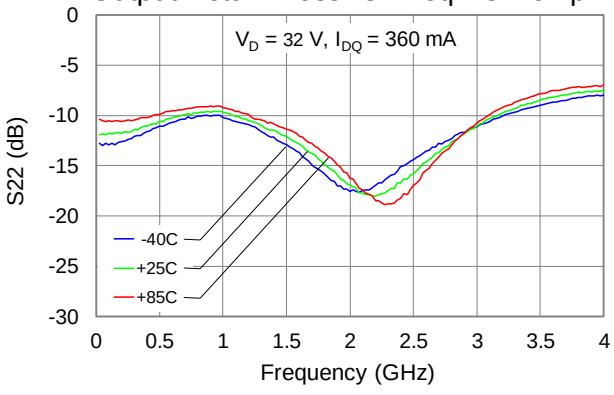
Output Return Loss vs. Freq. vs. V_D



Input Return Loss vs. Freq. vs. Temp.



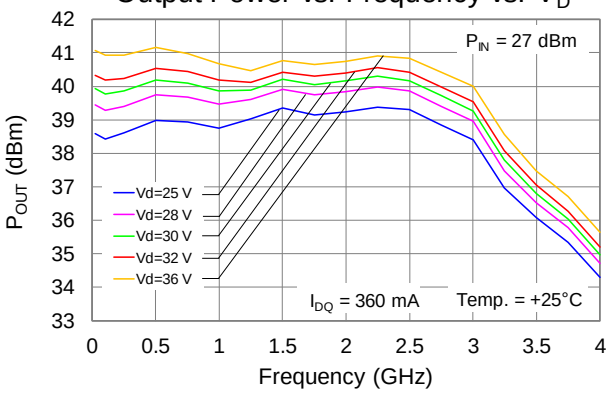
Output Return Loss vs. Freq. vs. Temp.



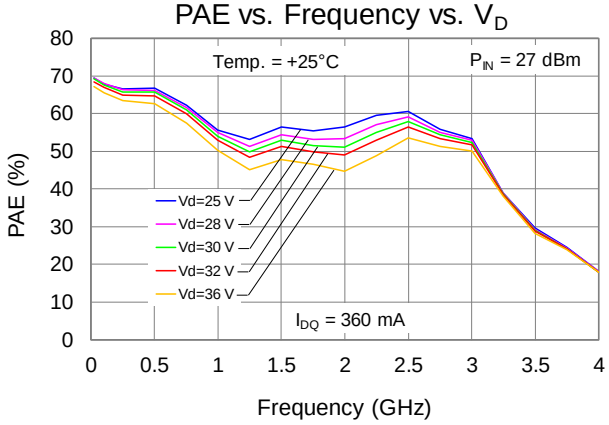
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

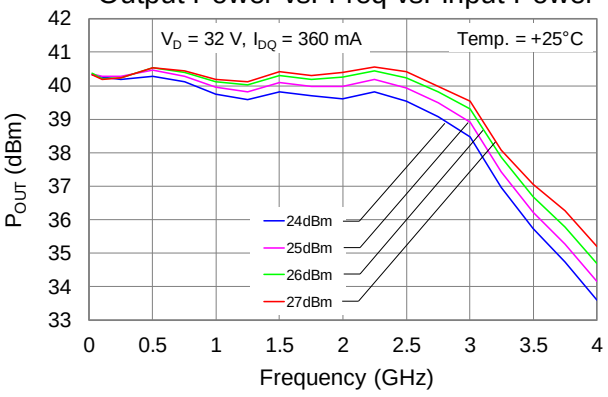
Output Power vs. Frequency vs. V_D



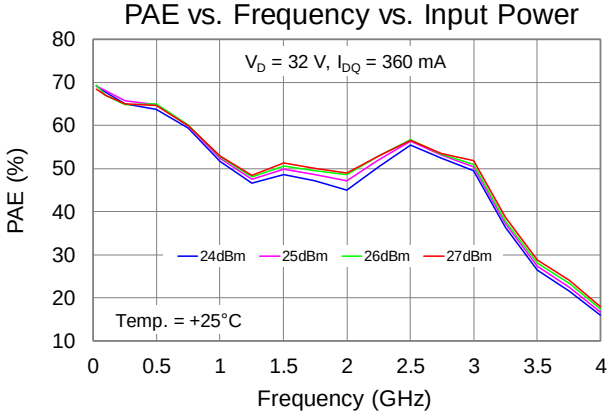
PAE vs. Frequency vs. V_D



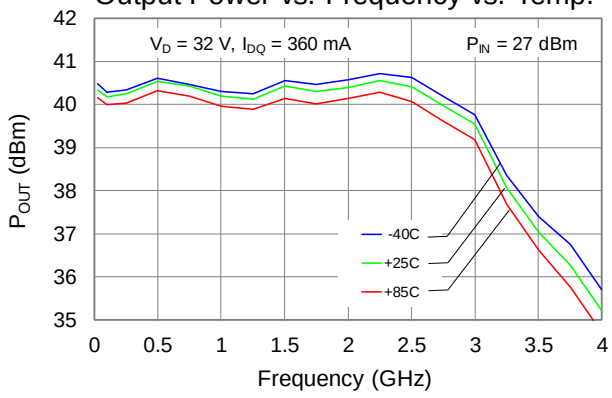
Output Power vs. Freq vs. Input Power



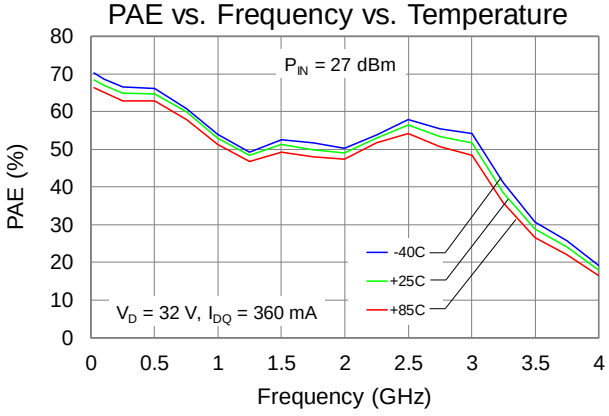
PAE vs. Frequency vs. Input Power



Output Power vs. Frequency vs. Temp.



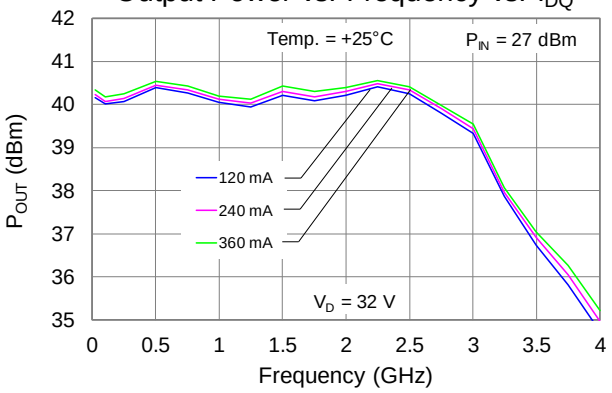
PAE vs. Frequency vs. Temperature



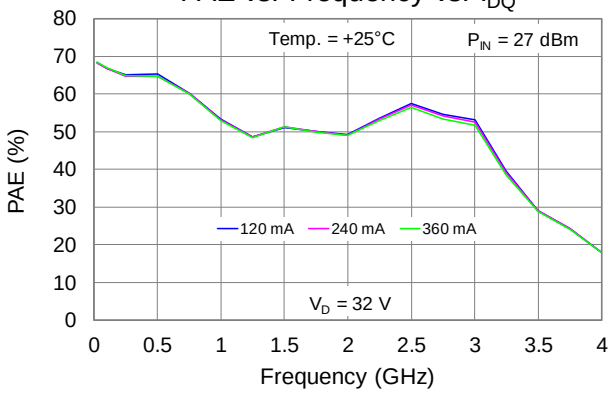
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

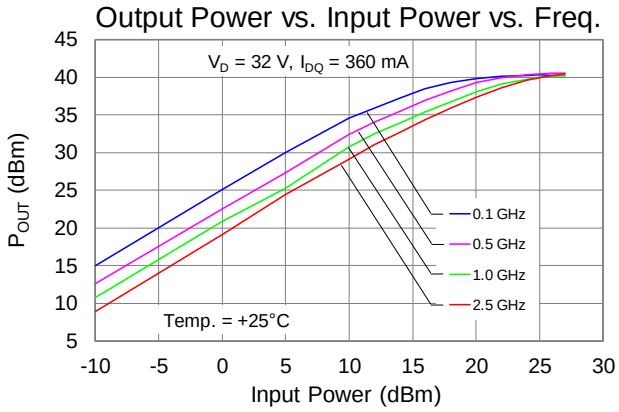
Output Power vs. Frequency vs. I_{DQ}



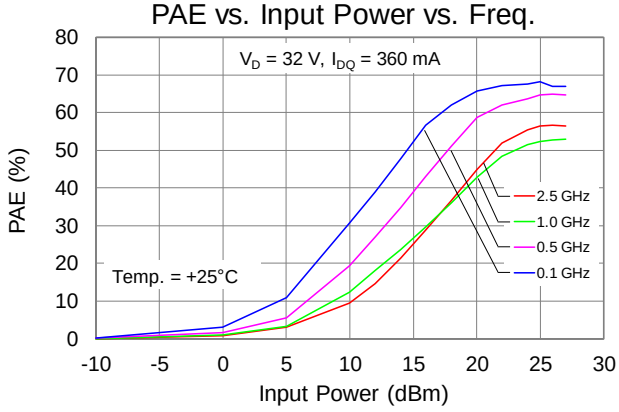
PAE vs. Frequency vs. I_{DQ}



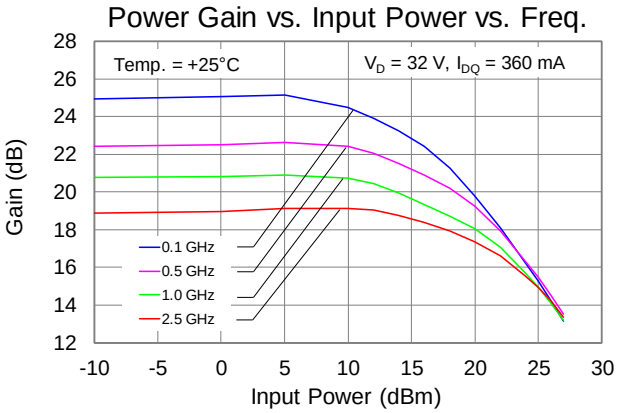
Output Power vs. Input Power vs. Freq.



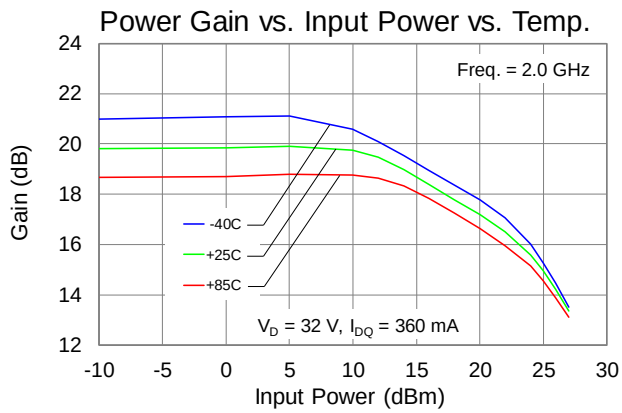
PAE vs. Input Power vs. Freq.



Power Gain vs. Input Power vs. Freq.



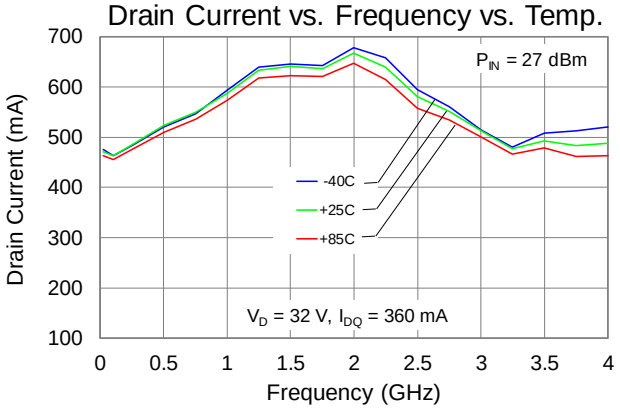
Power Gain vs. Input Power vs. Temp.



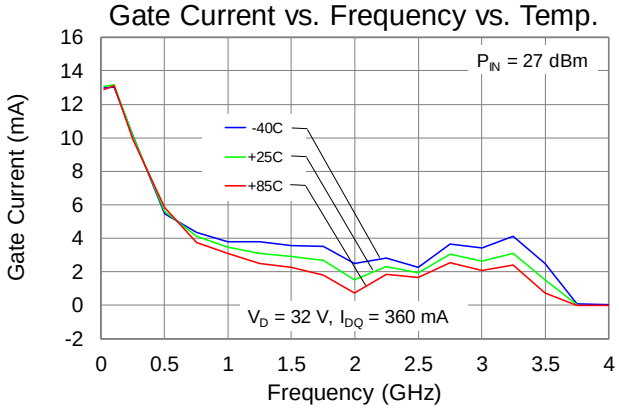
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

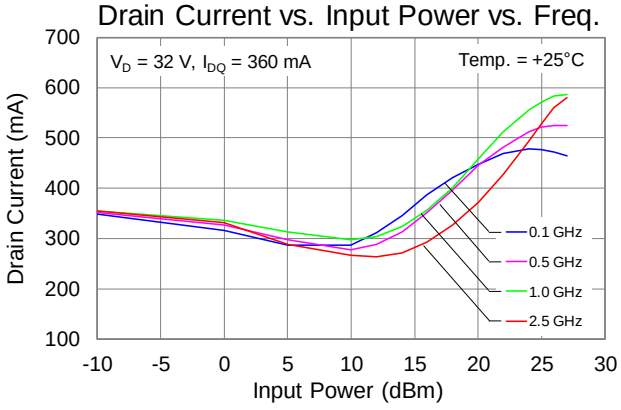
Drain Current vs. Frequency vs. Temp.



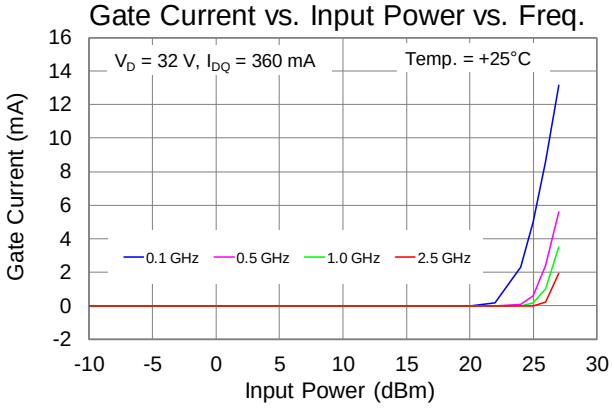
Gate Current vs. Frequency vs. Temp.



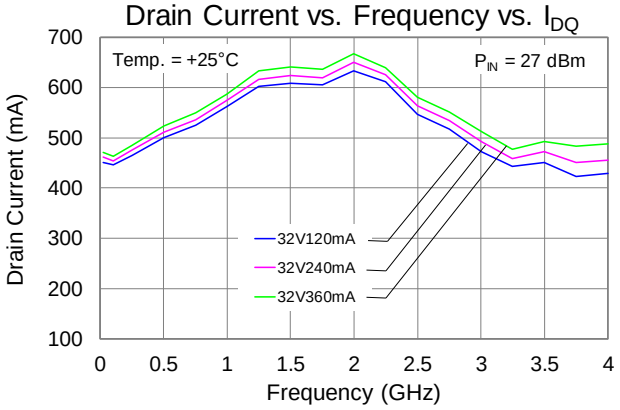
Drain Current vs. Input Power vs. Freq.



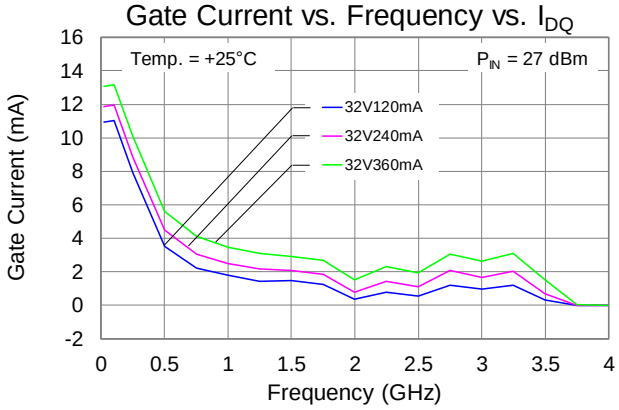
Gate Current vs. Input Power vs. Freq.



Drain Current vs. Frequency vs. I_{DQ}



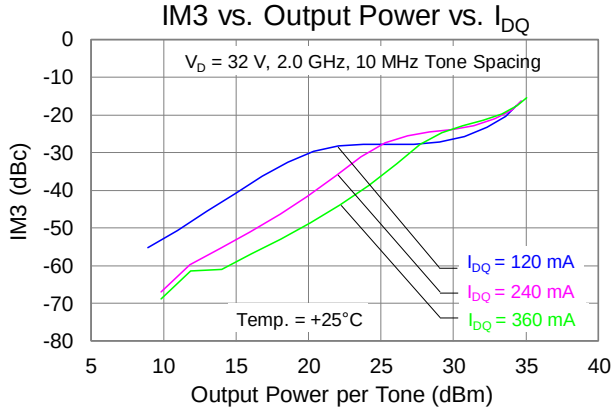
Gate Current vs. Frequency vs. I_{DQ}



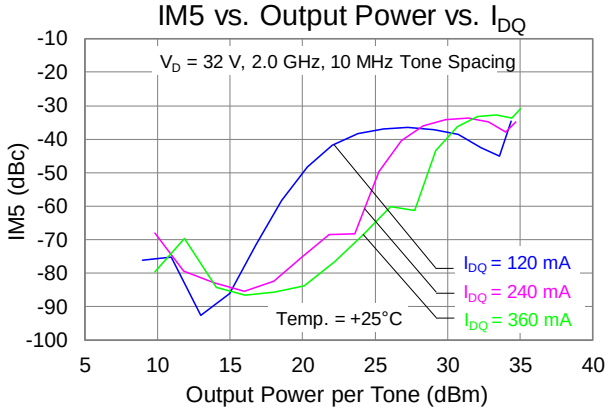
Typical Performance: Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

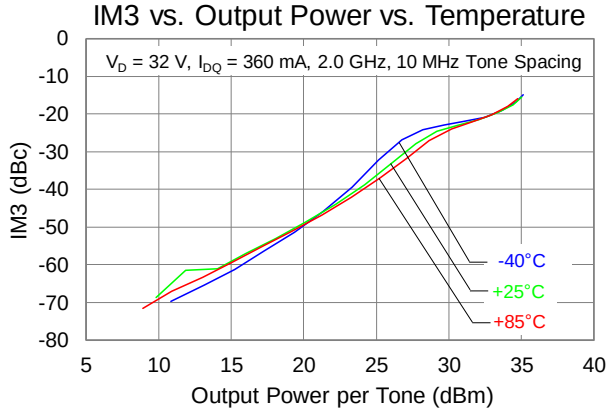
IM3 vs. Output Power vs. I_{DQ}



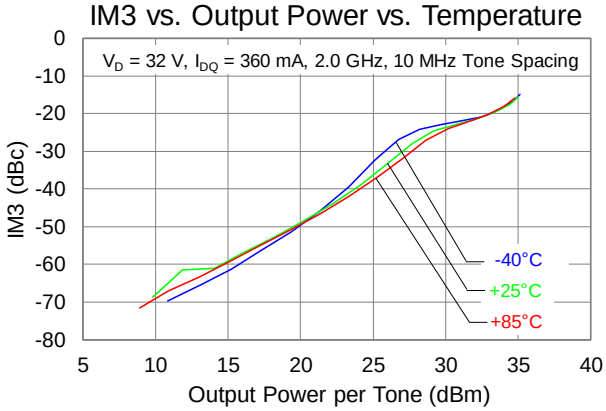
IM5 vs. Output Power vs. I_{DQ}



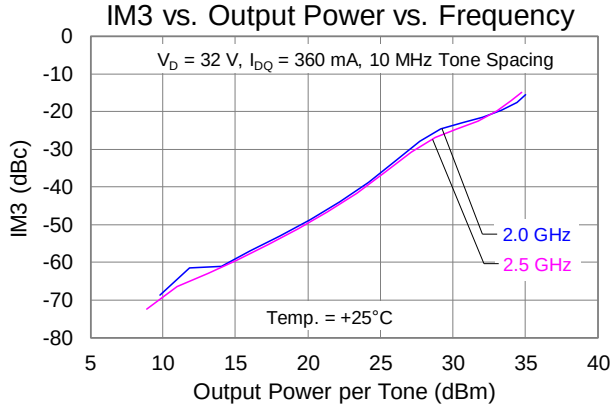
IM3 vs. Output Power vs. Temperature



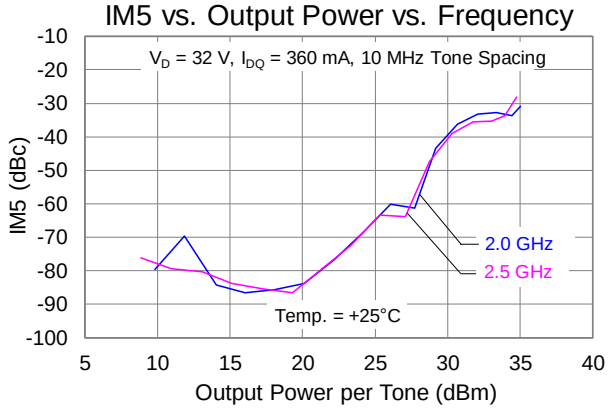
IM3 vs. Output Power vs. Temperature



IM3 vs. Output Power vs. Frequency

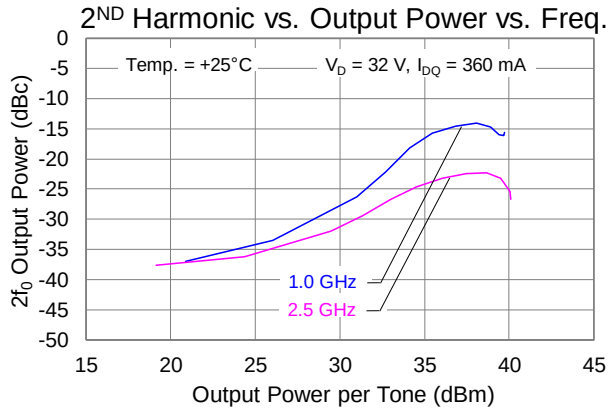


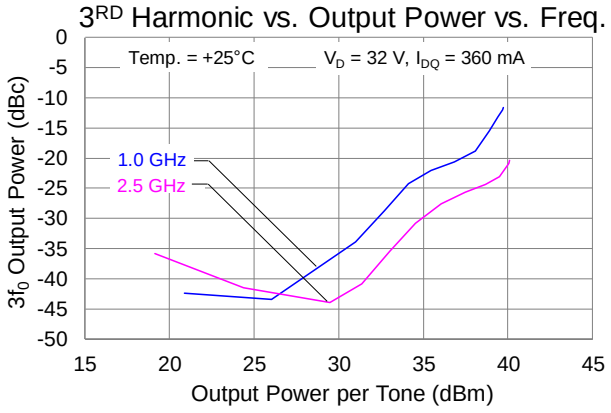
IM5 vs. Output Power vs. Frequency

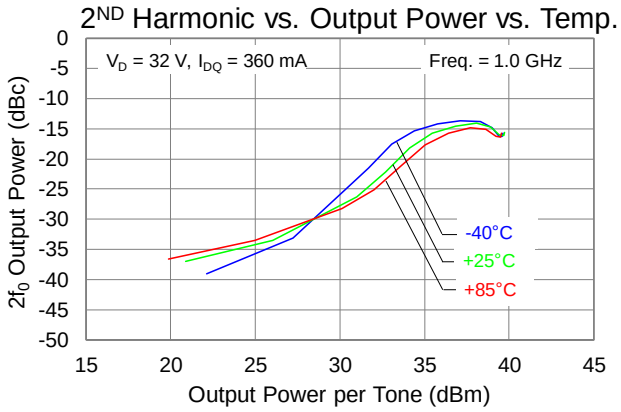


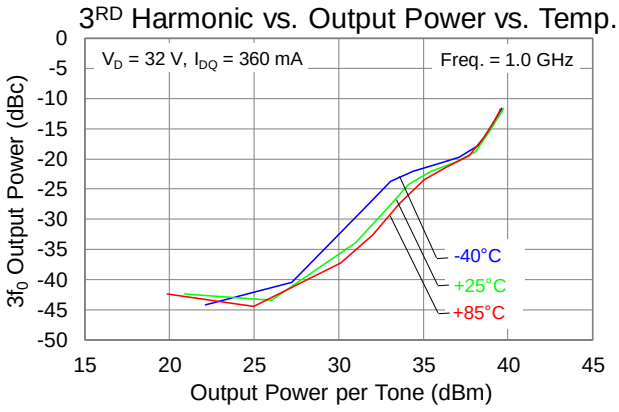
Typical Performance: Linearity

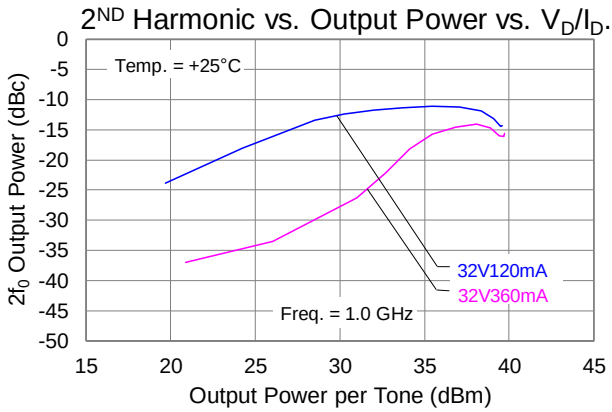
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

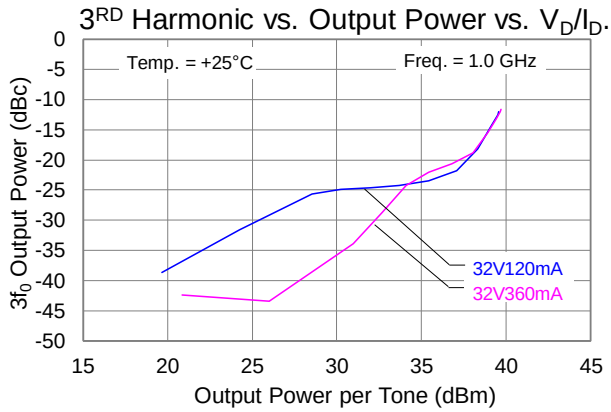






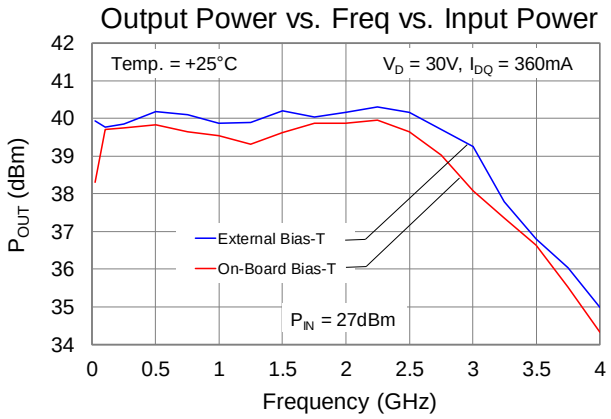


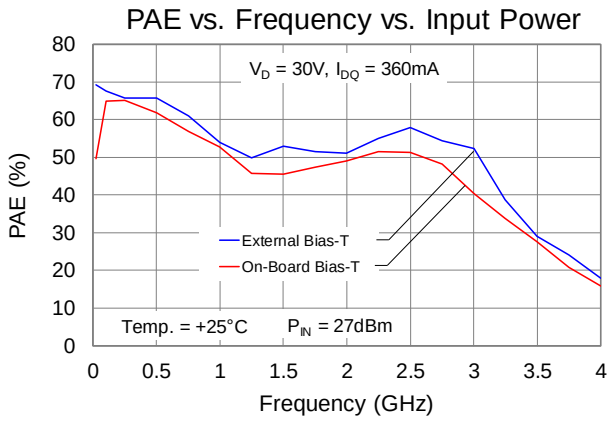




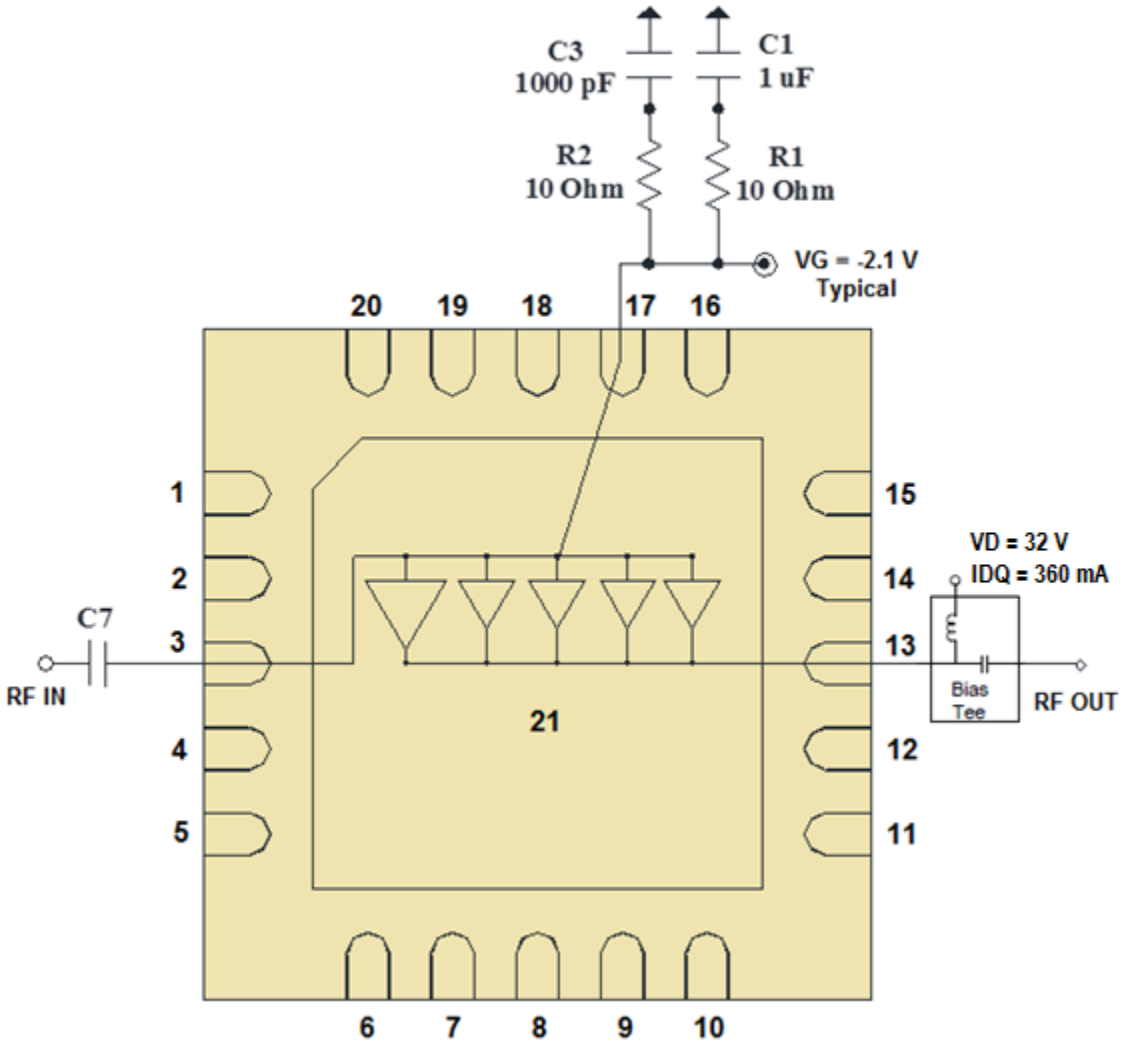
Typical Performance: Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 11 and 13)





Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. Coaxial input DC block (C7) is used for input port (RF In.)
2. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee.

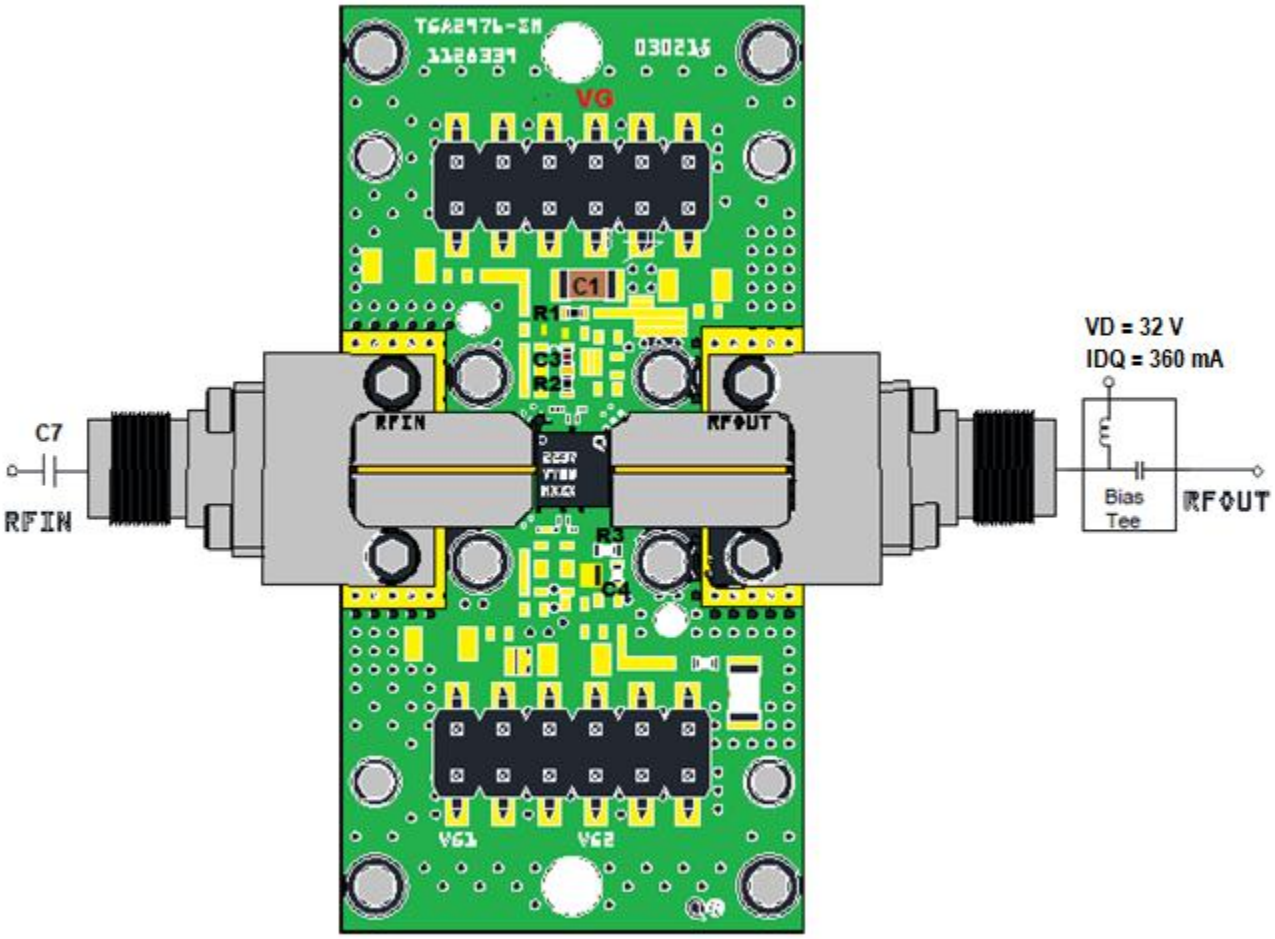
Bias-up Procedure

1. Set I_D limit to 700mA, I_G limit to 15mA
2. Set V_G to -5.0V
3. Set V_D +32V
4. Adjust V_G more positive until I_{DQ} = 360mA (V_G ~ -2.1V Typical)
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

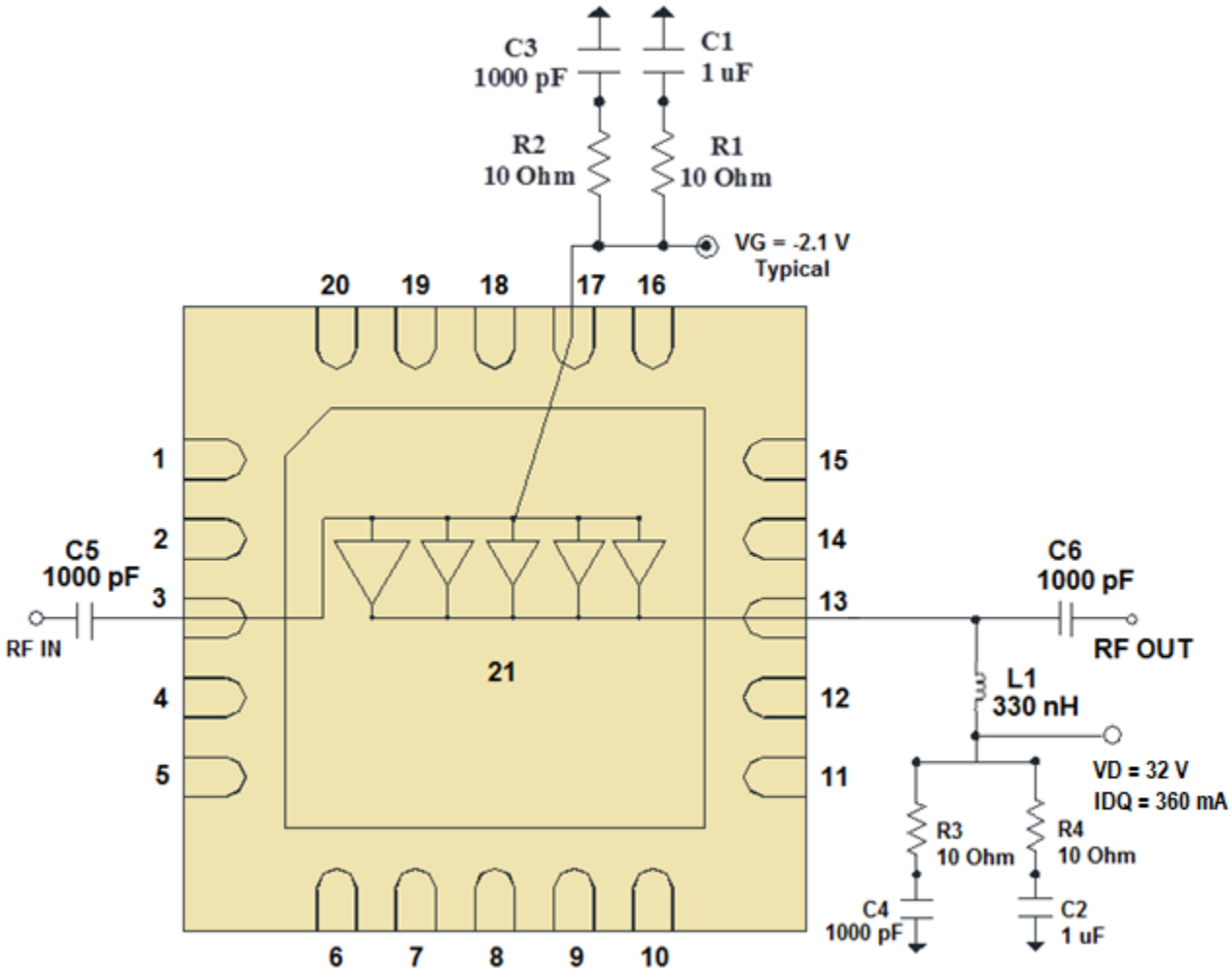
Assembly Drawing (Coaxial input DC block and coaxial output bias tee)



Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1	1 uF	Cap, 1206, 50V, 5%, X7R	Various	
C3	1000 pF	Cap, 0402, 100V, 10%, X7R	Various	
C7		DC Block	Various	
R1 – R2	10Ω	Res, 0402, 5%, SMD	Various	

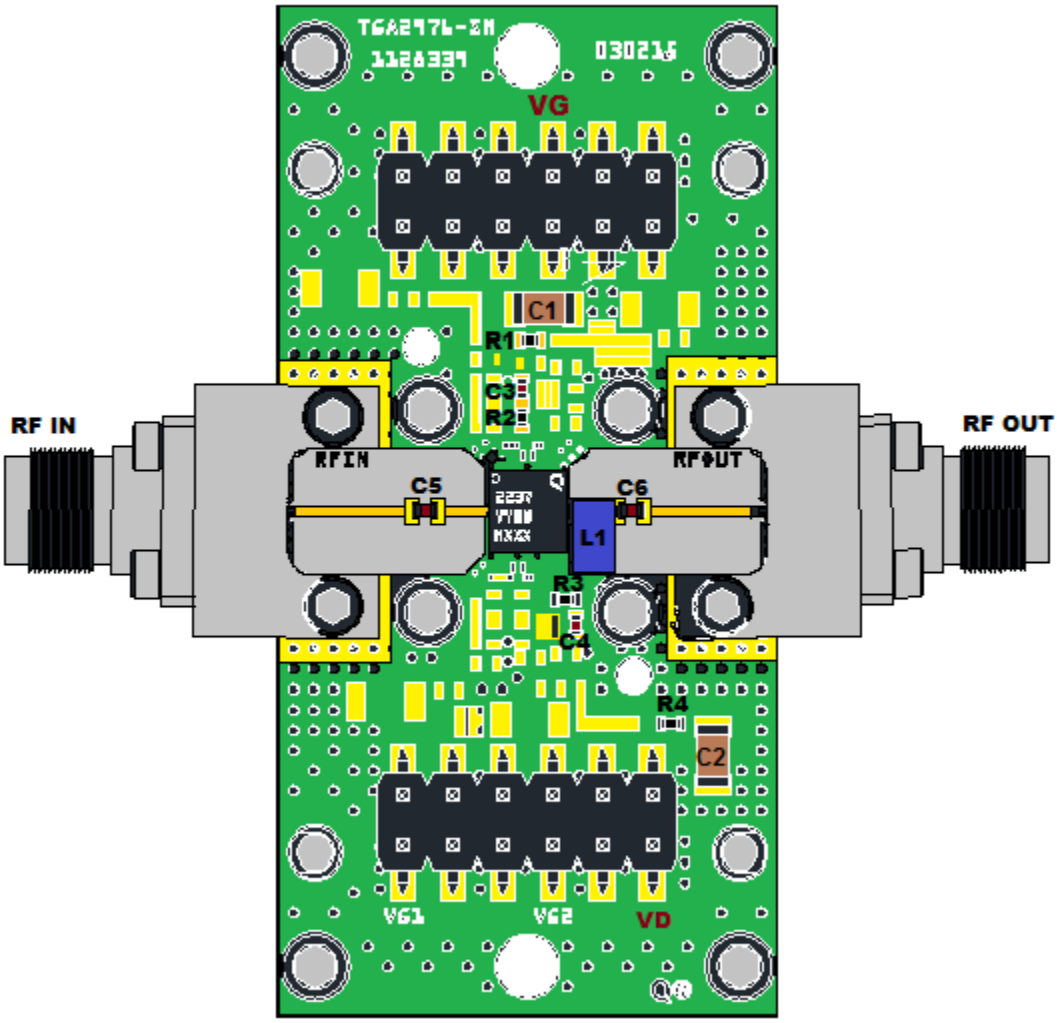
Application Circuit (Option with board-level DC blocks and output bias tee)



Notes:

1. Performance of the DUT with surface-mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.

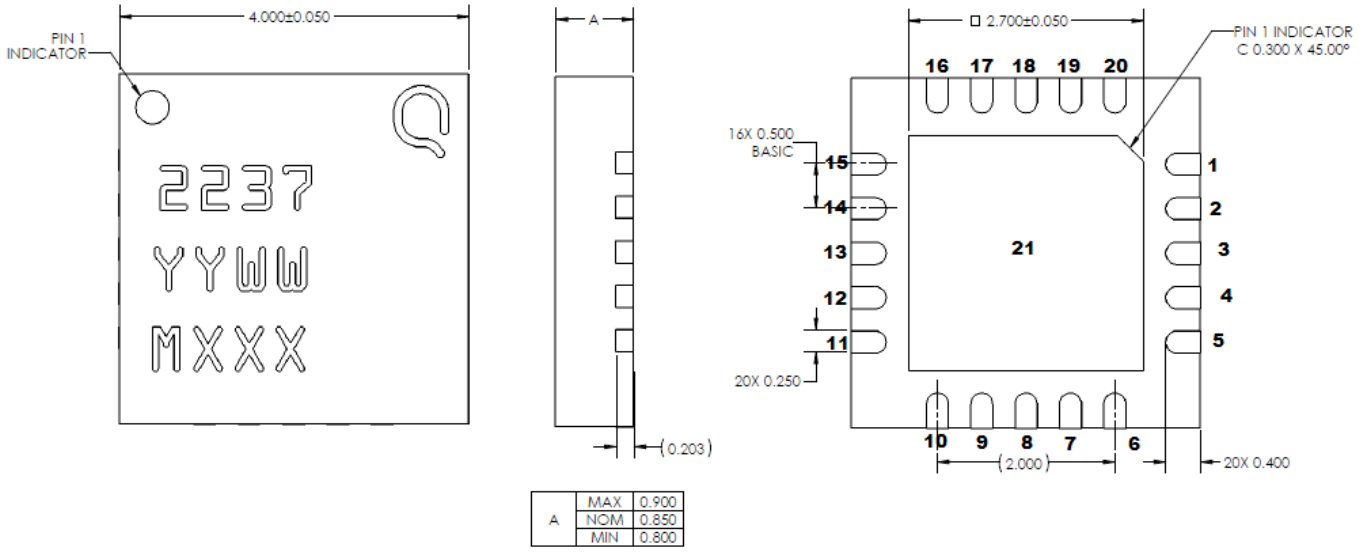
Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option



Bill of Materials For On-Board Bias-Tee

Reference Design	Value	Description	Manufacturer	Part Number
C1, C2	1 uF	Cap, 1206, 50V, 5%, X7R	Various	
C3 – C6	1000 pF	Cap, 0402, 100V, 10%, X7R	Various	
L1	330nH	Ind, 1206, 850mA	Various	
R1 – R4	10Ω	Res, 0402, 5%, SMD	Various	

Mechanical Drawing and Pin Description



A		
	MAX	0.900
	NOM	0.850
	MIN	0.800

UNITS: inches
TOLERANCES: unless specified
x.xx = ± 0.01
x.xxx = ± 0.005
PACKAGE LEADS ARE GOLD PLATED
PART IS MOLD ENCAPSULATED
PART MARKING:
2237: Part number
YY: Part Assembly year
WW: Part Assembly weak
MXXX: Batch ID

Pin Description

Pin No.	Symbol	Description
1, 2, 4 – 12, 14 – 16, 18 – 20	N/C	No connection
3	RF IN	Input; matched to 50 Ω.
13	RF OUT/V_D	Output; matched to 50 Ω.
17	V_G	GATE voltage; bias network is required; see recommended Application Information on page 11
21	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Recommended Soldering Temperature Profile