

N-Channel Power MOSFET (8A, 800Volts)

DESCRIPTION

The Nell **8N80** is a three-terminal silicon device with current conduction capability of 8A, fast switching speed, low on-state resistance, breakdown voltage rating of 800V, and max. threshold voltage of 5 volts.

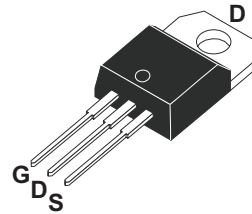
They are designed for use in applications, such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits, and general purpose switching applications.

FEATURES

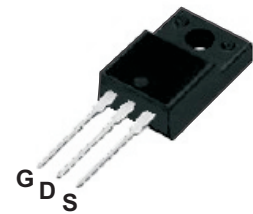
- $R_{DS(ON)} = 1.55\Omega @ V_{GS} = 10V$
- Ultra low gate charge(35nC max.)
- Low reverse transfer capacitance ($C_{RSS} = 13pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature

PRODUCT SUMMARY

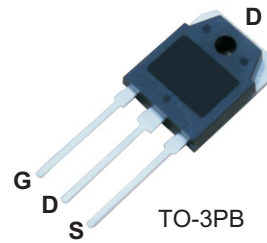
I_D (A)	8
V_{DSS} (V)	800
$R_{DS(ON)}$ (Ω)	1.55 @ $V_{GS} = 10V$
Q_G (nC) max.	35



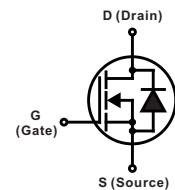
TO-220AB
(8N80A)



TO-220F
(8N80AF)



TO-3PB
(8N80B)



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage	$T_J = 25^\circ C$ to $150^\circ C$	800	V
V_{DGR}	Drain to Gate voltage	$R_{GS} = 20K\Omega$	800	
V_{GS}	Gate to Source voltage		± 30	
I_D	Continuous Drain Current	$T_C = 25^\circ C$	8	A
		$T_C = 100^\circ C$	5.1	
I_{DM}	Pulsed Drain current(Note 1)		32	
I_{AR}	Avalanche current(Note 1)		8	
E_{AR}	Repetitive avalanche energy(Note 1)	$I_{AR} = 8A, R_{GS} = 50\Omega, V_{GS} = 10V$	17.8	mJ
E_{AS}	Single pulse avalanche energy(Note 2)	$I_{AS} = 8A, L = 25mH$	850	
dv/dt	Peak diode recovery dv/dt(Note 3)		4.5	V/ns
P_D	Total power dissipation (Derate above $25^\circ C$)	$T_C = 25^\circ C$	TO-3PB: 220 (1.75)	W($W/^\circ C$)
			TO-220AB: 178 (1.43)	
			TO-220F: 59 (0.48)	
T_J	Operation junction temperature		-55 to 150	$^\circ C$
T_{STG}	Storage temperature		-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf·in (N·m)

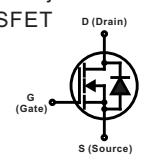
Note: 1. Repetitive rating: pulse width limited by junction temperature..

2. $I_{AS} = 8A, V_{DD} = 50V, L = 25mH, R_{GS} = 25\Omega$, starting $T_J = 25^\circ C$.

3. $I_{SD} \leq 8A, di/dt \leq 200A/\mu s, V_{DD} \leq V_{(BR)DSS}$, starting $T_J = 25^\circ C$.

THERMAL RESISTANCE						
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT	
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-3PB		0.57	°C/W	
		TO-220AB		0.70		
		TO-220F		2.10		
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-3PB		40		
		TO-220AB/TO-220F		62.5		

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
⊙ OFF CHARACTERISTICS						
$V_{(BR)DSS}$	Drain to source breakdown voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	800			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	$I_D = 250\mu\text{A}, V_{DS} = V_{GS}$		0.5		V/°C
I_{DSS}	Drain to source leakage current	$V_{DS} = 800\text{V}, V_{GS} = 0\text{V}$			10	μA
		$V_{DS} = 640\text{V}, V_{GS} = 0\text{V}$			100	
I_{GSS}	Gate to source forward leakage current	$V_{GS} = 30\text{V}, V_{DS} = 0\text{V}$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -30\text{V}, V_{DS} = 0\text{V}$			-100	
⊙ ON CHARACTERISTICS						
$R_{DS(ON)}$	Static drain to source on-state resistance	$I_D = 4\text{A}, V_{GS} = 10\text{V}$		1.29	1.55	Ω
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3		5	V
g_{fs}	Forward transconductance (Note 1)	$V_{DS} = 50\text{V}, I_D = 4\text{A}$		5.6		S
⊙ DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1580	2050	pF
C_{OSS}	Output capacitance		135	175		
C_{RSS}	Reverse transfer capacitance		13	17		
⊙ SWITCHING CHARACTERISTICS						
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 400\text{V}, V_{GS} = 10\text{V}, I_D = 8\text{A}, R_{GS} = 25\Omega$ (Note 1, 2)		40	90	ns
t_r	Rise time		110	250		
$t_{d(OFF)}$	Turn-off delay time		65	140		
t_f	Fall time		70	150		
Q_G	Total gate charge	$V_{DD} = 640\text{V}, V_{GS} = 10\text{V}, I_D = 8\text{A}$ (Note 1, 2)		35	45	nC
Q_{GS}	Gate to source charge		10			
Q_{GD}	Gate to drain charge (Miller charge)		14			

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	$I_{SD} = 8\text{A}, V_{GS} = 0\text{V}$			1.4	V
$I_S (I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			8	A
I_{SM}	Pulsed source current		32			
t_{rr}	Reverse recovery time	$I_{SD} = 8\text{A}, V_{GS} = 0\text{V}, di_F/dt = 100\text{A}/\mu\text{s}$		690		ns
Q_{rr}	Reverse recovery charge			8.2		μC

Note: 1. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
 2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

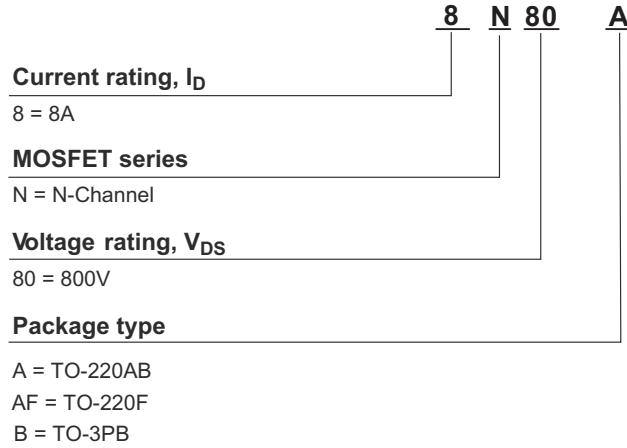


Fig.1 On-State characteristics

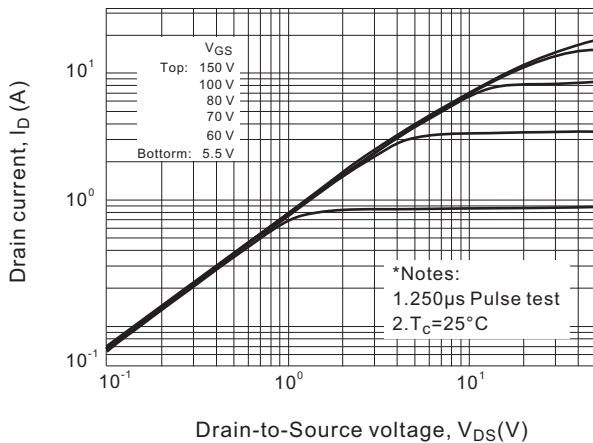


Fig.2 Transfer characteristics

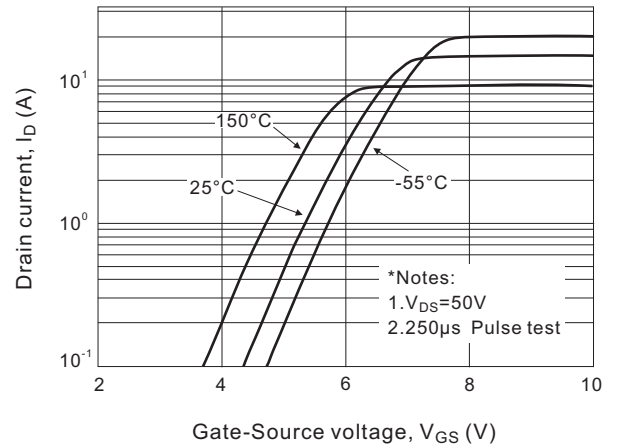


Fig.3 On-resistance variation vs. drain current and gate voltage

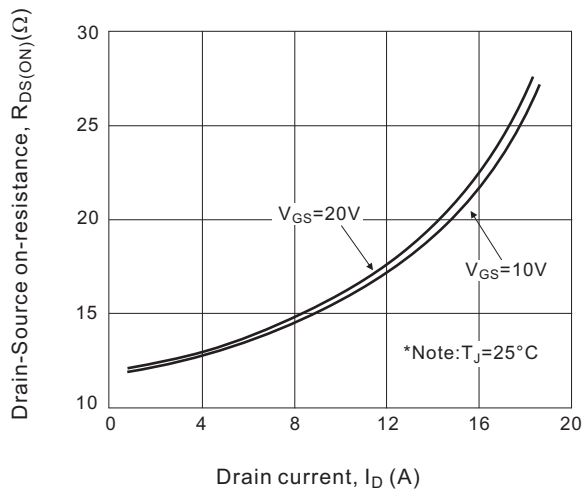


Fig.4 Body diode forward voltage vs. source current

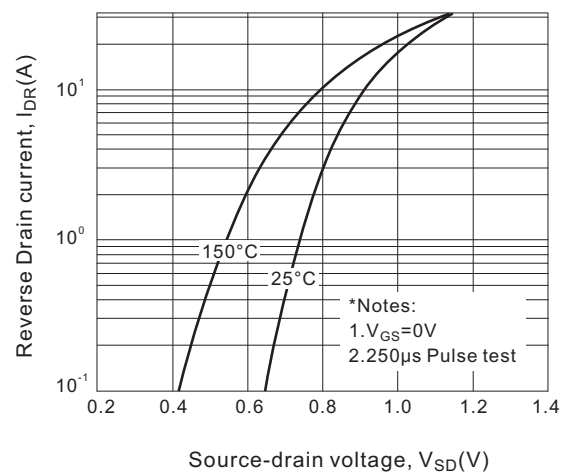


Fig.5 Capacitance characteristics

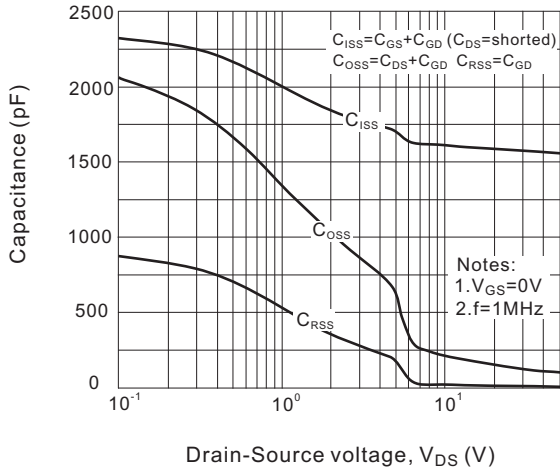


Fig.6 Gate charge characteristics

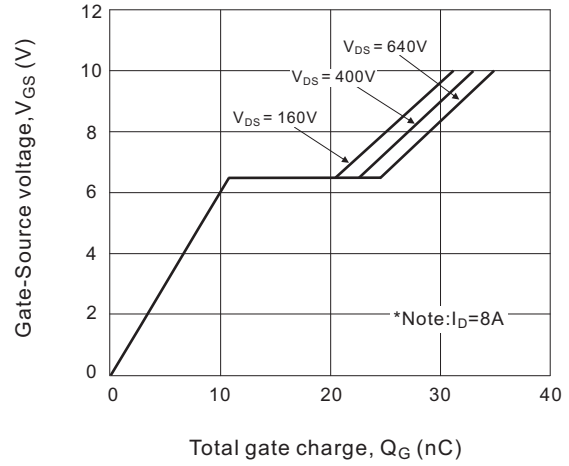


Fig.7 Breakdown voltage variation vs. temperature

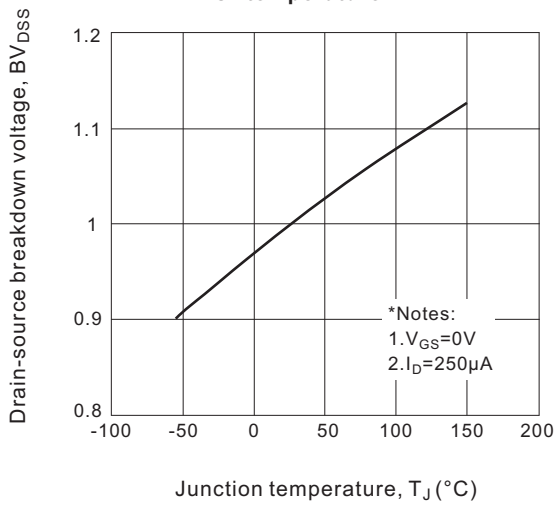


Fig.8 On-resistance variation vs. Junction temperature

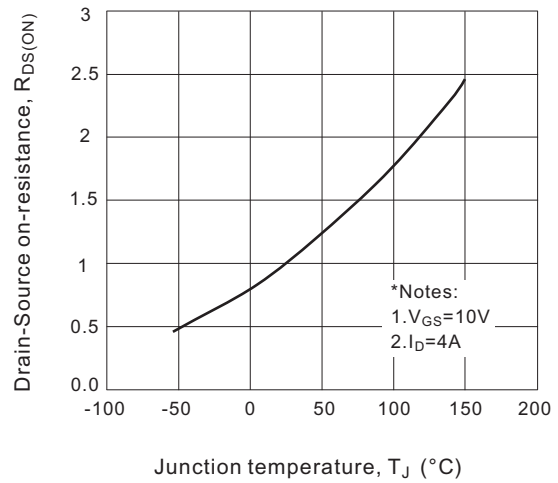


Fig.9-1 Maximum safe operating area for 8N80B

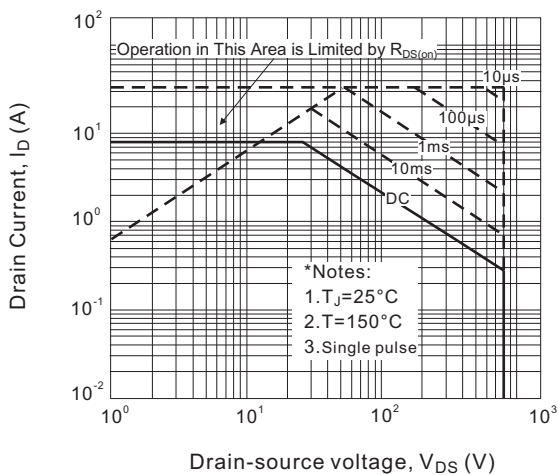


Fig.9-2 Maximum safe operating area for 8N80A

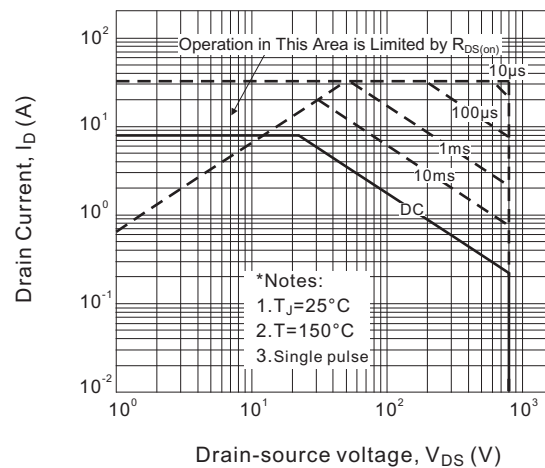


Fig.9-3 Maximum safe operating area for 8N80AF

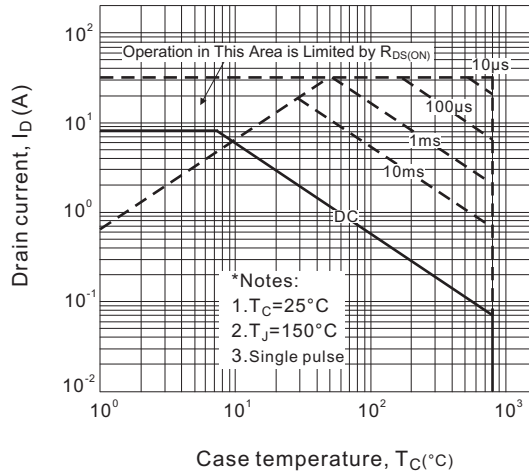


Fig.10 Maximum drain current vs. case temperature

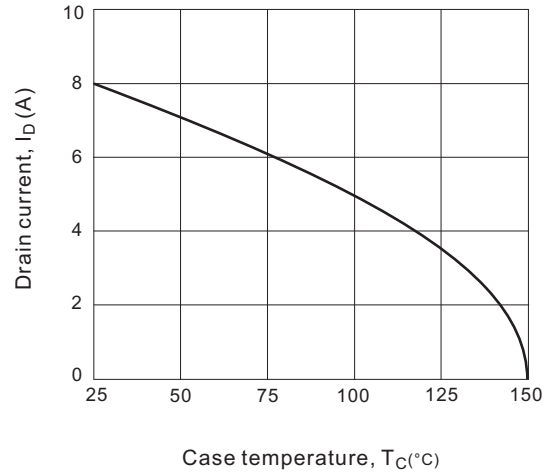


Fig.11-1 Transient Thermal Response Curve for 8N80A

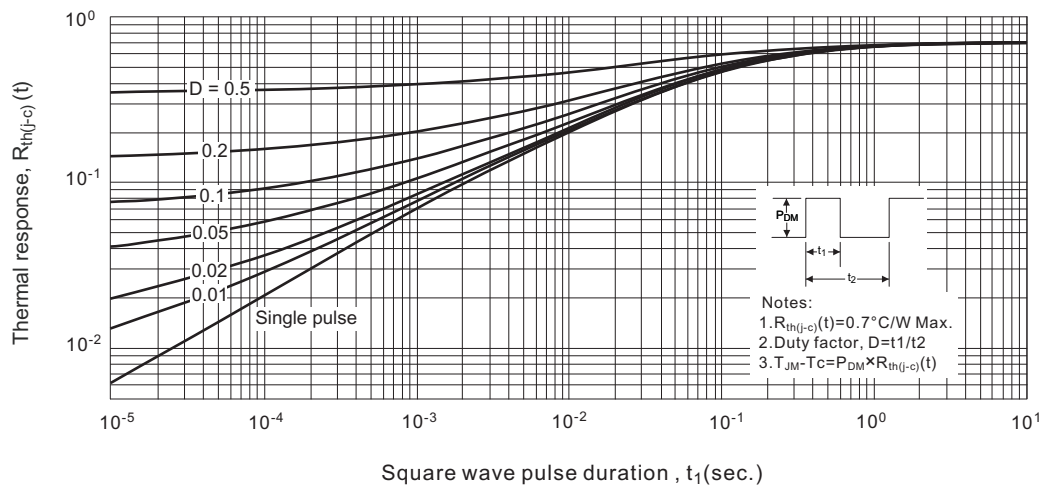


Fig.11-2 Transient Thermal Response Curve for 8N80AF

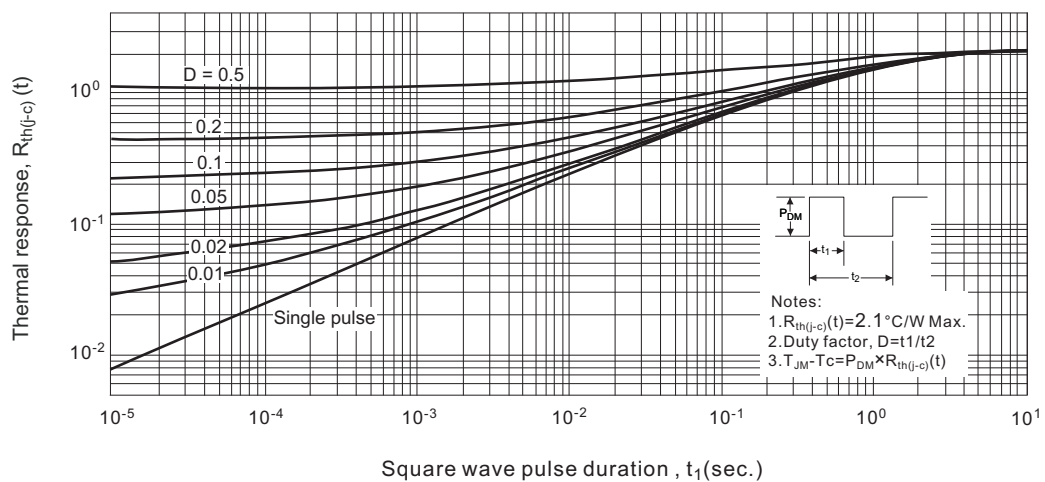
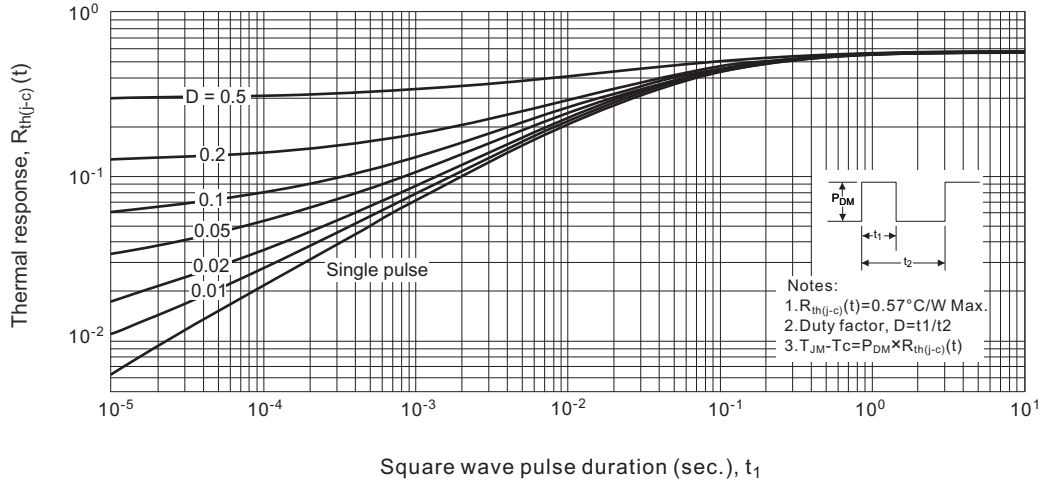


Fig.11-3 Transient Thermal Response Curve for 8N80B



■ TEST CIRCUITS AND WAVEFORMS

Fig.1A Peak diode recovery dv/dt test circuit

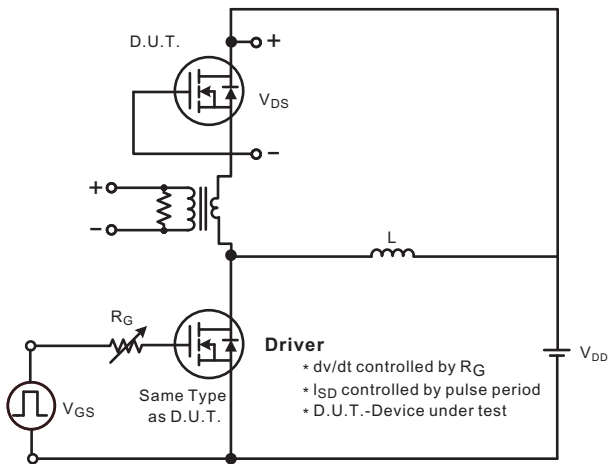


Fig.1B Peak diode recovery dv/dt waveforms

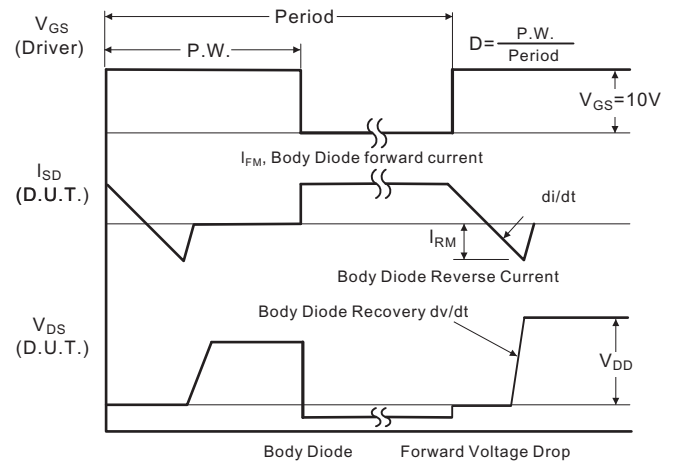


Fig.2A Switching test circuit

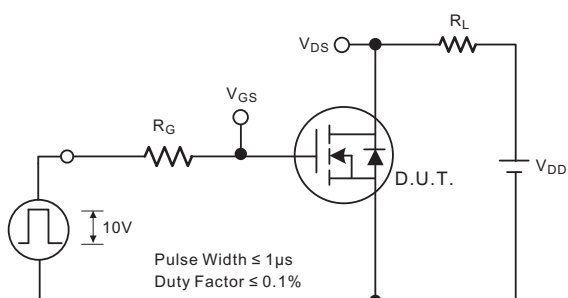


Fig.2B Switching Waveforms

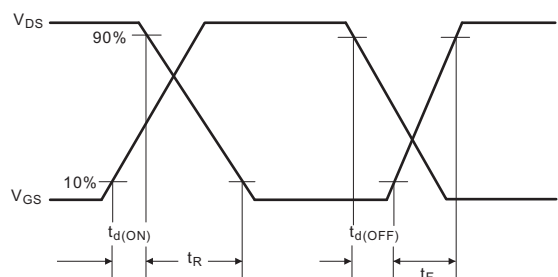


Fig.3A Gate charge test circuit

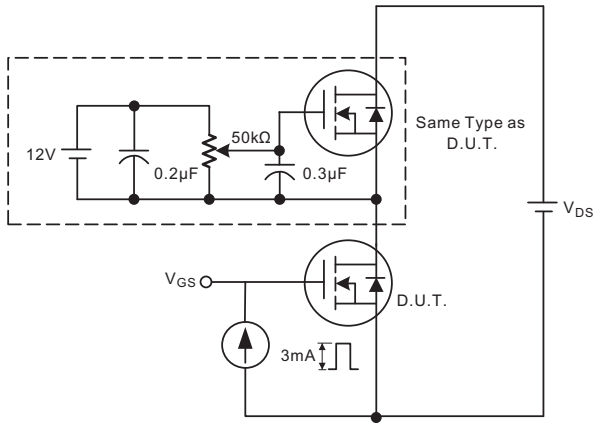


Fig.3B Gate charge waveform

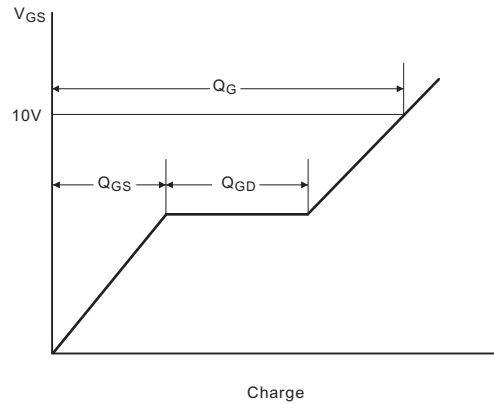


Fig.4A Unclamped Inductive switching test circuit

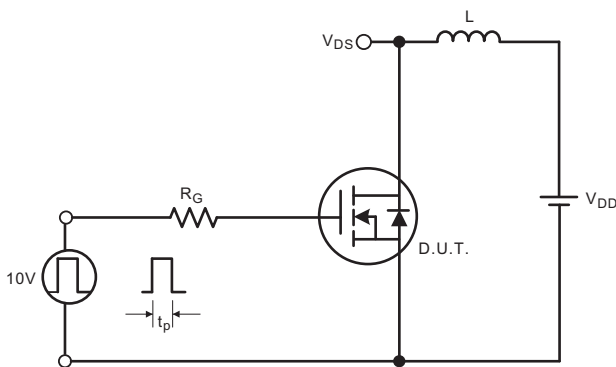
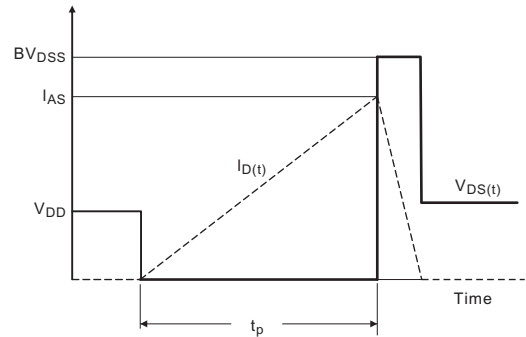
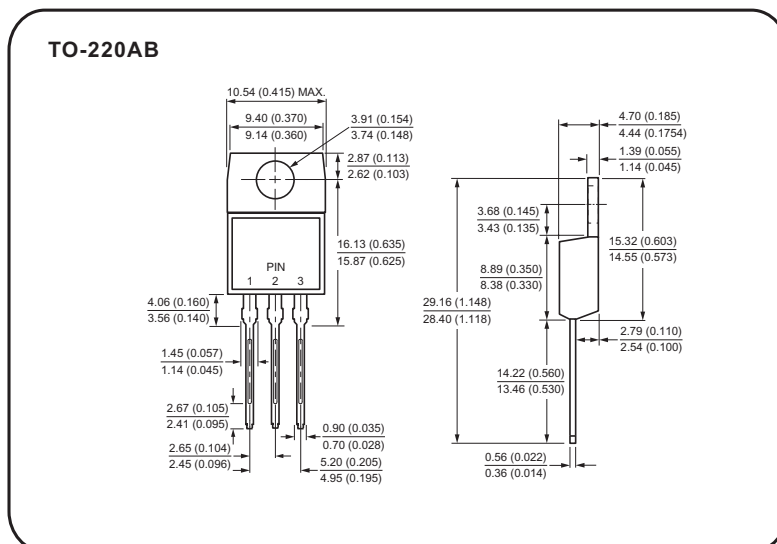


Fig.4B Unclamped Inductive switching waveforms

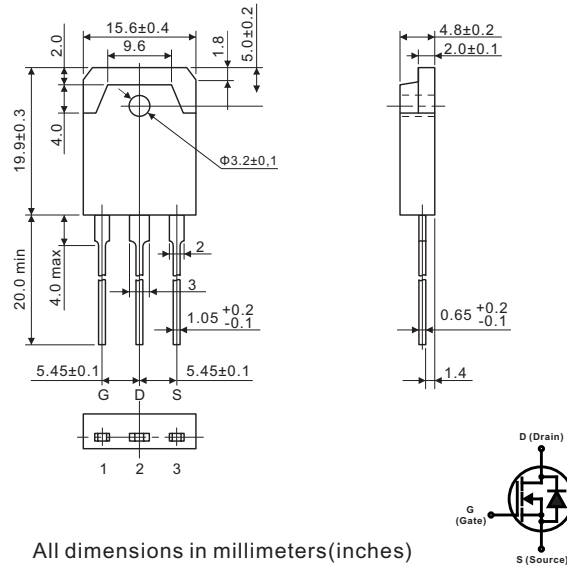


Case Style



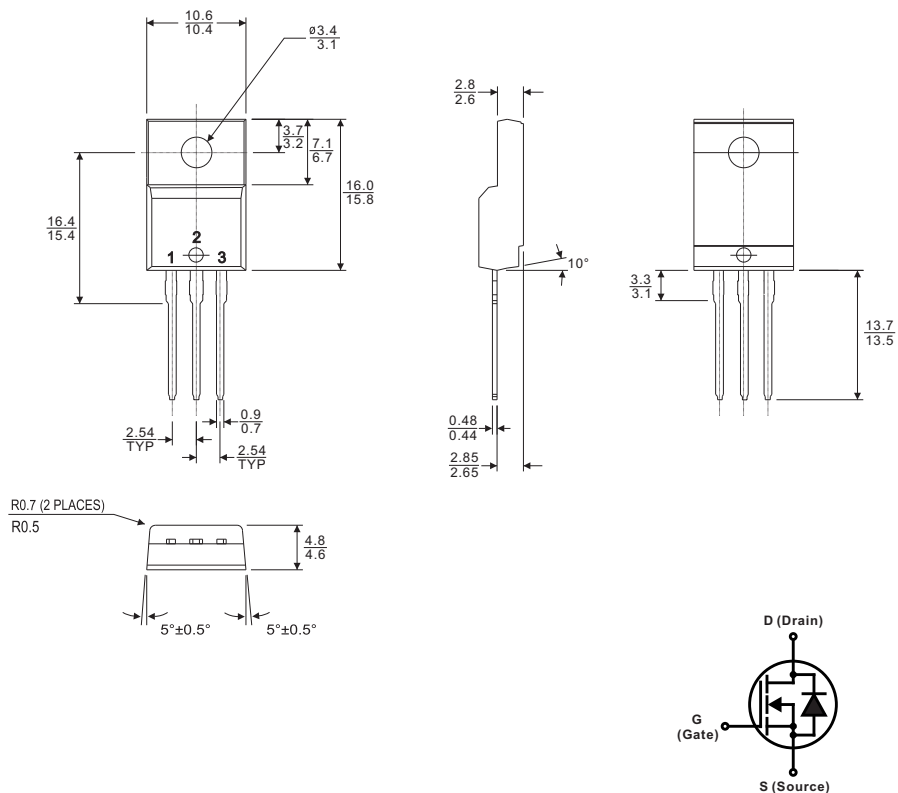
Case Style

TO-3PB



All dimensions in millimeters(inches)

TO-220F



All dimensions in millimeters