1. General Description

This 8-bit Micro-controller with built-in carrier generator uses a fully static CMOS technology to achieve high speed, small size, low power and high noise immunity.

On chip memory includes 512 words of ROM, and 28 bytes of static RAM.

2. Features

- Fully CMOS static design
- 8-bit data bus
- On chip ROM size : 512 words
- Internal RAM size : 28 bytes
  (24general purpose registers, 4 special registers)
- 34 single word instructions
- 14-bit instructions
- 2-level stacks
- Operating voltage : 2.0V ~ 5.0 V
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Internal RC 432K, 440K, 455K, 480KHz select in option.
- System clock : 455KHz crystal (OSC1 cap 50P; OSC2 cap 50P)
- Auto detect external crystal on board .
- PA0-7 : 8 input only pins with pull-high resistor and input low wakeup detect circuit.
- PB0 : CMOS output.
- PB1~7 : Seven open drain output pins.
- Built in remote control carrier synthesizer Fosc/8 (56.9K) or Fosc/12 (37.9K) by firmware setting.
- Option used PB0 NMOS without BJT.
- 4096 clocks for external oscillator start up time.

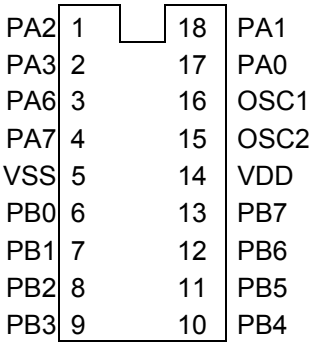
3. Applications

- Remote controller

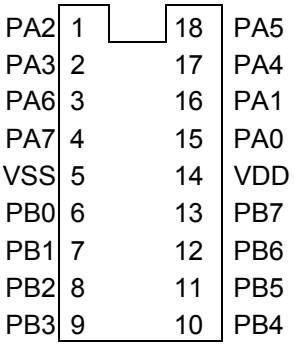
4. Pin Assignment

※ ***P – PDIP, S - PSOP***

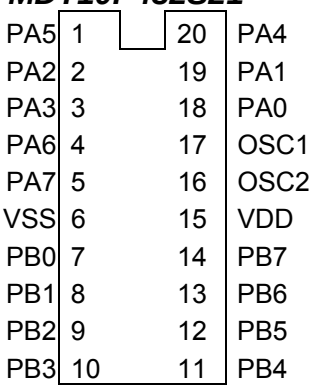
MDT10P432P11
MDT10P432S11



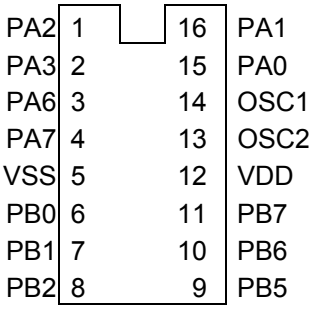
MDT10P432P13
MDT10P432S13



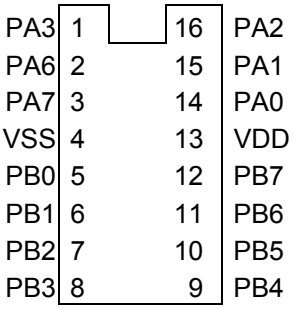
MDT10P432P21
MDT10P432S21



MDT10P432P31
MDT10P432S31



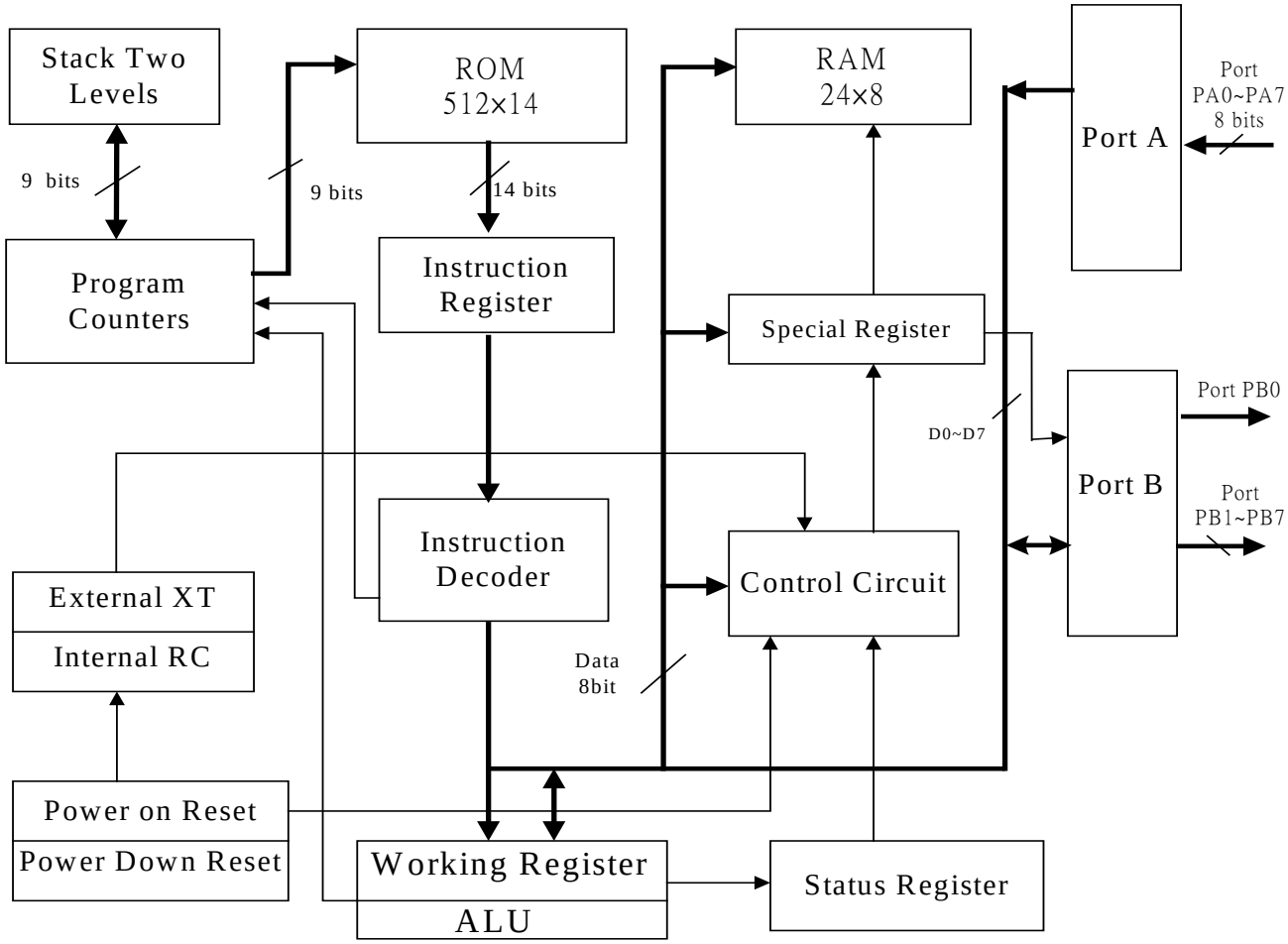
MDT10P432P35
MDT10P432S35



5. Order Information

Device	ROM (Words)	RAM (Bytes)	I/O	Package	mil	Remark
MDT10P432P11	0.5K	24	14 (6 input; 8 output)	18-DIP	300	18 pin ; 6 input (no PA 4~5) ; 8 output
MDT10P432P13	0.5K	24	16 (8 input; 8 output)	18-DIP	300	18 pin ; 8 input ; 8 output; (no OSC1&2)
MDT10P432P21	0.5K	24	16 (8 input; 8 output)	20-DIP	300	20 pin ; 8 input ; 8 output
MDT10P432P31	0.5K	24	12 (6 input; 6 output)	16-DIP	300	16 pin ; 6 input (no PA 4&5) ; 6 output (no PB 3&4)
MDT10P432P35	0.5K	24	14 (6 input; 8 output)	16-DIP	300	16 pin ; 6 input (no PA 4~5) ; 8 output; (no OSC1&2)
MDT10P432S11	0.5K	24	14 (6 input; 8 output)	18-SOP	300	18 pin ; 6 input (no PA 4~5) ; 8 output
MDT10P432S13	0.5K	24	16 (8 input; 8 output)	18-SOP	300	18 pin ; 8 input ; 8 output; (no OSC1&2)
MDT10P432S21	0.5K	24	16 (8 input; 8 output)	20-SOP	300	20 pin ; 8 input ; 8 output
MDT10P432S31	0.5K	24	12 (6 input; 6 output)	16-SOP	150	16 pin ; 6 input (no PA 4&5) ; 6 output (no PB 3&4)
MDT10P432S35	0.5K	24	14 (6 input; 8 output)	16-SOP	150	16 pin ; 6 input (no PA 4~5) ; 8 output; (no OSC1&2)

6. Block Diagram

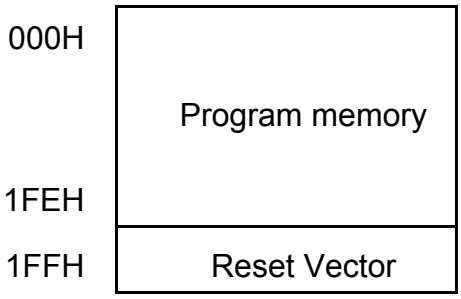


7. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA7	I	Port A, TTL input level. Built in 50K ohm pull-high resistor. In sleep mode, a high-to-low change on any pin will cause chip reset.
PB0	O	CMOS output pin. Enable NMOS sink 250mA by option (replace BJT)
PB1~PB7	O	Port B open drain output pins, 50K ohm pull-high resistor.
OSC1	I	Crystal oscillation input pin
OSC2	O	Crystal oscillation output pin
Vdd		Power supply
Vss		Ground

8. Memory Map

8.1 Program memory :

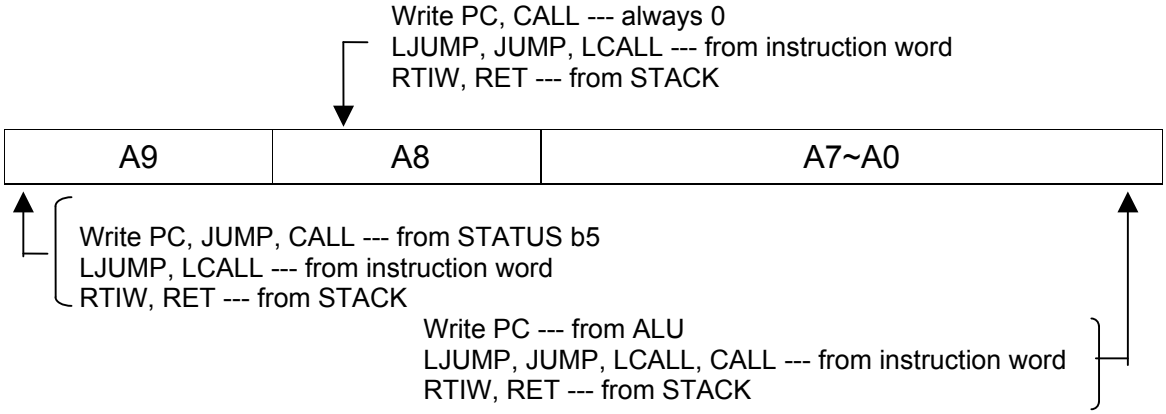


8.2 Register Map

Address	Description
00	Indirect Addressing Register
01	Unimplemented
02	PC
03	STATUS
04	MSR
05	Port A (Input Only)
06	Port B output register
07	Unimplemented
08~1F	Internal RAM, General Purpose Register

(1) IAR (Indirect Address Register) : R0

(2) PC (Program Counter) : R2



(3) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PF	Power loss Flag bit
4	/LPT	Low power detect
		=0 : Vdd is lower than 2.1 ~ 2.3V
		=1 : Vdd is higher than 2.1 ~ 2.3V
5	——	General purpose bit
7 - 6	——	Carrier frequency control bits
		=00 No carrier (default)
		=01 Fosc/8, 1/2 duty
		=10 Fosc/12, 1/2 duty
		=11 Fosc/12, 1/3 duty (1/3 – Hi ; 2/3 - Low)

(4) MSR (Memory Select Register) : R4

(5) PORT A : R5

Bit 7-0 : Port A data input

(6) PORT B : R6

Bit 7-1 : PB7-PB1 output register (open drain output)

Bit 0 : PB0 output register (CMOS output)

9. Reset Condition for all Registers

Register	Address	Power-On Reset
IAR	00h	—
PC	02h	1111 1111
STATUS	03h	0001 1xxx
MSR	04h	111x xxxx
PB Output data	06h	1111 111#

Note : " x "＝unknown, " – "＝unimplemented, read as "0"

"**#** "＝value depends on condition

10. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z

Instruction Code	Mnemonic Operands	Function	Operating	Status
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
1000nn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
1010nn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110000 nnnnnnnn	CALL n	Call subroutine	n→PC, PC+1→Stack	None
110001 iiiiiiii	RTIW i	Return, place immediate to W	Stack→PC, i→W	None
11001n nnnnnnnn	JUMP n	JUMP to address	n→PC	None

Note :

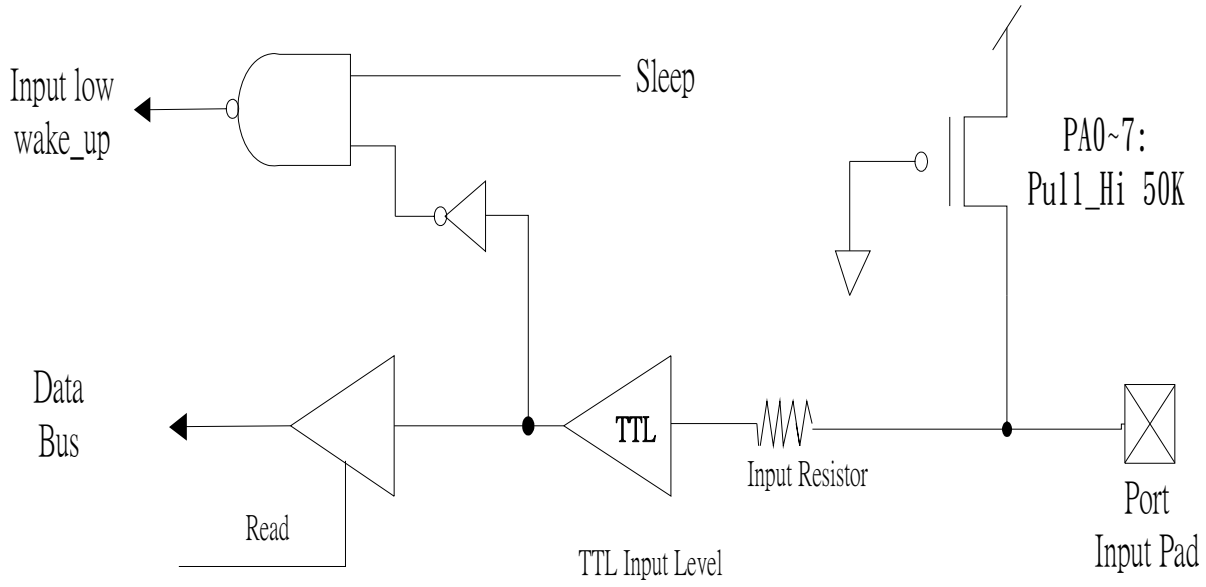
W	:	Working register	b	:	Bit position
CPIO	:	Control I/O port register	t	:	Target
HC	:	Half carry			0 : Working register
Z	:	Zero flag			1 : General register
C	:	Carry flag			
PF	:	Power loss flag	R	:	General register address
PC	:	Program Counter	i	:	Immediate data (8 bits)
OSC	:	Oscillator	n	:	Immediate address
Inclu.	:	Inclusive ‘∪’	/	:	Complement
Exclu.	:	Exclusive ‘⊕’	x	:	Don’t care
AND	:	Logic AND ‘∩’			

11. Electrical Characteristics

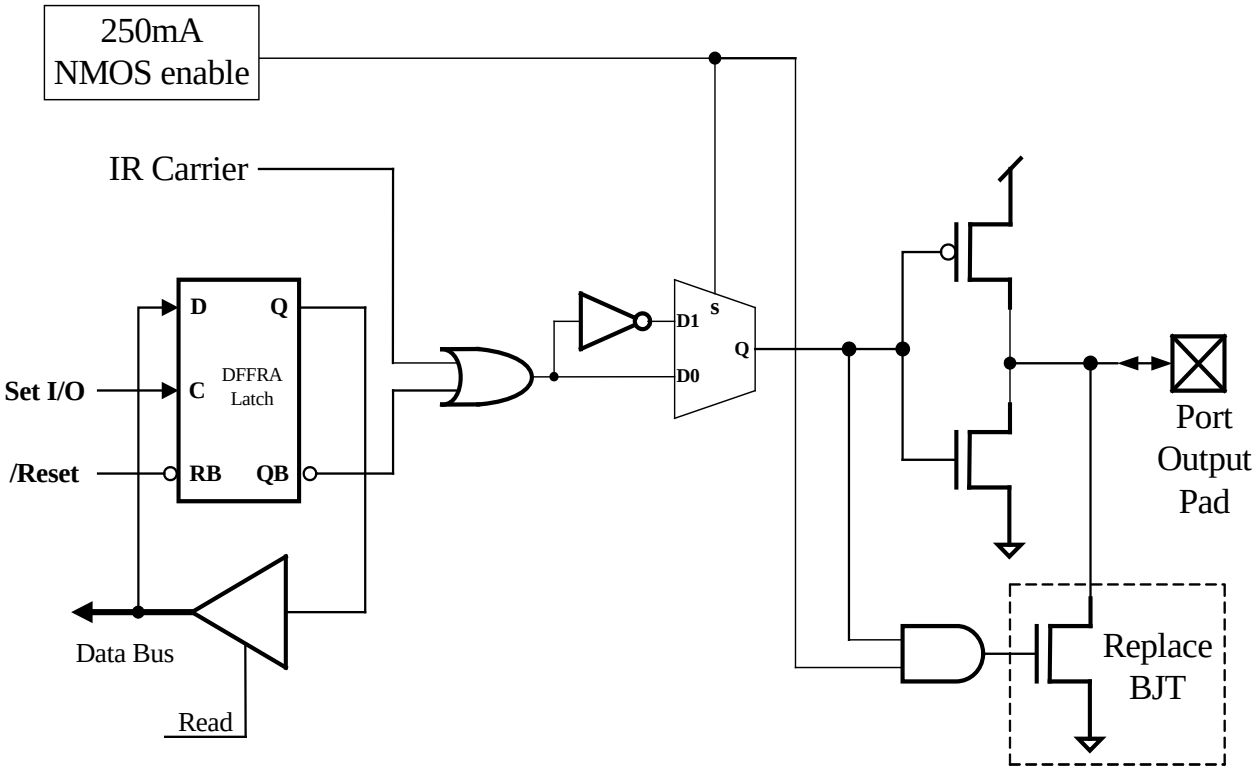
(Operating temperature at 25℃).

Sym	Description	Condition	Min	Typ	Max	Unit
Vdd	Operating voltage		2.0		6.0	V
V_{IL}	Input Low Voltage					
	PA	Vdd=5V	-0.6		1.0	V
V_{IH}	Input high Voltage					
	PA	Vdd=5V	2.0		Vdd+0.6	V
I_{IL}	Input leakage current	Vdd=5V			+/-1	μA
V_{OL}	Output Low Voltage					
	PB7~0	Vdd=5V, I_{OL}=20mA		0.6		V
		Vdd=5V, I_{OL}=5mA		0.2		V
	PB0 enable 250mA NMOS	Vdd=5V, I_{OL}=20mA		0.08		V
		Vdd=5V, I_{OL}=20mA		0.03		V
	PB0 enable 250mA NMOS	Vdd=3V, sink current		250		mA
		Vdd=2V, sink current		100		mA
V_{OH}	Output High Voltage					
	PB0	Vdd=5V, I_{OH}= -20mA		2.8		V
		Vdd=5V, I_{OH}= -5mA		4.2		V
V_{pr}	Power Edge-detector Reset Voltage			1.8		V

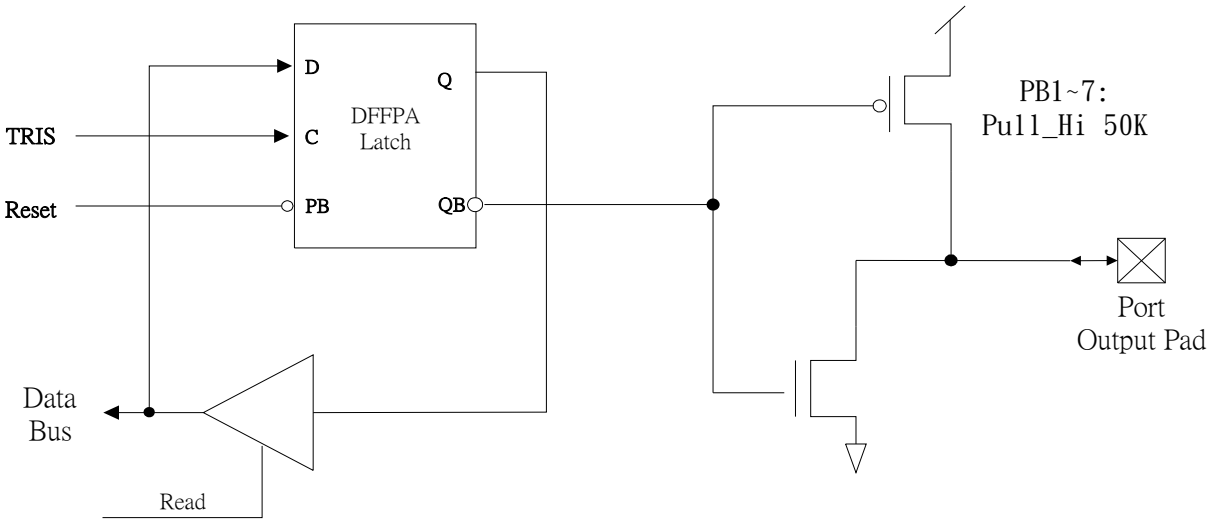
12. PA0 ~ PA7 Equivalent Circuit



13. (A) PB0 Equivalent Circuit



(B) PB1~7 Equivalent Circuit

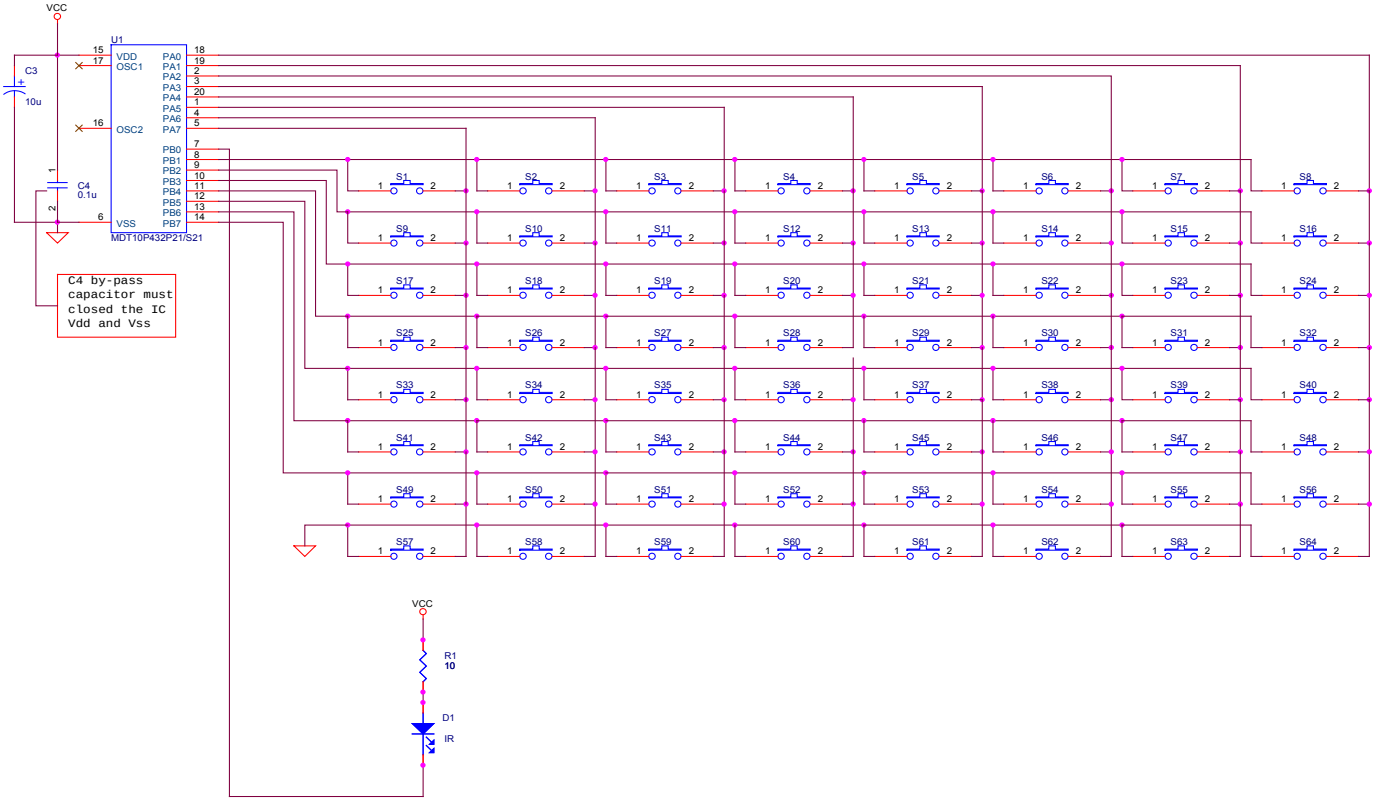


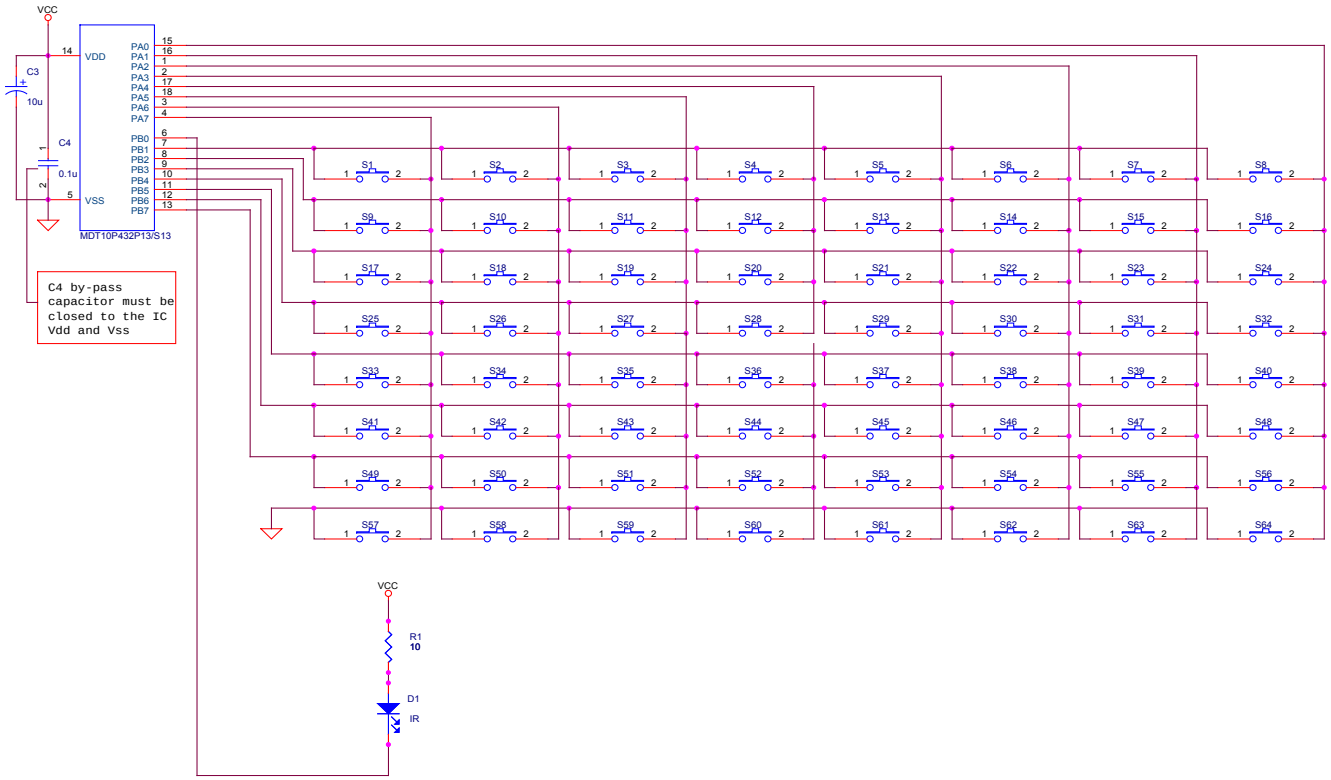
14. Application circuit (reference)

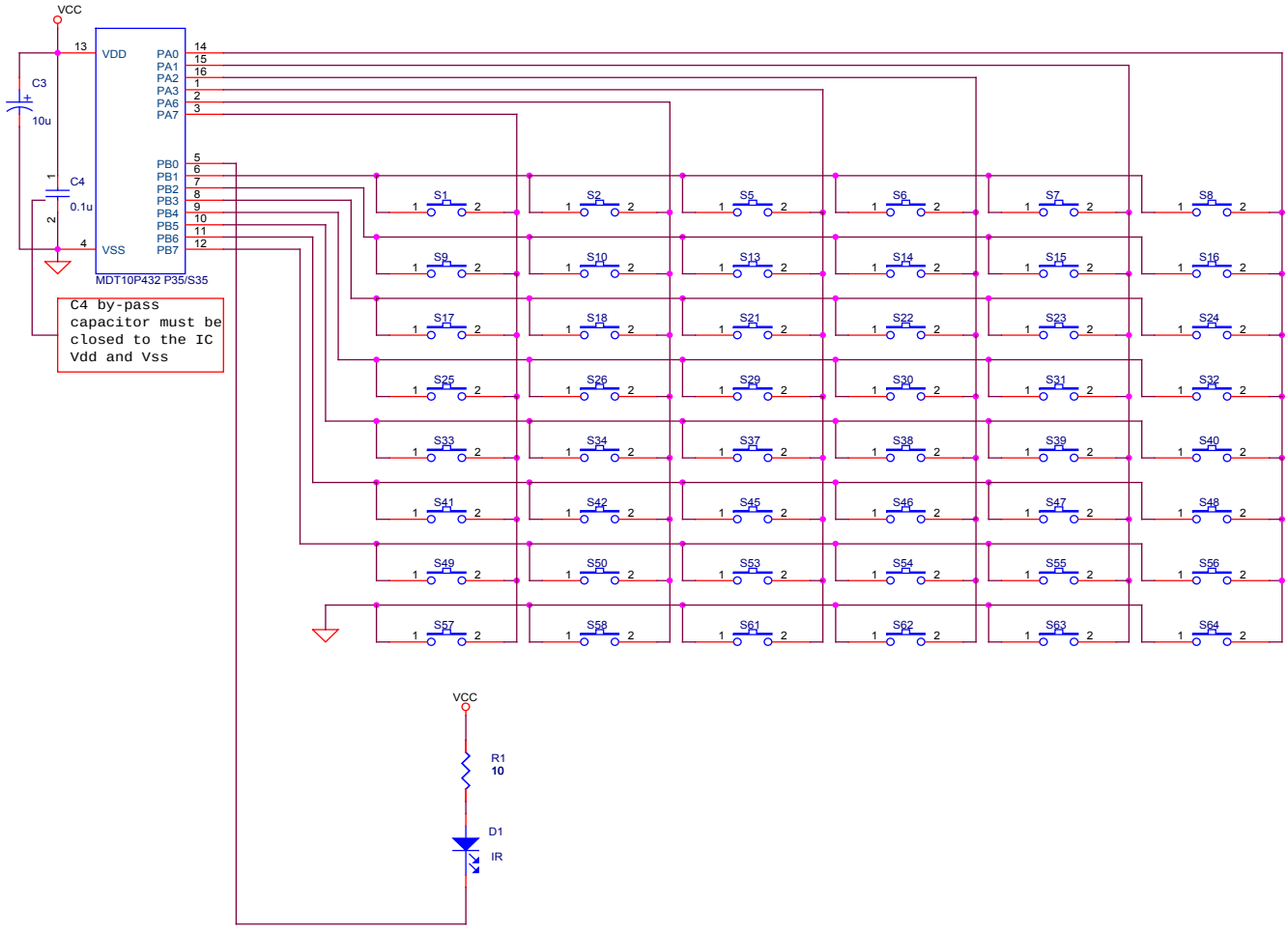
(A). Enable internal 455KHz & 250 mA NMOS (Without BJT)

Note : Power Vdd & Vss must used metal line to IC Vdd & Vss with shortest distance

IR must used metal line to Vdd & PB0

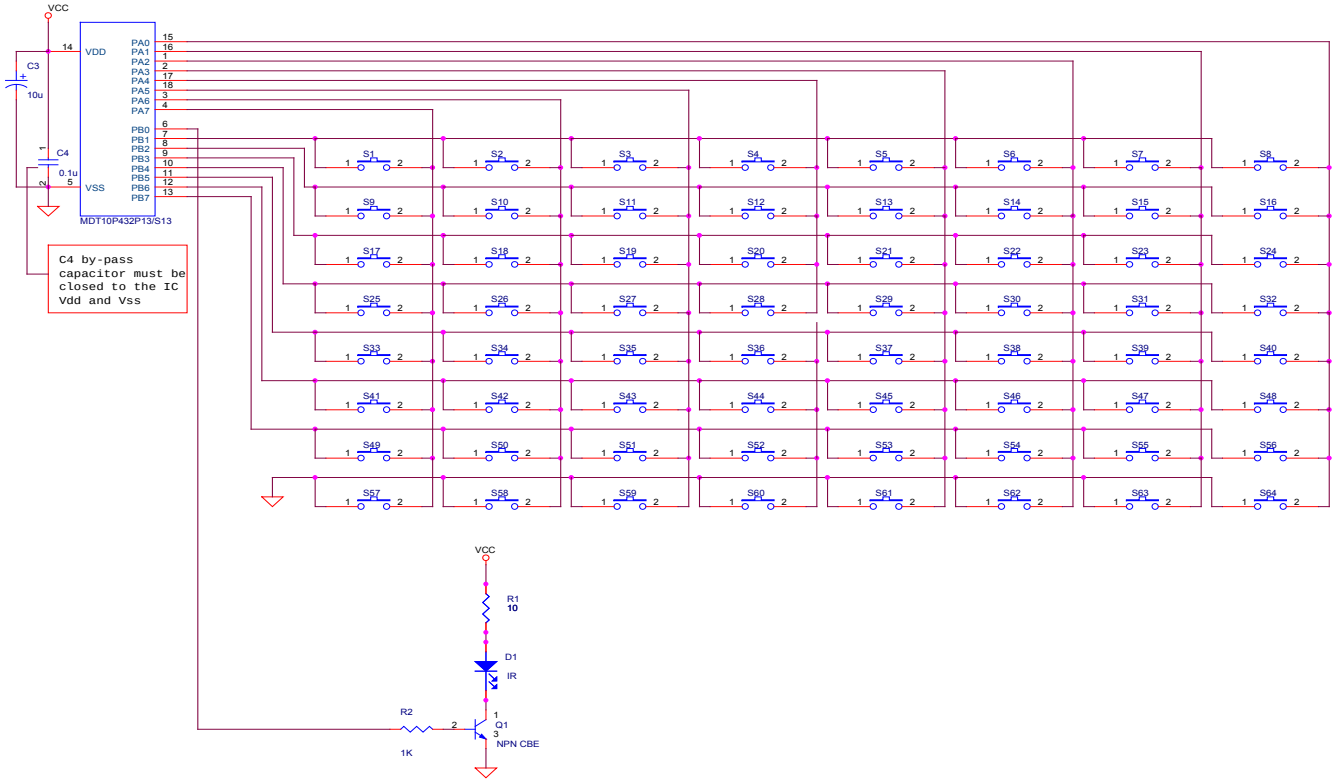


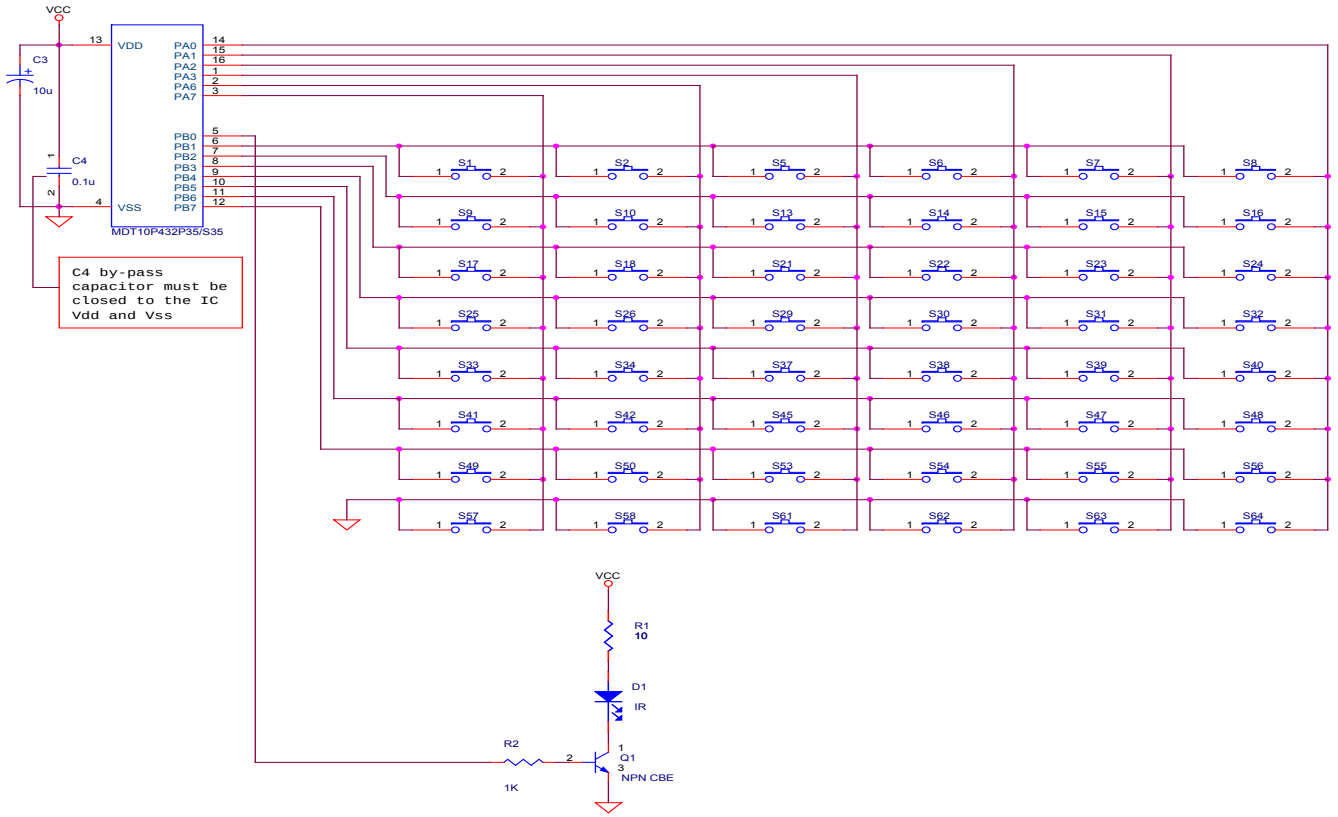

VCC
C3
10u
C4
0.1u
VDD
VSS
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
MDT10P432P13/S13
C4 by-pass capacitor must be closed to the IC Vdd and Vss
R1
10
D1
IR


VCC
C3
10u
C4
0.1u
VDD
VSS
PA0
PA1
PA2
PA3
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
MDT10P432 P35/S35
C4 by-pass capacitor must be closed to the IC Vdd and Vss
R1
10
D1
IR

(B). Enable internal 455KHz , disable 250 mA NMOS

Note : Power Vdd & Vss must used metal line to IC Vdd & Vss with shortest distance





(C). Disable internal 455KHz & 250 mA NMOS

Note : Power Vdd & Vss must used metal line to IC Vdd & Vss with shortest distance