

TENTATIVE TOSHIBA MULTI-CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

SRAM AND FLASH MEMORY MIXED MULTI-CHIP PACKAGE

DESCRIPTION

The TH50VSF3582/3583AASB is a mixed multi-chip package containing a 8,388,608-bit Full CMOS SRAM and a 33,554,432-bit flash memory. The CIOS and CIOF inputs can be used to select the optimal memory configuration. The power supply. FLASH MEMORY a Simultaneous Read/Write operation so that data can be read during a Write or Erase operation. The TH50VSF3582/3583AASB can range from 2.67 V to 3.3 V. The TH50VSF3582/3583AASB is available in a 69-pin BGA package, making it suitable for a variety of design applications.

FEATURES

- Power supply voltage
 $V_{CCs} = 2.67\text{ V} \sim 3.3\text{ V}$
 $V_{CCf} = 2.67\text{ V} \sim 3.3\text{ V}$
- Data retention supply voltage
 $V_{CCs} = 1.5\text{ V} \sim 3.3\text{ V}$
- Current consumption
 Operating: 45 mA maximum (CMOS level)
 Standby: 10 μA maximum (SRAM CMOS level)
 Standby: 10 μA maximum (FLASH)
- Block erase architecture for flash memory
 8 \times 8 Kbytes
 63 \times 64 Kbytes
- Organization

| CIOF | CIOS | Flash Memory | SRAM |
|----------|----------|----------------------------|---------------------------|
| V_{CC} | V_{CC} | 2,097,152 words of 16 bits | 524,288 words of 16 bits |
| V_{CC} | V_{SS} | 2,097,152 words of 16 bits | 1,048,576 words of 8 bits |
| V_{SS} | V_{SS} | 4,194,304 words of 8 bits | 1,048,576 words of 8 bits |

- Function mode control for flash memory
 Compatible with JEDEC-standard commands
- Flash memory functions
 Simultaneous Read/Write operations
 Auto-Program
 Auto Chip Erase, Auto Block Erase
 Auto Multiple-Block Erase
 Program Suspend/Resume
 Block-Erase Suspend/Resume
 Data Polling/Toggle Bit function
 Block Protection/Boot Block Protection
 Automatic Sleep, Hidden ROM Area Supports
 Common Flash Memory Interface (CFI)
 Byte/Word Mode
- Erase and Program cycle for flash memory
 10^5 cycles (typical)
- Boot block architecture for flash memory
 TH50VSF3582AASB: Top boot block
 TH50VSF3583AASB: Bottom boot block
- Package
 P-FBGA69-1209-0.80A3: 0.31 g (typ.)

PIN ASSIGNMENT (TOP VIEW)

- Case: CIOF = V_{CC} , CIOS = $V_{CC} (\times 16, \times 16)$

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|----|--------------------------|------------------------|------------------------|----------------------------|------------------------|------|------|----------|----|
| A | NC | | | | | | | | | NC |
| B | NC | | | | | | | | | NC |
| C | NC | | A7 | $\overline{\text{LB}}$ | $\overline{\text{WP/ACC}}$ | $\overline{\text{WE}}$ | A8 | A11 | | |
| D | | A3 | A6 | $\overline{\text{UB}}$ | $\overline{\text{RESET}}$ | CE2S | A19 | A12 | A15 | |
| E | | A2 | A5 | A18 | RY/ $\overline{\text{BY}}$ | A20 | A9 | A13 | NC | |
| F | NC | A1 | A4 | A17 | | | A10 | A14 | NC | NC |
| G | NC | A0 | V_{SS} | DQ1 | | | DQ6 | DU | A16 | NC |
| H | | $\overline{\text{CEF}}$ | $\overline{\text{OE}}$ | DQ9 | DQ3 | DQ4 | DQ13 | DQ15 | CIOF | |
| J | | $\overline{\text{CE1S}}$ | DQ0 | DQ10 | V_{CCf} | V_{CCs} | DQ12 | DQ7 | V_{SS} | |
| K | | | DQ8 | DQ2 | DQ11 | CIOS | DQ5 | DQ14 | | |
| L | NC | | | | | | | | | NC |
| M | NC | | | | | | | | | NC |

PIN NAMES

| | |
|---|--|
| A0~A21 | Address Inputs |
| A12S | A12 Input for SRAM |
| A12F | A12 Input for Flash Memory |
| SA | A18 Input for SRAM |
| DQ0~DQ15 | Data Inputs/Outputs |
| $\overline{\text{CE1S}}$, $\overline{\text{CE2S}}$ | Chip Enable Inputs for SRAM |
| $\overline{\text{CEF}}$ | Chip Enable Input for Flash Memory |
| $\overline{\text{OE}}$ | Output Enable Input |
| $\overline{\text{WE}}$ | Write Enable Input |
| $\overline{\text{LB}}$, $\overline{\text{UB}}$ | Data Byte Control Input |
| RY/ $\overline{\text{BY}}$ | Ready/Busy Output |
| $\overline{\text{RESET}}$ | Hardware Reset Input |
| $\overline{\text{WP/ACC}}$ | Write Protect/Program Acceleration Input |
| CIOS | Word Enable Input for SRAM |
| CIOF | Word Enable Input for Flash Memory |
| V_{CCs} | Power Supply for SRAM |
| V_{CCf} | Power Supply for Flash Memory |
| V_{SS} | Ground |
| NC | Not Connected |
| DU | Don't Use |

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PIN ASSIGNMENT (TOP VIEW)

- Case: CIOF = V_{CC}, CIOS = V_{SS} (×16, ×8)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|----|-------------------|-----------------|------|---------------------|------------------|------|------|-----------------|----|
| A | NC | | | | | | | | | NC |
| B | NC | | | | | | | | | NC |
| C | NC | | A7 | DU | $\overline{WP/ACC}$ | \overline{WE} | A8 | A11 | | |
| D | | A3 | A6 | DU | \overline{RESET} | CE2S | A19 | A12 | A15 | |
| E | | A2 | A5 | A18 | RY/BY | A20 | A9 | A13 | NC | |
| F | NC | A1 | A4 | A17 | | | A10 | A14 | NC | NC |
| G | NC | A0 | V _{SS} | DQ1 | | | DQ6 | SA | A16 | NC |
| H | | \overline{CEF} | \overline{OE} | DQ9 | DQ3 | DQ4 | DQ13 | DQ15 | CIOF | |
| J | | $\overline{CE1S}$ | DQ0 | DQ10 | V _{CCf} | V _{CCs} | DQ12 | DQ7 | V _{SS} | |
| K | | | DQ8 | DQ2 | DQ11 | CIOS | DQ5 | DQ14 | | |
| L | NC | | | | | | | | | NC |
| M | NC | | | | | | | | | NC |

- Case: CIOF = V_{SS}, CIOS = V_{SS} (×8, ×8)

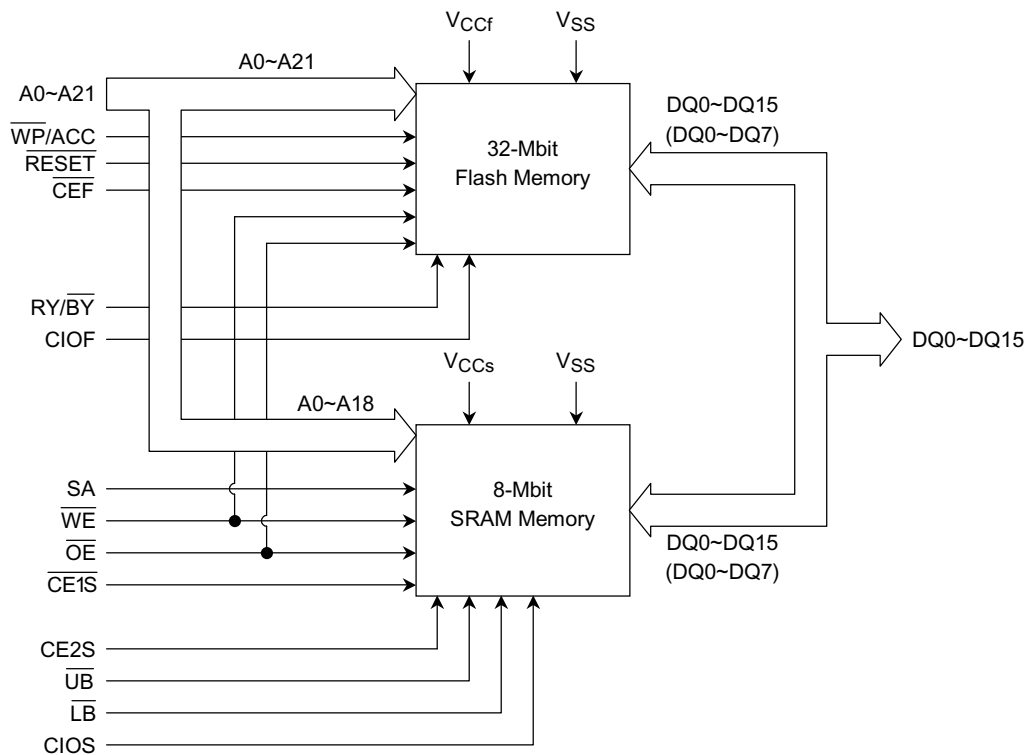
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|----|-------------------|-----------------|-----|---------------------|------------------|-----|------|-----------------|----|
| A | NC | | | | | | | | | NC |
| B | NC | | | | | | | | | NC |
| C | NC | | A7 | DU | $\overline{WP/ACC}$ | \overline{WE} | A8 | A11 | | |
| D | | A3 | A6 | DU | \overline{RESET} | CE2S | A20 | A13 | A16 | |
| E | | A2 | A5 | A19 | RY/BY | A21 | A9 | A14 | NC | |
| F | NC | A1 | A4 | A18 | | | A10 | A15 | NC | NC |
| G | NC | A0 | V _{SS} | DQ1 | | | DQ6 | A12S | A17 | NC |
| H | | \overline{CEF} | \overline{OE} | DU | DQ3 | DQ4 | DU | A12F | CIOF | |
| J | | $\overline{CE1S}$ | DQ0 | DU | V _{CCf} | V _{CCs} | DU | DQ7 | V _{SS} | |
| K | | | DU | DQ2 | DU | CIOS | DQ5 | DU | | |
| L | NC | | | | | | | | | NC |
| M | NC | | | | | | | | | NC |

Note: A12F and A12S should be wired and used as A12 pin.

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BLOCK DIAGRAM



MODE SELECTION

| OPERATION MODE | \overline{CEF} | $\overline{CE1S}$ | $\overline{CE2S}$ | \overline{OE} | \overline{WE} | \overline{RESET} | \overline{UB} | \overline{LB} | $\overline{WP/ACC}$ | DQ0-DQ7 | DQ8-DQ15 |
|--------------------------------|------------------|-------------------|-------------------|-----------------|-----------------|--------------------|-----------------|-----------------|---------------------|------------------|------------------|
| Flash Read | L | H | X | L | H | H | X | X | X | D _{OUT} | D _{OUT} |
| | L | X | L | L | H | H | X | X | X | D _{OUT} | D _{OUT} |
| SRAM Read | H | L | H | L | H | H | L | L | X | D _{OUT} | D _{OUT} |
| | H | L | H | L | H | H | H | L | X | D _{OUT} | Hi-Z |
| | H | L | H | L | H | H | L | H | X | Hi-Z | D _{OUT} |
| Flash Write | L | H | X | H | L | H | X | X | X | D _{IN} | D _{IN} |
| | L | X | L | H | L | H | X | X | X | D _{IN} | D _{IN} |
| SRAM Write | H | L | H | X | L | H | L | L | X | D _{IN} | D _{IN} |
| | H | L | H | X | L | H | H | L | X | D _{IN} | Hi-Z |
| | H | L | H | X | L | H | L | H | X | Hi-Z | D _{IN} |
| Flash Output Disable | X | H | X | H | H | X | X | X | X | Hi-Z | Hi-Z |
| | X | X | L | H | H | X | X | X | X | Hi-Z | Hi-Z |
| SRAM Output Disable | H | X | X | H | H | X | X | X | X | Hi-Z | Hi-Z |
| | H | X | X | X | X | X | H | H | X | Hi-Z | Hi-Z |
| Flash Standby | H | X | X | X | X | H | X | X | X | S | S |
| Flash Hardware Reset / Standby | X | X | X | X | X | L | X | X | X | S | S |
| SRAM Standby | X | H | X | X | X | X | X | X | X | F | F |
| | X | X | L | X | X | X | X | X | X | F | F |

Notes: L = V_{IL} ; H = V_{IH} ; X = V_{IH} or V_{IL}

F: Depends on flash memory operation mode. S: Depends on SRAM operation mode.

When CIOS = V_{CC} and CIOF = V_{CC} , Word Mode is selected for both SRAM and flash memory.

Does not apply when $\overline{CEF} = \overline{CE1S} = V_{IL}$ and $\overline{CE2S} = V_{IH}$ at the same time.

ID CODE TABLE

| TYPE | | A20~A12 | A6 | A1 | A0 | CODE (HEX) ⁽¹⁾ |
|----------------------|-----------------|-------------------|----|----|----|---------------------------|
| Manufacturer Code | | * | L | L | L | 0098H |
| Device Code | TH50VSF3582AASB | * | L | L | H | 009AH |
| | TH50VSF3583AASB | * | L | L | H | 009CH |
| Verify Block Protect | | BA ⁽²⁾ | L | H | L | Data ⁽³⁾ |

Note: * = V_{IH} or V_{IL}

L = V_{IL} H = V_{IH}

(1) DQ8~DQ15 are Hi-Z in Byte mode

(2) BA: Block address

(3) 0001H: Protected block
0000H: Unprotected block

COMMAND SEQUENCES

| COMMAND SEQUENCE | BUS WRITE CYCLES REQ'D | FIRST BUS WRITE CYCLE | | SECOND BUS WRITE CYCLE | | THIRD BUS WRITE CYCLE | | FOURTH BUS WRITE CYCLE | | FIFTH BUS WRITE CYCLE | | SIXTH BUS WRITE CYCLE | | |
|-----------------------|------------------------|-----------------------|--------------------------|------------------------|---------------------|-----------------------|--------------------------|------------------------|---------------------|-----------------------|------|-----------------------|-------------------|-----|
| | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | |
| Read/Reset | 1 | XXXH | F0H | | | | | | | | | | | |
| Read/Reset | Word | 3 | 555H | AAH | 2AAH | 55H | 555H | F0H | RA ⁽¹⁾ | RD ⁽²⁾ | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| ID Read | Word | 3 | 555H | AAH | 2AAH | 55H | BK ⁽³⁾ + 555H | 90H | IA ⁽⁴⁾ | ID ⁽⁵⁾ | | | | |
| | Byte | | AAAH | | 555H | | BK ⁽³⁾ + AAHA | | | | | | | |
| Auto-Program | Word | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA ⁽⁶⁾ | PD ⁽⁷⁾ | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Program Suspend | 1 | BK ⁽³⁾ | B0H | | | | | | | | | | | |
| Program Resume | 1 | BK ⁽³⁾ | 30H | | | | | | | | | | | |
| Auto Chip Erase | Word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| | Byte | | AAAH | | 555H | | AAAH | | 555H | | AAAH | | | |
| Auto Block Erase | Word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | BA ⁽⁸⁾ | 30H |
| | Byte | | AAAH | | 555H | | AAAH | | 555H | | AAAH | | | |
| Block Erase Suspend | 1 | BK ⁽³⁾ | B0H | | | | | | | | | | | |
| Block Erase Resume | 1 | BK ⁽³⁾ | 30H | | | | | | | | | | | |
| Block Protect | 4 | XXXH | 60H | BPA ⁽⁹⁾ | 60H | XXXH | 40H | BPA ⁽⁹⁾ | BPD ⁽¹⁰⁾ | | | | | |
| Verify Block Protect | Word | 3 | 555H | AAH | 2AAH | 55H | BK ⁽³⁾ + 555H | 90H | BPA ⁽⁹⁾ | BPD ⁽¹⁰⁾ | | | | |
| | Byte | | AAAH | | 555H | | BK ⁽³⁾ + AAHA | | | | | | | |
| Fast Program Set | Word | 3 | 555H | AAH | 2AAH | 55H | 555H | 20H | | | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Fast Program | 2 | XXXH | A0H | PA ⁽⁶⁾ | PD ⁽⁷⁾ | | | | | | | | | |
| Fast Program Reset | 2 | XXXH | 90H | XXXH | F0H ⁽¹³⁾ | | | | | | | | | |
| Hidden ROM Mode Entry | Word | 3 | 555H | AAH | 2AAH | 55H | 555H | 88H | | | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Hidden ROM Program | Word | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA ⁽⁶⁾ | PD ⁽⁷⁾ | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Hidden ROM Erase | Word | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | BA ⁽⁸⁾ | 30H |
| | Byte | | AAAH | | 555H | | AAAH | | 555H | | AAAH | | | |
| Hidden ROM Mode Exit | Word | 4 | 555H | AAH | 2AAH | 55H | 555H | 90H | XXXH | 00H | | | | |
| | Byte | | AAAH | | 555H | | AAAH | | | | | | | |
| Query Command | Word | 2 | BK ⁽³⁾ + 55H | 98H | CA ⁽¹¹⁾ | CD ⁽¹²⁾ | | | | | | | | |
| | Byte | | BK ⁽³⁾ + AAHA | | | | | | | | | | | |

Note: The system should generate the following address patterns:

- Word Mode: 555H or 2AAH to addresses A10~A0
- Byte Mode: AAHA or 555H to addresses A10~A0, A12F
- DQ8~DQ15 are ignored in Word mode.
- Byte mode when V_{IL} is inputted to CIOF, and addresses are A21~A0
- Write mode when V_{IH} is inputted to CIOF, and addresses are A20~A0
- Valid addresses are A10~A0 when a command is entered.

- | | |
|---|---|
| (1) RA: Read Address | (6) PA: Program Address |
| (2) RD: Read Data | (7) PD: Program Data |
| (3) BK: Bank Address = A20~A15 | (8) BA: Block Address = A20~A12 |
| (4) IA: Bank Address and ID Read Address (A6, A1, A0) | (9) BPA: Block Address and ID Read Address (A6, A1, A0) |
| Bank Address = A20~A15 | Block Address = A20~A12 |
| Manufacturer Code = (0, 0, 0) | ID Read Address = (0, 1, 0) |
| Device Code = (0, 0, 1) | (10) BPD: Verify Data |
| (5) ID: ID Data | (11) CA: CFI Address |
| 0098H - Manufacturer Code | (12) CD: CFI Data |
| 009AH - Device Code (TH50VSF3582AASB) | (13) F0H: 00H is valid too |
| 009CH - Device Code (TH50VSF3583AASB) | |
| 0001H - Protected Block | |

BLOCK ERASE ADDRESS TABLES

TH50VSF3582AASB (top boot block)

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | |
|--------|---------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----------------|------------------|
| | | BANK ADDRESS | | | | | | | | | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | |
| BK0 | BA0 | L | L | L | L | L | L | * | * | * | 000000H~00FFFFH | 000000H~007FFFFH |
| | BA1 | L | L | L | L | L | H | * | * | * | 010000H~01FFFFH | 008000H~00FFFFH |
| | BA2 | L | L | L | L | H | L | * | * | * | 020000H~02FFFFH | 010000H~017FFFFH |
| | BA3 | L | L | L | L | H | H | * | * | * | 030000H~03FFFFH | 018000H~01FFFFH |
| | BA4 | L | L | L | H | L | L | * | * | * | 040000H~04FFFFH | 020000H~027FFFFH |
| | BA5 | L | L | L | H | L | H | * | * | * | 050000H~05FFFFH | 028000H~02FFFFH |
| | BA6 | L | L | L | H | H | L | * | * | * | 060000H~06FFFFH | 030000H~037FFFFH |
| BK1 | BA7 | L | L | L | H | H | H | * | * | * | 070000H~07FFFFH | 038000H~03FFFFH |
| | BA8 | L | L | H | L | L | L | * | * | * | 080000H~08FFFFH | 040000H~047FFFFH |
| | BA9 | L | L | H | L | L | H | * | * | * | 090000H~09FFFFH | 048000H~04FFFFH |
| | BA10 | L | L | H | L | H | L | * | * | * | 0A0000H~0AFFFFH | 050000H~057FFFFH |
| | BA11 | L | L | H | L | H | H | * | * | * | 0B0000H~0BFFFFH | 058000H~05FFFFH |
| | BA12 | L | L | H | H | L | L | * | * | * | 0C0000H~0CFFFFH | 060000H~067FFFFH |
| | BA13 | L | L | H | H | L | H | * | * | * | 0D0000H~0DFFFFH | 068000H~06FFFFH |
| BK2 | BA14 | L | L | H | H | H | L | * | * | * | 0E0000H~0EFFFFH | 070000H~077FFFFH |
| | BA15 | L | L | H | H | H | H | * | * | * | 0F0000H~0FFFFFH | 078000H~07FFFFH |
| | BA16 | L | H | L | L | L | L | * | * | * | 100000H~10FFFFH | 080000H~087FFFFH |
| | BA17 | L | H | L | L | L | H | * | * | * | 110000H~11FFFFH | 088000H~08FFFFH |
| | BA18 | L | H | L | L | H | L | * | * | * | 120000H~12FFFFH | 090000H~097FFFFH |
| | BA19 | L | H | L | L | H | H | * | * | * | 130000H~13FFFFH | 098000H~09FFFFH |
| | BA20 | L | H | L | H | L | L | * | * | * | 140000H~14FFFFH | 0A0000H~0A7FFFFH |
| BK3 | BA21 | L | H | L | H | L | H | * | * | * | 150000H~15FFFFH | 0A8000H~0AFFFFH |
| | BA22 | L | H | L | H | H | L | * | * | * | 160000H~16FFFFH | 0B0000H~0B7FFFFH |
| | BA23 | L | H | L | H | H | H | * | * | * | 170000H~17FFFFH | 0B8000H~0BFFFFH |
| | BA24 | L | H | H | L | L | L | * | * | * | 180000H~18FFFFH | 0C0000H~0C7FFFFH |
| | BA25 | L | H | H | L | L | H | * | * | * | 190000H~19FFFFH | 0C8000H~0CFFFFH |
| | BA26 | L | H | H | L | H | L | * | * | * | 1A0000H~1AFFFFH | 0D0000H~0D7FFFFH |
| | BA27 | L | H | H | L | H | H | * | * | * | 1B0000H~1BFFFFH | 0D8000H~0DFFFFH |
| BK3 | BA28 | L | H | H | H | L | L | * | * | * | 1C0000H~1CFFFFH | 0E0000H~0E7FFFFH |
| | BA29 | L | H | H | H | L | H | * | * | * | 1D0000H~1DFFFFH | 0E8000H~0EFFFFH |
| | BA30 | L | H | H | H | H | L | * | * | * | 1E0000H~1EFFFFH | 0F0000H~0F7FFFFH |
| | BA31 | L | H | H | H | H | H | * | * | * | 1F0000H~1FFFFFH | 0F8000H~0FFFFFH |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|-----------------|-----------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK4 | BA32 | H | L | L | L | L | L | * | * | * | 200000H~20FFFFH | 100000H~107FFFH | |
| | BA33 | H | L | L | L | L | H | * | * | * | 210000H~21FFFFH | 108000H~10FFFFH | |
| | BA34 | H | L | L | L | H | L | * | * | * | 220000H~22FFFFH | 110000H~117FFFH | |
| | BA35 | H | L | L | L | H | H | * | * | * | 230000H~23FFFFH | 118000H~11FFFFH | |
| | BA36 | H | L | L | H | L | L | * | * | * | 240000H~24FFFFH | 120000H~127FFFH | |
| | BA37 | H | L | L | H | L | H | * | * | * | 250000H~25FFFFH | 128000H~12FFFFH | |
| | BA38 | H | L | L | H | H | L | * | * | * | 260000H~26FFFFH | 130000H~137FFFH | |
| | BA39 | H | L | L | H | H | H | * | * | * | 270000H~27FFFFH | 138000H~13FFFFH | |
| BK5 | BA40 | H | L | H | L | L | L | * | * | * | 280000H~28FFFFH | 140000H~147FFFH | |
| | BA41 | H | L | H | L | L | H | * | * | * | 290000H~29FFFFH | 148000H~14FFFFH | |
| | BA42 | H | L | H | L | H | L | * | * | * | 2A0000H~2AFFFFH | 150000H~157FFFH | |
| | BA43 | H | L | H | L | H | H | * | * | * | 2B0000H~2BFFFFH | 158000H~15FFFFH | |
| | BA44 | H | L | H | H | L | L | * | * | * | 2C0000H~2CFFFFH | 160000H~167FFFH | |
| | BA45 | H | L | H | H | L | H | * | * | * | 2D0000H~2DFFFFH | 168000H~16FFFFH | |
| | BA46 | H | L | H | H | H | L | * | * | * | 2E0000H~2EFFFFH | 170000H~177FFFH | |
| | BA47 | H | L | H | H | H | H | * | * | * | 2F0000H~2FFFFFH | 178000H~17FFFFH | |
| BK6 | BA48 | H | H | L | L | L | L | * | * | * | 300000H~30FFFFH | 180000H~187FFFH | |
| | BA49 | H | H | L | L | L | H | * | * | * | 310000H~31FFFFH | 188000H~18FFFFH | |
| | BA50 | H | H | L | L | H | L | * | * | * | 320000H~32FFFFH | 190000H~197FFFH | |
| | BA51 | H | H | L | L | H | H | * | * | * | 330000H~33FFFFH | 198000H~19FFFFH | |
| | BA52 | H | H | L | H | L | L | * | * | * | 340000H~34FFFFH | 1A0000H~1A7FFFH | |
| | BA53 | H | H | L | H | L | H | * | * | * | 350000H~35FFFFH | 1A8000H~1AFFFFH | |
| | BA54 | H | H | L | H | H | L | * | * | * | 360000H~36FFFFH | 1B0000H~1B7FFFH | |
| | BA55 | H | H | L | H | H | H | * | * | * | 370000H~37FFFFH | 1B8000H~1BFFFFH | |
| BK7 | BA56 | H | H | H | L | L | L | * | * | * | 380000H~38FFFFH | 1C0000H~1C7FFFH | |
| | BA57 | H | H | H | L | L | H | * | * | * | 390000H~39FFFFH | 1C8000H~1CFFFFH | |
| | BA58 | H | H | H | L | H | L | * | * | * | 3A0000H~3AFFFFH | 1D0000H~1D7FFFH | |
| | BA59 | H | H | H | L | H | H | * | * | * | 3B0000H~3BFFFFH | 1D8000H~1DFFFFH | |
| | BA60 | H | H | H | H | L | L | * | * | * | 3C0000H~3CFFFFH | 1E0000H~1E7FFFH | |
| | BA61 | H | H | H | H | L | H | * | * | * | 3D0000H~3DFFFFH | 1E8000H~1EFFFFH | |
| | BA62 | H | H | H | H | H | L | * | * | * | 3E0000H~3EFFFFH | 1F0000H~1F7FFFH | |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|------------------|------------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK8 | BA63 | H | H | H | H | H | H | L | L | L | 3F0000H~3F1FFFFH | 1F8000H~1F8FFFFH | |
| | BA64 | H | H | H | H | H | H | L | L | H | 3F2000H~3F3FFFFH | 1F9000H~1F9FFFFH | |
| | BA65 | H | H | H | H | H | H | L | H | L | 3F4000H~3F5FFFFH | 1FA000H~1FAFFFFH | |
| | BA66 | H | H | H | H | H | H | L | H | H | 3F6000H~3F7FFFFH | 1FB000H~1FBFFFFH | |
| | BA67 | H | H | H | H | H | H | H | L | L | 3F8000H~3F9FFFFH | 1FC000H~1FCFFFFH | |
| | BA68 | H | H | H | H | H | H | H | L | H | 3FA000H~3FBFFFFH | 1FD000H~1FDFFFFH | |
| | BA69 | H | H | H | H | H | H | H | H | L | 3FC000H~3FDFFFFH | 1FE000H~1FEFFFFH | |
| | BA70 | H | H | H | H | H | H | H | H | H | 3FE000H~3FFFFFFH | 1FF000H~1FFFFFFH | |

TH50VSF3583AASB (bottom boot block)

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | |
|--------|---------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-------------------|-------------------|
| | | BANK ADDRESS | | | | | | | | | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | | |
| BK0 | BA0 | L | L | L | L | L | L | L | L | L | 000000H~001FFFFH | 000000H~000FFFFH |
| | BA1 | L | L | L | L | L | L | L | L | H | 002000H~003FFFFH | 001000H~001FFFFH |
| | BA2 | L | L | L | L | L | L | L | H | L | 004000H~005FFFFH | 002000H~002FFFFH |
| | BA3 | L | L | L | L | L | L | L | H | H | 006000H~007FFFFH | 003000H~003FFFFH |
| | BA4 | L | L | L | L | L | L | H | L | L | 008000H~009FFFFH | 004000H~004FFFFH |
| | BA5 | L | L | L | L | L | L | H | L | H | 00A000H~00BFFFFH | 005000H~005FFFFH |
| | BA6 | L | L | L | L | L | L | H | H | L | 00C000H~00DFFFFH | 006000H~006FFFFH |
| | BA7 | L | L | L | L | L | L | H | H | H | 00E000H~00FFFFFFH | 007000H~007FFFFH |
| BK1 | BA8 | L | L | L | L | L | H | * | * | * | 010000H~01FFFFFFH | 008000H~00FFFFFFH |
| | BA9 | L | L | L | L | H | L | * | * | * | 020000H~02FFFFFFH | 010000H~017FFFFH |
| | BA10 | L | L | L | L | H | H | * | * | * | 030000H~03FFFFFFH | 018000H~01FFFFFFH |
| | BA11 | L | L | L | H | L | L | * | * | * | 040000H~04FFFFFFH | 020000H~027FFFFH |
| | BA12 | L | L | L | H | L | H | * | * | * | 050000H~05FFFFFFH | 028000H~02FFFFFFH |
| | BA13 | L | L | L | H | H | L | * | * | * | 060000H~06FFFFFFH | 030000H~037FFFFH |
| | BA14 | L | L | L | H | H | H | * | * | * | 070000H~07FFFFFFH | 038000H~03FFFFFFH |
| BK2 | BA15 | L | L | H | L | L | L | * | * | * | 080000H~08FFFFFFH | 040000H~047FFFFH |
| | BA16 | L | L | H | L | L | H | * | * | * | 090000H~09FFFFFFH | 048000H~04FFFFFFH |
| | BA17 | L | L | H | L | H | L | * | * | * | 0A0000H~0AFFFFFFH | 050000H~057FFFFH |
| | BA18 | L | L | H | L | H | H | * | * | * | 0B0000H~0BFFFFFFH | 058000H~05FFFFFFH |
| | BA19 | L | L | H | H | L | L | * | * | * | 0C0000H~0CFFFFFFH | 060000H~067FFFFH |
| | BA20 | L | L | H | H | L | H | * | * | * | 0D0000H~0DFFFFFFH | 068000H~06FFFFFFH |
| | BA21 | L | L | H | H | H | L | * | * | * | 0E0000H~0EFFFFFFH | 070000H~077FFFFH |
| | BA22 | L | L | H | H | H | H | * | * | * | 0F0000H~0FFFFFFFH | 078000H~07FFFFFFH |
| BK3 | BA23 | L | H | L | L | L | L | * | * | * | 100000H~10FFFFFFH | 080000H~087FFFFH |
| | BA24 | L | H | L | L | L | H | * | * | * | 110000H~11FFFFFFH | 088000H~08FFFFFFH |
| | BA25 | L | H | L | L | H | L | * | * | * | 120000H~12FFFFFFH | 090000H~097FFFFH |
| | BA26 | L | H | L | L | H | H | * | * | * | 130000H~13FFFFFFH | 098000H~09FFFFFFH |
| | BA27 | L | H | L | H | L | L | * | * | * | 140000H~14FFFFFFH | 0A0000H~0A7FFFFH |
| | BA28 | L | H | L | H | L | H | * | * | * | 150000H~15FFFFFFH | 0A8000H~0AFFFFFFH |
| | BA29 | L | H | L | H | H | L | * | * | * | 160000H~16FFFFFFH | 0B0000H~0B7FFFFH |
| | BA30 | L | H | L | H | H | H | * | * | * | 170000H~17FFFFFFH | 0B8000H~0BFFFFFFH |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|-----------------|------------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK4 | BA31 | L | H | H | L | L | L | * | * | * | 180000H~18FFFFH | 0C0000H~0C7FFFFH | |
| | BA32 | L | H | H | L | L | H | * | * | * | 190000H~19FFFFH | 0C8000H~0CFFFFH | |
| | BA33 | L | H | H | L | H | L | * | * | * | 1A0000H~1AFFFFH | 0D0000H~0D7FFFFH | |
| | BA34 | L | H | H | L | H | H | * | * | * | 1B0000H~1BFFFFH | 0D8000H~0DFFFFH | |
| | BA35 | L | H | H | H | L | L | * | * | * | 1C0000H~1CFFFFH | 0E0000H~0E7FFFFH | |
| | BA36 | L | H | H | H | L | H | * | * | * | 1D0000H~1DFFFFH | 0E8000H~0EFFFFH | |
| | BA37 | L | H | H | H | H | L | * | * | * | 1E0000H~1EFFFFH | 0F0000H~0F7FFFFH | |
| | BA38 | L | H | H | H | H | H | * | * | * | 1F0000H~1FFFFFH | 0F8000H~0FFFFFH | |
| BK5 | BA39 | H | L | L | L | L | L | * | * | * | 200000H~20FFFFH | 100000H~107FFFFH | |
| | BA40 | H | L | L | L | L | H | * | * | * | 210000H~21FFFFH | 108000H~10FFFFH | |
| | BA41 | H | L | L | L | H | L | * | * | * | 220000H~22FFFFH | 110000H~117FFFFH | |
| | BA42 | H | L | L | L | H | H | * | * | * | 230000H~23FFFFH | 118000H~11FFFFH | |
| | BA43 | H | L | L | H | L | L | * | * | * | 240000H~24FFFFH | 120000H~127FFFFH | |
| | BA44 | H | L | L | H | L | H | * | * | * | 250000H~25FFFFH | 128000H~12FFFFH | |
| | BA45 | H | L | L | H | H | L | * | * | * | 260000H~26FFFFH | 130000H~137FFFFH | |
| | BA46 | H | L | L | H | H | H | * | * | * | 270000H~27FFFFH | 138000H~13FFFFH | |
| BK6 | BA47 | H | L | H | L | L | L | * | * | * | 280000H~28FFFFH | 140000H~147FFFFH | |
| | BA48 | H | L | H | L | L | H | * | * | * | 290000H~29FFFFH | 148000H~14FFFFH | |
| | BA49 | H | L | H | L | H | L | * | * | * | 2A0000H~2AFFFFH | 150000H~157FFFFH | |
| | BA50 | H | L | H | L | H | H | * | * | * | 2B0000H~2BFFFFH | 158000H~15FFFFH | |
| | BA51 | H | L | H | H | L | L | * | * | * | 2C0000H~2CFFFFH | 160000H~167FFFFH | |
| | BA52 | H | L | H | H | L | H | * | * | * | 2D0000H~2DFFFFH | 168000H~16FFFFH | |
| | BA53 | H | L | H | H | H | L | * | * | * | 2E0000H~2EFFFFH | 170000H~177FFFFH | |
| | BA54 | H | L | H | H | H | H | * | * | * | 2F0000H~2FFFFFH | 178000H~17FFFFH | |
| BK7 | BA55 | H | H | L | L | L | L | * | * | * | 300000H~30FFFFH | 180000H~187FFFFH | |
| | BA56 | H | H | L | L | L | H | * | * | * | 310000H~31FFFFH | 188000H~18FFFFH | |
| | BA57 | H | H | L | L | H | L | * | * | * | 320000H~32FFFFH | 190000H~197FFFFH | |
| | BA58 | H | H | L | L | H | H | * | * | * | 330000H~33FFFFH | 198000H~19FFFFH | |
| | BA59 | H | H | L | H | L | L | * | * | * | 340000H~34FFFFH | 1A0000H~1A7FFFFH | |
| | BA60 | H | H | L | H | L | H | * | * | * | 350000H~35FFFFH | 1A8000H~1AFFFFH | |
| | BA61 | H | H | L | H | H | L | * | * | * | 360000H~36FFFFH | 1B0000H~1B7FFFFH | |
| | BA62 | H | H | L | H | H | H | * | * | * | 370000H~37FFFFH | 1B8000H~1BFFFFH | |

| BANK # | BLOCK # | BLOCK ADDRESS | | | | | | | | | ADDRESS RANGE | | |
|--------|---------|---------------|-----|-----|-----|-----|-----|---|-----|-----|-----------------|-----------------|-----------|
| | | BANK ADDRESS | | | | | | | A14 | A13 | A12 | BYTE MODE | WORD MODE |
| | | A20 | A19 | A18 | A17 | A16 | A15 | | | | | | |
| BK8 | BA63 | H | H | H | L | L | L | * | * | * | 380000H~38FFFFH | 1C0000H~1C7FFFH | |
| | BA64 | H | H | H | L | L | H | * | * | * | 390000H~39FFFFH | 1C8000H~1CFFFFH | |
| | BA65 | H | H | H | L | H | L | * | * | * | 3A0000H~3AFFFFH | 1D0000H~1D7FFFH | |
| | BA66 | H | H | H | L | H | H | * | * | * | 3B0000H~3BFFFFH | 1D8000H~1DFFFFH | |
| | BA67 | H | H | H | H | L | L | * | * | * | 3C0000H~3CFFFFH | 1E0000H~1E7FFFH | |
| | BA68 | H | H | H | H | L | H | * | * | * | 3D0000H~3DFFFFH | 1E8000H~1EFFFFH | |
| | BA69 | H | H | H | H | H | L | * | * | * | 3E0000H~3EFFFFH | 1F0000H~1F7FFFH | |
| | BA70 | H | H | H | H | H | H | * | * | * | 3F0000H~3FFFFFH | 1F8000H~1FFFFFH | |

BLOCK SIZE TABLE**TH50VSF3582AASB (top boot block)**

| BLOCK # | BLOCK SIZE | | BANK # | BANK SIZE | | BLOCK COUNT |
|-----------|------------|-----------|--------|------------|------------|-------------|
| | BYTE MODE | WORD MODE | | BYTE MODE | WORD MODE | |
| BA0~BA7 | 64 Kbytes | 32 Kwords | BK0 | 512 Kbytes | 256 Kwords | 8 |
| BA8~BA15 | 64 Kbytes | 32 Kwords | BK1 | 512 Kbytes | 256 Kwords | 8 |
| BA16~BA23 | 64 Kbytes | 32 Kwords | BK2 | 512 Kbytes | 256 Kwords | 8 |
| BA24~BA31 | 64 Kbytes | 32 Kwords | BK3 | 512 Kbytes | 256 Kwords | 8 |
| BA32~BA39 | 64 Kbytes | 32 Kwords | BK4 | 512 Kbytes | 256 Kwords | 8 |
| BA40~BA47 | 64 Kbytes | 32 Kwords | BK5 | 512 Kbytes | 256 Kwords | 8 |
| BA48~BA55 | 64 Kbytes | 32 Kwords | BK6 | 512 Kbytes | 256 Kwords | 8 |
| BA56~BA62 | 64 Kbytes | 32 Kwords | BK7 | 448 Kbytes | 224 Kwords | 7 |
| BA63~BA70 | 8 Kbytes | 4 Kwords | BK8 | 64 Kbytes | 32 Kwords | 8 |

TH50VSF3583AASB (bottom boot block)

| BLOCK # | BLOCK SIZE | | BANK # | BANK SIZE | | BLOCK COUNT |
|-----------|------------|-----------|--------|------------|------------|-------------|
| | BYTE MODE | WORD MODE | | BYTE MODE | WORD MODE | |
| BA0~BA7 | 8 Kbytes | 4 Kwords | BK0 | 64 Kbytes | 32 Kwords | 8 |
| BA8~BA14 | 64 Kbytes | 32 Kwords | BK1 | 448 Kbytes | 224 Kwords | 7 |
| BA15~BA22 | 64 Kbytes | 32 Kwords | BK2 | 512 Kbytes | 256 Kwords | 8 |
| BA23~BA30 | 64 Kbytes | 32 Kwords | BK3 | 512 Kbytes | 256 Kwords | 8 |
| BA31~BA38 | 64 Kbytes | 32 Kwords | BK4 | 512 Kbytes | 256 Kwords | 8 |
| BA39~BA46 | 64 Kbytes | 32 Kwords | BK5 | 512 Kbytes | 256 Kwords | 8 |
| BA47~BA54 | 64 Kbytes | 32 Kwords | BK6 | 512 Kbytes | 256 Kwords | 8 |
| BA55~BA62 | 64 Kbytes | 32 Kwords | BK7 | 512 Kbytes | 256 Kwords | 8 |
| BA63~BA70 | 64 Kbytes | 32 Kwords | BK8 | 512 Kbytes | 256 Kwords | 8 |

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RANGE | UNIT |
|---------------------|---|------------------------------------|-------|
| V _{CC} | V _{CCs} /V _{CCf} Supply Voltage | -0.3~4.2 | V |
| V _{IN} | Input Voltage ⁽¹⁾ | -0.3~4.2 | V |
| V _{DQ} | Input/Output Voltage | -0.5~V _{CC} + 0.5 (≤ 4.2) | V |
| T _{opr} | Operating Temperature | -30~85 | °C |
| P _D | Power Dissipation | 0.6 | W |
| T _{solder} | Soldering Temperature (10 s) | 260 | °C |
| I _{OSHORT} | Output Short Circuit Current ⁽²⁾ | 100 | mA |
| N _{EW} | Erase/Program Cycling Capability | 100,000 | Cycle |
| T _{stg} | Storage Temperature | -55~125 | °C |

(1) -2.0 V for pulse width ≤ 20 ns

(2) Output shorted for no more than one second. No more than one output shorted at a time

HARDWARE STATUS FLAGS

| STATUS | | | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 | RY/BY | |
|---------------------|--|-----------------|-----------------------------|-------------------------|--------|------|------|--------|------|
| In Progress | Auto Programming | | $\overline{\text{DQ7}}$ | Toggle | 0 | 0 | 1 | 0 | |
| | Read in Program Suspend ⁽¹⁾ | | Data | Data | Data | Data | Data | Hi-Z | |
| | In Auto-Erase | Erase Hold Time | Selected ⁽²⁾ | 0 | Toggle | 0 | 0 | Toggle | 0 |
| | | | Non-Selected ⁽³⁾ | 0 | Toggle | 0 | 0 | 1 | 0 |
| | | Auto-Erase | Selected | 0 | Toggle | 0 | 1 | Toggle | 0 |
| | | | Non-Selected | 0 | Toggle | 0 | 1 | 1 | 0 |
| | In Erase Suspend | Read | Selected | 1 | 1 | 0 | 0 | Toggle | Hi-Z |
| | | | Non-Selected | Data | Data | Data | Data | Data | Hi-Z |
| | | Programming | Selected | $\overline{\text{DQ7}}$ | Toggle | 0 | 0 | Toggle | 0 |
| | | | Non-Selected | $\overline{\text{DQ7}}$ | Toggle | 0 | 0 | 1 | 0 |
| Time Limit Exceeded | Auto Programming | | $\overline{\text{DQ7}}$ | Toggle | 1 | 0 | 1 | 0 | |
| | Auto-Erase | | 0 | Toggle | 1 | 1 | N/A | 0 | |
| | Programming in Erase Suspend | | $\overline{\text{DQ7}}$ | Toggle | 1 | 0 | N/A | 0 | |

Notes: DQ outputs cell data and RY/BY to high impedance when the operation has completed.

DQ0 and DQ1 pins are reserved for future use.

DQ0, DQ1 and DQ4 output 0.

(1) Data output from an address to which Write is being performed are undefined.

(2) Output when the block address selected for Auto Block Erase is specified and data is read from there.

During Auto Chip Erase, all blocks are selected.

(3) Output when a block address not selected for Auto Block Erase of same bank as selected block is specified and data is read from there.

RECOMMENDED DC OPERATING CONDITIONS (Ta = -30°~85°C)

| SYMBOL | PARAMETER | MIN | TYP. | MAX | UNIT |
|------------------------------------|--------------------------------------|---------------------|------|-----------------------|------|
| V _{CCs} /V _{CCf} | Power Supply Voltage | 2.67 | — | 3.3 | V |
| V _{IH} | Input High-Level Voltage | 2.2 | — | V _{CC} + 0.3 | |
| V _{IL} | Input Low-Level Voltage | -0.3 ⁽¹⁾ | — | V _{CC} × 0.2 | |
| V _{DH} | Data Retention Voltage for SRAM | 1.5 | — | 3.3 | |
| V _{LKO} | Flash Low-Lock Voltage | 2.3 | — | 2.5 | |
| V _{ACC} | High Voltage for $\overline{WP/ACC}$ | 8.5 | — | 9.5 | |
| V _{ID} | High Voltage for \overline{RESET} | 11.4 | — | 12.6 | |

(1) -2.0 V for pulse width ≤ 20 ns

CAPACITANCE (Ta = 25°C, f = 1 MHz)

| SYMBOL | PARAMETER | CONDITION | MIN | TYP. | MAX | UNIT |
|------------------|--------------------|------------------------|-----|------|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = GND | — | — | 15 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = GND | — | — | 20 | pF |

Note: These parameters are sampled periodically and are not tested for every device.

DC CHARACTERISTICS (Ta = -30°~85°C, VCCs/VCCf = 2.67 V~3.3 V)

| SYMBOL | PARAMETER | CONDITION | MIN | TYP. | MAX | UNIT | | |
|-------------------|--|---|--------------------------------------|---------------|-----|------|------|-----|
| I _{IL} | Input Leakage Current | V _{IN} = 0 V~V _{CC} | — | — | ±1 | μA | | |
| I _{ILW} | Input Leakage Current (WP/ACC pin) | 0 V ≤ V _{IN} ≤ V _{CC} | — | — | ±10 | μA | | |
| I _{SOH} | SRAM Output High Current | V _{OH} = V _{CCs} - 0.5 V | -0.5 | — | — | mA | | |
| I _{SOL} | SRAM Output Low Current | V _{OL} = 0.4 V | 2.1 | — | — | mA | | |
| I _{FOH1} | Flash Output High Current (TTL) | V _{OH} = 2.4 V | -0.4 | — | — | mA | | |
| I _{FOH2} | Flash Output High Current (CMOS) | V _{OH} = V _{CCf} × 0.85 | -2.5 | — | — | mA | | |
| | | V _{OH} = V _{CCf} - 0.4 V | -100 | — | — | μA | | |
| I _{FOL} | Flash Output Low Current | V _{OL} = 0.4 V | 4 | — | — | mA | | |
| I _{LO} | Output Leakage Current | V _{OUT} = 0 V~V _{CC} , $\overline{OE} = V_{IH}$ | — | — | ±1 | μA | | |
| I _{CCO1} | Flash Average Read Current | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, I _{OUT} = 0 mA, t _{cycle} = t _{RC} (min) | — | — | 30 | mA | | |
| I _{CCO2} | Flash Average Program/Erase Current | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, I _{OUT} = 0 mA | — | — | 15 | mA | | |
| I _{CCO3} | SRAM Average Operating Current | $\overline{CE1S} = V_{IL}$, CE2S = V _{IH} , $\overline{OE} = V_{IH}$, I _{OUT} = 0 mA | t _{cycle} = t _{RC} | — | — | 50 | mA | |
| | | | t _{cycle} = 1 MHz | — | — | 10 | | |
| I _{CCO4} | | $\overline{CE1S} = 0.2 V$, $\overline{OE} = V_{CCs} - 0.2 V$, CE2S = V _{CCs} - 0.2 V, I _{OUT} = 0 mA | t _{cycle} = t _{RC} | — | — | 45 | mA | |
| | | | t _{cycle} = 1 MHz | — | — | 5 | | |
| I _{CCO5} | Flash Average Read-While-Program Current | V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0 mA, t _{cycle} = t _{RC} (min) | — | — | 45 | mA | | |
| I _{CCO6} | Flash Average Read-While-Erase Current | V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0 mA, t _{cycle} = t _{RC} (min) | — | — | 45 | mA | | |
| I _{CCO7} | Flash Average Program-While-Erase-Suspend Current | V _{IN} = V _{IH} /V _{IL} , I _{OUT} = 0 mA | — | — | 15 | mA | | |
| I _{CCS1} | Flash Standby Current | $\overline{CE} = \overline{RESET} = V_{CCf}$ or $\overline{RESET} = V_{SS}$ | — | — | 10 | μA | | |
| I _{CCS2} | Flash Standby Current (Automatic Sleep Mode ⁽¹⁾) | V _{IH} = V _{CCf} or V _{IL} = V _{SS} | — | — | 10 | μA | | |
| I _{CCS3} | SRAM Standby Current | $\overline{CE1S} = V_{IH}$ or CE2S = V _{IL} | — | — | 2 | mA | | |
| I _{CCS4} | | $\overline{CE1S} = V_{CCs} - 0.2 V$ or CE2S = 0.2 V ⁽²⁾ | V _{CCs} = 3.3 V | Ta = 25°C | — | | — | 1 |
| | | | | Ta = -30~85°C | — | | — | 10 |
| | | | V _{CCs} = 3.0 V | Ta = 25°C | — | | 0.01 | 0.5 |
| | | | | Ta = -30~40°C | — | | — | 1 |
| Ta = -30~85°C | — | — | 5 | | | | | |
| I _{ACC} | High Voltage Input Current for WP/ACC | 8.5 V ≤ V _{ACC} ≤ 9.5 V | — | — | 20 | mA | | |

(1) The device is going to Automatic Sleep Mode, when address remain steady during 150 ns.

(2) In Standby Mode, with $\overline{CE1S} \geq V_{CCs} - 0.2 V$, these limits are guaranteed when CE2S ≥ V_{CCs} - 0.2 V or CE2S ≤ 0.2 V and CIOs ≥ V_{CCs} - 0.2 V or CIOs ≤ 0.2 V.

AC CHARACTERISTICS (SRAM) (Ta = -40°~85°C, VCCs = 2.7 V~3.6 V)

Read cycle

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|------------------|--|-----|-----|------|
| t _{RC} | Read Cycle Time | 70 | — | ns |
| t _{ACC} | Address Access Time | — | 70 | |
| t _{CO1} | Chip Enable (CE1S) Access Time | — | 70 | |
| t _{CO2} | Chip Enable (CE2S) Access Time | — | 70 | |
| t _{OE} | Output Enable Access Time | — | 35 | |
| t _{BA} | Data Byte Control Access Time | — | 35 | |
| t _{COE} | Chip Enable Low to Output Active | 5 | — | |
| t _{OEE} | Output Enable Low to Output Active | 0 | — | |
| t _{BE} | Data Byte Control Low to Output Active | 0 | — | |
| t _{OD} | Chip Enable High to Output Hi-Z | — | 30 | |
| t _{ODO} | Output Enable High to Output Hi-Z | — | 30 | |
| t _{BD} | Data Byte Control High to Output Hi-Z | — | 30 | |
| t _{OH} | Output Data Hold Time | 10 | — | |
| t _{CCR} | CE Recovery Time | 0 | — | |

Write cycle

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|------------------|---------------------------------------|-----|-----|------|
| t _{WC} | Write Cycle Time | 70 | — | ns |
| t _{WP} | Write Pulse Width | 50 | — | |
| t _{CW} | Chip Enable to End of Write | 60 | — | |
| t _{BW} | Data Byte Control to End of Write | 50 | — | |
| t _{AS} | Address Set-up Time | 0 | — | |
| t _{WR} | Write Recovery Time | 0 | — | |
| t _{ODW} | \overline{WE} Low to Output Hi-Z | — | 30 | |
| t _{OEW} | \overline{WE} High to Output Active | 0 | — | |
| t _{DS} | Data Set-up Time | 30 | — | |
| t _{DH} | Data Hold Time | 0 | — | |

AC TEST CONDITIONS

| PARAMETER | VALUES |
|---|--------------------------------------|
| Input Pulse Level | 0.4 V, 2.4 V |
| Input Pulse Rise and Fall Time (10%~90%) | 5 ns |
| Timing Measurement Reference Level (input) | V _{CCs} × 0.5 |
| Timing Measurement Reference Level (output) | V _{CCs} × 0.5 |
| Output Load | C _L (100 pF) + 1 TTL gate |

AC CHARACTERISTICS (FLASH MEMORY)

READ CYCLE

| SYMBOL | PARAMETER | LOAD CAPACITANCE | | | | UNIT |
|------------------|---|------------------|-----|-------|-----|------|
| | | 30pF | | 100pF | | |
| | | MIN | MAX | MIN | MAX | |
| t _{RC} | Read Cycle Time | 70 | — | — | 80 | ns |
| t _{ACC} | Address Access Time | — | 70 | — | 80 | ns |
| t _{CE} | $\overline{\text{CE}}\overline{\text{F}}$ Access Time | — | 70 | — | 80 | ns |
| t _{OE} | $\overline{\text{OE}}$ Access Time | — | 30 | — | 35 | ns |
| t _{CEE} | $\overline{\text{CE}}\overline{\text{F}}$ to Output Low-Z | 0 | — | 0 | — | ns |
| t _{OEE} | $\overline{\text{OE}}$ to Output Low-Z | 0 | — | 0 | — | ns |
| t _{OEH} | $\overline{\text{OE}}$ Hold Time | 0 | — | 0 | — | ns |
| t _{OH} | Output Data Hold Time | 0 | — | 0 | — | ns |
| t _{DF1} | $\overline{\text{CE}}\overline{\text{F}}$ to Output Hi-Z | — | 30 | — | 25 | ns |
| t _{DF2} | $\overline{\text{OE}}$ to Output Hi-Z | — | 20 | — | 25 | ns |

BLOCK PROTECT

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-------------------|---|-----|-----|------|
| t _{VPS} | V _{ID} Set-up Time | 4 | — | μs |
| t _{CESP} | $\overline{\text{CE}}\overline{\text{F}}$ Set-up Time | 4 | — | μs |
| t _{VPH} | $\overline{\text{OE}}$ Hold Time | 4 | — | μs |
| t _{PPLH} | $\overline{\text{WE}}$ Low-Level Hold Time | 100 | — | μs |

PROGRAM AND ERASE CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-------------------|-------------------------------|-----------------|-----|--------|
| t _{PPW} | Auto-Program Time (Byte Mode) | 8* | 300 | μs |
| | Auto-Program Time (Word Mode) | 11* | 300 | μs |
| t _{PCEW} | Auto Chip Erase Time | 50* | 710 | s |
| t _{PBEW} | Auto Block Erase Time | 0.7* | 10 | s |
| t _{EW} | Erase/Program Cycle | 10 ⁵ | — | Cycles |

*: typ.

COMMAND WRITE/PROGRAM/ERASE CYCLE

| SYMBOL | PARAMETER | LOAD CAPACITANCE | | | | UNIT |
|--------------------|---|------------------|-----|-------|-----|------|
| | | 30pF | | 100pF | | |
| | | MIN | MAX | MIN | MAX | |
| t _{CMD} | Command Write Cycle Time | 70 | — | 80 | — | ns |
| t _{AS} | Address Set-up Time / $\overline{\text{BYTE}}$ Set-up Time | 0 | — | 0 | — | ns |
| t _{AH} | Address Hold Time / $\overline{\text{BYTE}}$ Hold Time | 40 | — | 40 | — | ns |
| t _{AHW} | Address Hold Time from $\overline{\text{WE}}$ High level | 20 | — | 20 | — | ns |
| t _{DS} | Data Set-up Time | 40 | — | 40 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | ns |
| t _{WELH} | $\overline{\text{WE}}$ Low-Level Hold Time ($\overline{\text{WE}}$ Control) | 40 | — | 40 | — | ns |
| t _{WEHH} | $\overline{\text{WE}}$ High-Level Hold Time ($\overline{\text{WE}}$ Control) | 20 | — | 20 | — | ns |
| t _{CES} | $\overline{\text{CE}}\overline{\text{F}}$ Set-up Time to $\overline{\text{WE}}$ Active ($\overline{\text{WE}}$ Control) | 0 | — | 0 | — | ns |
| t _{CEH} | $\overline{\text{CE}}\overline{\text{F}}$ Hold Time from $\overline{\text{WE}}$ High Level ($\overline{\text{WE}}$ Control) | 0 | — | 0 | — | ns |
| t _{CELH} | $\overline{\text{CE}}\overline{\text{F}}$ Low-Level Hold Time ($\overline{\text{CE}}\overline{\text{F}}$ Control) | 40 | — | 40 | — | ns |
| t _{CEHH} | $\overline{\text{CE}}\overline{\text{F}}$ High-Level Hold Time ($\overline{\text{CE}}\overline{\text{F}}$ Control) | 20 | — | 20 | — | ns |
| t _{WES} | $\overline{\text{WE}}$ Set-up time to $\overline{\text{CE}}\overline{\text{F}}$ Active ($\overline{\text{CE}}\overline{\text{F}}$ Control) | 0 | — | 0 | — | ns |
| t _{WEH} | $\overline{\text{WE}}$ Hold Time from $\overline{\text{CE}}\overline{\text{F}}$ High Level ($\overline{\text{CE}}\overline{\text{F}}$ Control) | 0 | — | 0 | — | ns |
| t _{OES} | $\overline{\text{OE}}$ Set-up Time | 0 | — | 0 | — | ns |
| t _{OEHP} | $\overline{\text{OE}}$ Hold Time (Toggle, Data Polling) | 90 | — | 90 | — | ns |
| t _{OEHT} | $\overline{\text{OE}}$ High-Level Hold Time (Toggle) | 20 | — | 20 | — | ns |
| t _{BEH} | Erase Hold Time | 50 | — | 50 | — | μs |
| t _{VCS} | V _{CCf} Set-up Time | 500 | — | 500 | — | μs |
| t _{BUSY} | Program/Erase Valid to RY/ $\overline{\text{BY}}$ Delay | — | 90 | — | 90 | ns |
| t _{RP} | $\overline{\text{RESET}}$ Low-Level Hold Time | 500 | — | 500 | — | ns |
| t _{READY} | $\overline{\text{RESET}}$ Low-Level to Read Mode | — | 20 | — | 20 | μs |
| t _{RB} | RY/ $\overline{\text{BY}}$ Recovery Time | 0 | — | 0 | — | ns |
| t _{RH} | $\overline{\text{RESET}}$ Recovery Time | 50 | — | 50 | — | ns |
| t _{CEBTS} | $\overline{\text{CE}}\overline{\text{F}}$ Set-up time $\overline{\text{BYTE}}$ Transition | 5 | — | 5 | — | ns |
| t _{SUSP} | Program Suspend Command to Suspend Mode | — | 1.5 | — | 1.5 | μs |
| t _{RESP} | Program Resume Command to Program Mode | — | 1 | — | 1 | μs |
| t _{SUSE} | Erase Suspend Command to Suspend Mode | — | 15 | — | 15 | μs |
| t _{RESE} | Erase Resume Command to Erase Mode | — | 1 | — | 1 | μs |

SIMULTANEOUS READ/WRITE OPERATION

The TH50VSF3582/3583AASB features a Simultaneous Read/Write operation. The Simultaneous Read/Write operation enables the device to simultaneously write data to or erase data from a bank while the device reads data from another bank.

The TH50VSF3582/3583AASB has a total of nine banks: 0.5 Mbits × 1 bank, 3.5 Mbits × 1 bank, and 4 Mbits × 7 banks. Banks are switched using bank addresses (A20 to A15). For bank blocks and addresses, refer to the Block Address Table and Block Size Table.

The Simultaneous Read/Write operation cannot perform multiple operations in a bank. The table below shows the operating modes in which simultaneous operation can be performed.

Note that during Auto Program execution or Auto Block Erase operation, the Simultaneous Read/Write operation cannot read data from addresses which are not selected for operation in the same bank. Data from such addresses can be read using the Program Suspend or Erase Suspend function.

SIMULTANEOUS READ/WRITE OPERATION

| ONE BANK STATUS | OTHER BANK STATUS |
|---|-------------------|
| Read mode | Read mode |
| ID Read mode ⁽¹⁾ | |
| Auto Program mode | |
| Fast Program mode ⁽²⁾ | |
| Program Suspend mode | |
| Auto Block Erase mode | |
| Auto Multiple Block Erase mode ⁽³⁾ | |
| Erase Suspend mode | |
| Program Suspend while Erase Suspend | |
| CFI mode | |

(1) Command mode only is valid.

(2) Includes when Acceleration mode is in use.

(3) If the selected bank exists in all banks, simultaneous operation is not supported.

OPERATING MODES

In addition to Read, Write, and Erase modes, the TH50VSF3582/3583AASB features many functions including Block Protect and Data Polling. When using the device, reference the timing charts and flow charts together with the description below.

Read Mode

To read data from the memory cell array, set the device to Read mode. In Read mode, the device can perform high-speed random access as asynchronous ROM.

The device is automatically set to Read mode immediately after power on or after completion of automatic operation. A software reset releases ID Read mode and the lock state when automatic operation ends abnormally, and sets to Read mode. A hardware reset terminates operation of the device and resets to Read mode. When reading the data without changing the address immediately after power on, either input a hardware reset or change $\overline{CE\overline{F}}$ from H to L.

ID Read Mode

ID Read mode is used to read the device maker code and device code. The mode is useful for EPROM programmers to automatically identify the device type.

In this method, simultaneous operation can be performed. Inputting an ID Read command sets the specified bank to ID Read mode. Banks are specified by inputting the bank address (BK) in the third bus write cycle of the command cycle. To read an ID code, the bank address as well as the ID read address must be specified. From address BK + 00 the maker code is output; from address BK + 01 the device code is output. From other banks, data are output from the memory cells. Inputting a Reset command releases ID Read mode and returns the device to Read mode.

Access time in ID Read mode is the same as that in Read mode. For the codes, see the ID Code Table.

Standby Mode

There are two methods of entering Standby mode.

- (1) Control using $\overline{CE\overline{F}}$ and $\overline{RESE\overline{T}}$

When the device is in Read mode, input $V_{DD} \pm 0.3$ V to $\overline{CE\overline{F}}$ and $\overline{RESE\overline{T}}$. The device enters Standby mode and the current becomes standby current (I_{CCS1}). However, if the device is in simultaneous operation, the device does not enter Standby mode but causes the operating current to flow.

- (2) Control using only $\overline{RESE\overline{T}}$

When the device is in Read mode, input $V_{SS} \pm 0.3$ V to $\overline{RESE\overline{T}}$. The device enters Standby mode and the current becomes standby current (I_{CCS1}). Even if the device is in simultaneous operation, this method can terminate the current operation and set the device to Standby mode. This is a hardware reset, described later.

In standby mode, DQ is put in high-impedance state.

Auto Sleep Mode

Function which suppresses power dissipation during read. When address input does not change for 150 ns or longer, the device automatically enters Sleep mode and the current becomes standby current (I_{CCS1}). However, if the device is in simultaneous operation, the device does not enter Standby mode but causes the operating current to flow. Because the output data are latched, data are output in Sleep mode. When the address is changed, Sleep mode is automatically released, outputting data from the changed address.

Output Disable Mode

Inputting V_{IH} to \overline{OE} disables output from the device, setting DQ to high-impedance.

Command Write

The TH50VSF3582/3583AASB utilizes the JEDEC command control standard for a single power supply E²PROM. A Command is executed by inputting an address and data into the Command register. The Command is written by inputting a pulse to \overline{WE} with $\overline{CE\overline{F}} = V_{IL}$ and $\overline{OE} = V_{IH}$ (\overline{WE} control). The command can also be written by inputting a pulse to $\overline{CE\overline{F}}$ with $\overline{WE} = V_{IL}$ ($\overline{CE\overline{F}}$ control). The address is latched on the falling edge of either \overline{WE} or $\overline{CE\overline{F}}$. The data is latched on the rising edge of either \overline{WE} or $\overline{CE\overline{F}}$. DQ0 to DQ7 are valid for data input and DQ8 to DQ15 are ignored.

To cancel input of the command sequence mid-way, use the Reset command. The device resets the Command register and enters Read mode. When an undefined command is input, the Command register is reset and the device enters Read mode.

Software Reset

Apply a software reset by inputting a Read/Reset command. Software reset returns the device from ID Read or CFI mode to Read mode, releases the lock state when automatic operation ends abnormally, or clears the Command register.

Hardware Reset

A hardware reset initializes the device and sets it to Read mode. When a pulse is input to \overline{RESET} for t_{RP} , the device ends the operation in progress and enters Read mode after t_{READY} . Note that if a hardware reset is applied during data overwrite such as a Write or Erase operation, data at that address or block become undefined.

After a hardware reset the device enters Read mode when $\overline{RESET} = V_{IH}$ and Standby mode when $\overline{RESET} = V_{IL}$. The DQ pins are High-Impedance when $\overline{RESET} = V_{IL}$. The Read operation sequence and input of any command are allowed after the device enters Read mode.

Comparison with Software Reset and Hardware Reset

| ACTION | SOFTWARE RESET | HARDWARE RESET |
|--|----------------|----------------|
| Release ID Read or CFI mode | Valid | Valid |
| Clear the Command register | Valid | Valid |
| Release the lock state when automatic operation ends abnormally | Valid | Valid |
| Stop automatic operation in progress | Invalid | Valid |
| All stops of operation other than the above, and return to Read mode | Invalid | Valid |

BYTE/WORD Mode

CIOF is used select Word mode (16 bits) or Byte mode (8 bits) for the TH50VSF3582/3583AASB. When V_{IH} is input to CIOF, the device operates in Word mode. Read data or write commands using DQ0 to DQ15. When V_{IL} is input to CIOF, read data or write commands using DQ0 to DQ7. A12F is used as the lowest address. DQ8 to DQ14 become high-impedance.

Auto-Program Mode

The TH50VSF3582/3583AASB can be programmed in either byte or word units. The Auto Program mode is set using the Program command. The program address is latched on the falling edge of the \overline{WE} signal and data is latched on the rising edge of the fourth bus cycle (with \overline{WE} control). Auto programming starts on the rising edge of the \overline{WE} signal in the fourth bus cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is determined from the Hardware Sequence flag. To read the Hardware Sequence flag, specify the address to which Write is being performed.

During Auto Program execution, a command sequence for the bank on which execution is being performed cannot be received. To terminate execution, use a hardware reset. Note that when the operation is terminated, data cannot be correctly written.

Programming of a protected block is ignored. The device enters Read mode 3 μ s after the rising edge of the \overline{WE} signal in the fourth bus cycle.

If an Auto Program operation fails, the device remains in programming state and does not automatically return to Read mode. The device status can be determined from the setting of the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure. If a programming operation fails, please do not try to use the block which contains the address to which data could not be programmed.

The device allows the programming of memory cells from 1 to 0. The programming of Memory cells from 0 to 1 will fail. At this time, execution of Auto Program fails. This indicates that the failure is due to the usage rather than the device. A cell must be erased to turn it from 0 to 1.

Fast Program Mode

Fast Program is a function which enables execution of the command sequence for the Auto Program in two cycles. In this mode the first two cycles of the command sequence, which normally needs four cycles, are omitted. Write is performed in the remaining two cycles. To execute Fast Program, input the Fast Program set command. Write in this mode uses the Fast Program command but operation is the same as that for ordinary Auto Program. The status of the device can be checked using the hardware sequence flag and read operations can be performed as usual. To exit this mode, the Fast Program Reset command must be input. When the command is input, the device returns to Read mode.

Acceleration Mode

The TH50VSF3582/3583AASB features Acceleration mode for reducing write time. Applying V_{ACC} to \overline{WP} or ACC automatically sets the device to Acceleration mode. In Acceleration mode, Block Protect mode changes to Temporary Block Unprotect mode. Write mode changes to Fast Program mode. Modes are switched by the \overline{WP}/ACC signal; thus, there is no need for a Temporary Block Unprotect operation or for setting or resetting Fast Program mode. Operation of Write is the same as that in Auto Program mode. Releasing V_{ACC} to \overline{WP}/ACC ends Acceleration mode.

Program Suspend / Resume Mode

Program Suspend is used to enable Data Read by suspending Write operation. The device receives a Program Suspend command in Write mode (including Write performed during Erase Suspend) but ignores the command in other modes. At command input, the address of the bank on which Write is being performed must be specified. After command input, the device enters Program Suspend Read mode after tSUSP.

During Program Suspend, Cell Data Read, ID Read and CFI Data Read can be performed. When Data Write is suspended, the address to which Write was being performed becomes undefined. ID Read and CFI Data Read are the same as usual.

After completion of Program Suspend, to return to Write mode, input a Program Resume command. At command input, specify the address of the bank on which Write is being performed. When the ID Read and CFI Data Read functions are used, end the functions before inputting the Resume command. On receiving the Resume command, the device returns to Write mode and resumes output of a Hardware Sequence flag from the bank to which data are being written.

Program Suspend can be run in Fast Program or Acceleration mode. However, note that when running Program Suspend in Acceleration mode, do not release VACC.

Auto Chip Erase Mode

The Auto Chip Erase mode is set using the Chip Erase command. The Auto Chip Erase operation starts on the rising edge of \overline{WE} in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is determined from the Hardware Sequence flag.

Command inputs are ignored during an Auto Chip Erase. The hardware reset allows interruption of an Auto Chip Erase operation. The Auto Chip Erase operation does not complete correctly when interrupted. Hence a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 100 μ s after the rising edge of the \overline{WE} signal in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device remains in, erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

In this case, the block in which a failure occurred cannot be detected. Either terminate device usage, or perform Block Erase for each block, specify the failed block, and stop using it. The host processor must take measures to prevent use of the failed block being used in the future.

Auto Block / Multiple Block Erase Mode

The Auto Block and Multiple Block Erase modes are set using the Block Erase command. The block address is latched on the falling edge of the \overline{WE} signal in the sixth bus cycle. The Block Erase starts as soon as the erase hold time (t_{BEH}) has elapsed after the rising edge of the \overline{WE} signal. To erase multiple blocks, repeat the 6th bus write cycles and input the block addresses and the Auto Block Erase command within the erase hold time (Auto Multiple Block Erase). If a command sequence other than Auto Block Erase or Erase Suspend command is input during the erase hold time, the device resets the Command register and enters Read mode. The erase hold time is valid every \overline{WE} rising edge. Once operation starts, all the memory cells in the block selected in the device are automatically preprogrammed to data 0, erased, and Erase is verified. The device status can be determined from the setting of the Hardware Sequence flag. To read the Hardware Sequence flag, the addresses of blocks on which Auto Erase is being performed must be specified. When the selected blocks exit in all the banks, simultaneous operation cannot be performed.

Commands (except Erase Suspend) are ignored during a Block/Multiple Block Erase operation. The operation can be aborted by a hardware reset. The Auto Erase operation does not complete correctly when aborted, therefore, a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all the selected blocks are protected, the Auto Erase operation is not executed and the device returns to Read mode 100 μ s after the rising edge of the \overline{WE} signal in the last bus cycle.

If an Auto Erase operation fails, the device remains in erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a Hardware reset is necessary to return the device to Read mode after a failure. If multiple blocks are selected, the block in which a failure occurred cannot be detected. Either terminate device usage, or perform Block Erase for each block, specify the failed block, and stop using it. The host processor must take measures to prevent use of the failed block being used in the future.

Erase Suspend / Resume Mode

Erase Suspend Mode suspends Auto Block Erase and reads data from or writes data to an unselected block. The Erase Suspend command is allowed during an auto block erase operation but is ignored in all other operation modes. The Erase Suspend command is inhibited to input during the Erase Hold Time. When the command is input, the address of the bank on which Erase is being performed must be specified.

In Erase Suspend Mode only a Read, Program or Resume command can be accepted. If an Erase Suspend command is input during an Auto Block Erase, the device will enter Erase Suspend Read Mode after t_{SUSE} . The device status (Erase Suspend Read Mode) can be verified by checking the Hardware Sequence flag. If data is read consecutively from the block selected for Auto Block Erase, the DQ2 output will toggle and the DQ6 output will stop toggling and $\overline{RY/BY}$ will be set to High-Impedance.

Inputting a Write command during an Erase Suspend enables a Write to be performed to a block which has not been selected for the Auto Block Erase. Data is written in the usual manner.

To resume the Auto Block Erase, input an Erase Resume command. On input of the command, the address of the bank on which the Write was being performed must be specified. On receiving an Erase Resume command, the device returns to the state it was in when the Erase Suspend command was input. If an Erase Suspend command is input during the Erase Hold Time, the device will return to the state it was in at the start of the Erase Hold Time. At this time more blocks can be specified for erasing. If an Erase Resume command is input during an Auto Block Erase, Erase resumes. At this time toggle output of DQ6 resumes and 0 is output on $\overline{RY/BY}$.

Block Protect

Block Protection is a function to disable write and erase in block units. Applying VID to $\overline{\text{RESET}}$ and inputting the Block Protect command performs block protection. The first cycle of the command sequence is the Setup command. In the second cycle, the Block Protect command is input, in which a block address and $A1 = V_{IH}$ and $A0 = A6 = V_{IL}$ are input. At this time, the device writes to the block protector circuit. Until write is complete, there must be a wait of t_{PPLH} but the device need not be controlled during this time. In the third cycle, the Verify Block Protect command is input. This command verifies write to the block protector circuit. Read is performed in the fourth cycle. If the protection operation is complete, 01H is output. If other than 01H is output, write is not complete; thus, input the Block Protect command again. Canceling VID to $\overline{\text{RESET}}$ exits this mode.

Temporary Block Unprotection

The TC58VSF3580/3581AASB has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying VID to the $\overline{\text{RESET}}$ pin. At this time, Write and Erase operations can be performed on all the blocks except the boot blocks protected by Boot Block Protect. The device returns to the previous condition after VID is removed from the $\overline{\text{RESET}}$ pin. That is, previously protected blocks are protected again.

Verify Block Protect

The Verify Block Protect command is used to ascertain whether a block is protected or unprotected. This mode is set by setting $A0$, $A6$ and the block address $A19 \sim A12$ to V_{IL} and setting $A1$ to V_{IH} . This command should be input before a Read operation is performed. 0001H is output if the block is protected and 0000H is output if the block is unprotected. In Byte Mode $DQ8$ to $DQ15$ are in High-Impedance state. Block protection verification can also be carried out using a software command.

Boot Block Protection

Boot Block Protection temporarily protects some boot blocks using a method other than ordinary block protection. VID or a command sequence is not required. Protection is performed simply by inputting V_{IL} to $\overline{\text{WP/ACC}}$. The target blocks are two of the boot blocks. The Top Boot Block uses $BA69/BA70$; the Bottom Boot Block, $BA0/BA1$. Inputting V_{IH} to $\overline{\text{WP/ACC}}$ releases the mode. At this time, the block is protected in ordinary block protection mode.

Hidden Rom Area

The TH50VSF3582/3583AASB features a 64-Kbyte Hidden ROM area apart from the memory cells. The area consists of one block. Data Read, Write, and Protect can be performed on the block. Because Protect cannot be released, once the block is protected, data in the block cannot be overwritten.

The Hidden ROM area is located in the address space indicated in the Hidden ROM Area Address Table. Normally, memory cell data are accessed. To access the Hidden ROM area, input a Hidden ROM mode Entry command. At this time, the device enters Hidden ROM mode, allowing Read, Write, Erase, and Block Protect. Write and Erase operations are the same as Auto operations except that the device is in Hidden ROM mode. To protect the Hidden ROM area, use the Block Protect function. Operation of Block Protect here is the same as in normal Block Protect except that V_{IH} rather than V_{ID} is input to \overline{RESET} . Once the block is protected, protection cannot be released even using a Temporary Block Unprotect function. Use Block Protect carefully. Note that in Hidden ROM mode, simultaneous operation cannot be performed. Therefore, do not access areas other than the Hidden ROM area.

To exit Hidden ROM mode, use the Hidden ROM Mode Exit command. The device returns to Read mode.

Hidden Rom Area Address Table

| TYPE | BOOT BLOCK ARCHITECTURE | BYTE MODE | | WORD MODE | |
|-----------------|-------------------------|-------------------|-----------|------------------|-----------|
| | | ADDRESS RANGE | SIZE | ADDRESS RANGE | SIZE |
| TH50VSF3582AASB | TOP BOOT BLOCK | 3F0000H~3FFFFFFH | 64 Kbytes | 1F8000H~1FFFFFFH | 32 Kwords |
| TH50VSF3583AASB | BOTTOM BOOT BLOCK | 000000H~00FFFFFFH | 64 Kbytes | 000000H~007FFFFH | 32 Kwords |

Common Flash Memory Interface (CFI)

The TH50VSF3582/3583AASB conforms to the CFI. Information on device specifications and characteristics can be obtained via CFI. To read information from the device, input the Query command followed by the address. In Word mode, DQ8 to DQ15 all output 0s. To exit this mode, input the Reset command.

CFI Code Table

| ADDRESS A6~A0 | DATA DQ15~DQ0 | DESCRIPTION |
|-------------------|-------------------------|---|
| 10H 11H 12H | 0051H 0052H 0059H | Query Unique ASCII string "QRY" |
| 13H 14H | 0002H 0000H | Primary OEM Command Set 2: AMD/FJ standard type |
| 15H 16H | 0040H 0000H | Address for Primary Extended Table |
| 17H 18H | 0000H 0000H | Alternate OEM Command Set 0: none exists |
| 19H 1AH | 0000H 0000H | Address for Alternate OEM Extended Table |
| 1BH | 0027H | V _{DD} Min (write/erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 1CH | 0036H | V _{DD} Max (write/erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 1DH | 0000H | V _{PP} Min voltage |
| 1EH | 0000H | V _{PP} Max voltage |
| 1FH | 0004H | Typical timeout per single byte/word write (2 ^N μs) |
| 20H | 0000H | Typical timeout for Min size buffer write (2 ^N μs) |
| 21H | 000AH | Typical timeout per individual block erase (2 ^N ms) |
| 22H | 0000H | Typical timeout for full chip erase (2 ^N ms) |
| 23H | 0005H | Max timeout for byte/word write (2 ^N times typical) |
| 24H | 0000H | Max timeout for buffer write (2 ^N times typical) |
| 25H | 0004H | Max timeout per individual block erase (2 ^N times typical) |
| 26H | 0000H | Max timeout for full chip erase (2 ^N times typical) |
| 27H | 0016H | Device Size (2 ^N byte) |
| 28H 29H | 0002H 0000H | Flash Device Interface description 2: ×8/×16 |
| 2AH 2BH | 0000H 0000H | Max number of byte in multi-byte write (2 ^N) |

| ADDRESS A6~A0 | DATA DQ15~DQ0 | DESCRIPTION |
|---------------|---------------|---|
| 2CH | 0002H | Number of Erase Block Region within device |
| 2DH | 0007H | Erase Block Region 1 Information 0~15 bit: y = Block Number 16~31 bit: z = Block Size (z × 256 byte) |
| 2EH | 0000H | |
| 2FH | 0020H | |
| 30H | 0000H | |
| 31H | 003EH | Erase Block Region 2 Information |
| 32H | 0000H | |
| 33H | 0000H | |
| 34H | 0001H | |
| 40H | 0050H | Query Unique ASCII string "PRI" |
| 41H | 0052H | |
| 42H | 0049H | |
| 43H | 0031H | Major version number, ASCII |
| 44H | 0031H | Minor version number, ASCII |
| 45H | 0000H | Address Sensitive Unlock 0: Required 1: Not Required |
| 46H | 0002H | Erase Suspend 0: Not Supported 1: To Read Only 2: To Read & Write |
| 47H | 0001H | Block Protect 0: Not Supported X: Number of blocks in per group |
| 48H | 0001H | Block Temporary Unprotect 0: Not Supported 1: Supported |
| 49H | 0004H | Block Protect/Unprotect scheme |
| 4AH | 0001H | Simultaneous Operation 0: Not Supported 1: Supported |
| 4BH | 0000H | Burst Mode 0: Not Supported |
| 4CH | 0000H | Page Mode 0: Not Supported |
| 4DH | 0085H | V _{ACC} Min voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 4EH | 0095H | V _{ACC} Max voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV |
| 4FH | 000XH | Top/Bottom Boot Block Flag 2: TH50VSF3582AASB 3: TH50VSF3583AASB |
| 50H | 0001H | Program Suspend 0: Not Supported 1: Supported |

HARDWARE SEQUENCE FLAGS FOR FLASH MEMORY

The TH50VSF3582/3583AASB has a Hardware Sequence flag which allows the device status to be determined during an auto mode operation. The output data is read out using the same timing as that used when $\overline{CE\overline{F}} = \overline{OE} = V_{IL}$ in Read Mode. The $\overline{RY/B\overline{Y}}$ output can be either High or Low.

The device re-enters Read Mode automatically after an auto mode operation has been completed successfully. The Hardware Sequence flag is read to determine the device status and the result of the operation is verified by comparing the read-out data with the original data.

DQ7 (\overline{DATA} polling)

During an Auto-Program or auto-erase operation, the device status can be determined using the data polling function. \overline{DATA} polling begins on the rising edge of \overline{WE} in the last bus cycle. In an Auto-Program operation, DQ7 outputs inverted data during the programming operation and outputs actual data after programming has finished. In an auto-erase operation, DQ7 outputs 0 during the erase operation and 1 when the erase operation has finished. If an auto mode operation fails, DQ7 simply outputs the data.

When the operation has finished, the address latch is reset. Data polling is asynchronous with the \overline{OE} signal.

DQ6 (Toggle bit 1)

The device status can be determined by the Toggle Bit function during an Auto Program or Auto Erase operation. The Toggle bit begins toggling on the rising edge of \overline{WE} in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each attempt (\overline{OE} access) while $\overline{CE\overline{F}} = V_{IL}$ while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation failed, the DQ6 output toggles.

DQ6 toggles for around 3 μ s when an attempt is made to execute an Auto Program operation on a protected block. It then stops toggling. DQ6 toggles for around 100 μ s when an attempt is made to execute an Auto Erase operation on a protected block. It then stops toggling. After toggling stops the device returns to Read mode.

DQ5 (internal time-out)

DQ5 outputs a 1 when the Internal Timer has timed out during a Program or Erase operation. This indicates that the operation has not completed within the allotted time.

An attempt to program 1 into a cell containing 0 will fail (see Auto Program mode). DQ5 outputs 1 in this case. Either a hardware reset or a software reset command is required to put the device into Read mode.

DQ3 (Block Erase timer)

The Block Erase operation starts 50 μ s (Erase Hold Time) after the rising edge of \overline{WE} in the last command cycle. DQ3 outputs a 0 during the Block Erase Hold Time and a 1 when the Erase operation starts. Additional Block Erase commands can only be accepted during this Block Erase Hold Time. Each Block Erase command received within this hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

DQ2 (Toggle bit 2)

DQ2 is used to detect blocks for Auto Block Erase or to detect whether the device is in Erase Suspend mode.

During Auto Block Erase, if data are continuously read from the selected block, DQ2 output toggles. At this time 1 is output from non-selected blocks; thus, the selected block can be detected. When the device is in Erase Suspend mode, if data are continuously read from the selected block for Auto Block Erase, DQ2 output toggles. At this time, because DQ6 output does not toggle, Erase Suspend mode can be detected. When the device is in Programming mode during Erase suspend, if data are read from the address to which data are being written, DQ2 outputs 1.

RY/ \overline{BY} (READY / \overline{BUSY})

The TH50VSF3582/3583AASB has a RY/ \overline{BY} signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto Program or Auto Erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can accept a new command. The RY/ \overline{BY} signal outputs a 0 when an operation has failed.

The RY/ \overline{BY} signal outputs a 0 after the rising edge of \overline{WE} in the last command cycle.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. The RY/ \overline{BY} signal outputs a 1 during an Erase Suspend operation. The output buffer for the RY/ \overline{BY} pin is an open drain type circuit, allowing a wired — OR connection. A pull-up resistor needs to be inserted between VCC and the RY/ \overline{BY} pin.

DATA PROTECTION

The TH50VSF3582/3583AASB features a function which makes malfunction or data damage difficult.

Protection Against Program/Erase Caused by Low Supply Voltage

To prevent malfunction at power on or power down, the device does not receive commands when V_{CCf} is below V_{LKO} . In this state, command input is ignored.

If V_{CCf} drops below V_{LKO} during Auto operations, the device terminates Auto Program execution. In this case, Auto operation is not executed again when V_{CCf} return to recommended V_{CCf} voltage Therefore, command need to be input to execute Auto operation again.

When $V_{CCf} > V_{LKO}$, make up countermeasure to be input accurately command in system side please.

Protection Against Malfunction Caused by Glitches

To prevent malfunction caused by noise from the system in operation, the device does not receive pulses shorter than 3 ns(Typ.) input to \overline{WE} , \overline{CEf} , or \overline{OE} . However, if a glitch exceeding 3 ns(Typ.) occurs and the glitch is input to the device, although rare, malfunction may occur.

The device uses standard JEDEC commands; thus making command input difficult. It is conceivable that in an extreme case a part of a command sequence input due to system noise may occur. At this time, the device acknowledges the part of the command sequence. Then, even if the proper command is input, the device does not operate. To avoid this, before command input, clear the Command register. In an environment where system noise occurs easily, Toshiba recommends input of a software or hardware reset before command input.

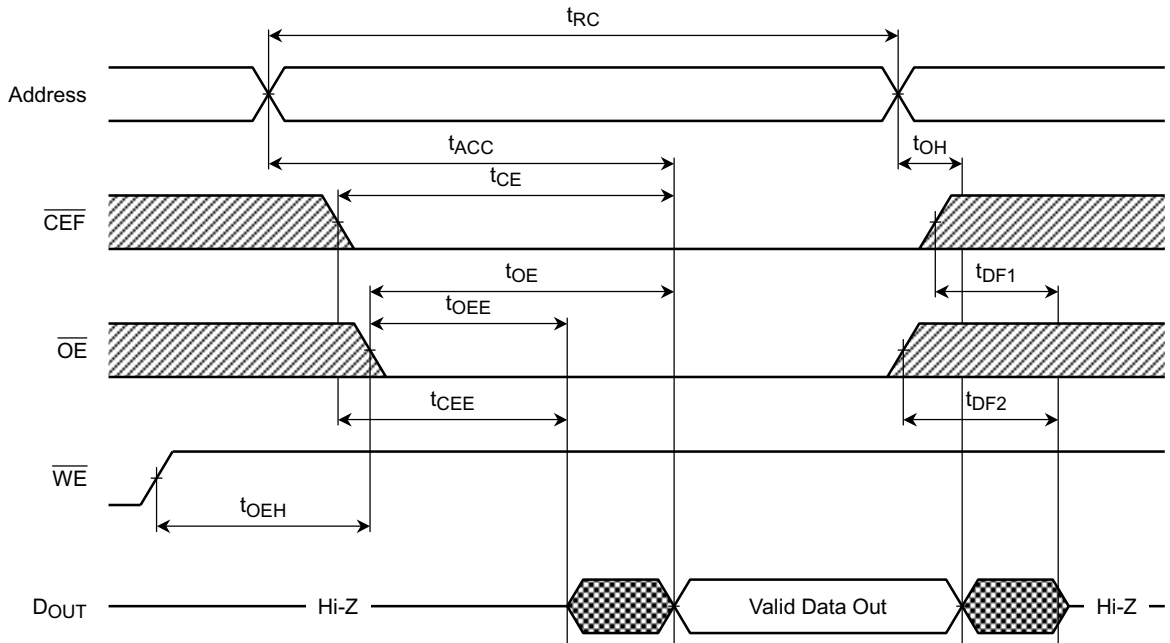
Protection Against Malfunction at Power-on

To prevent damage to data caused by sudden noise at power on, when power is turned on with $\overline{WE} = \overline{CEf} = V_{IL}$ and $\overline{OE} = V_{IL}$, the device does not latch the command at the first rising edge of \overline{WE} or \overline{CEf} . The device automatically resets the Command register and enters Read mode.

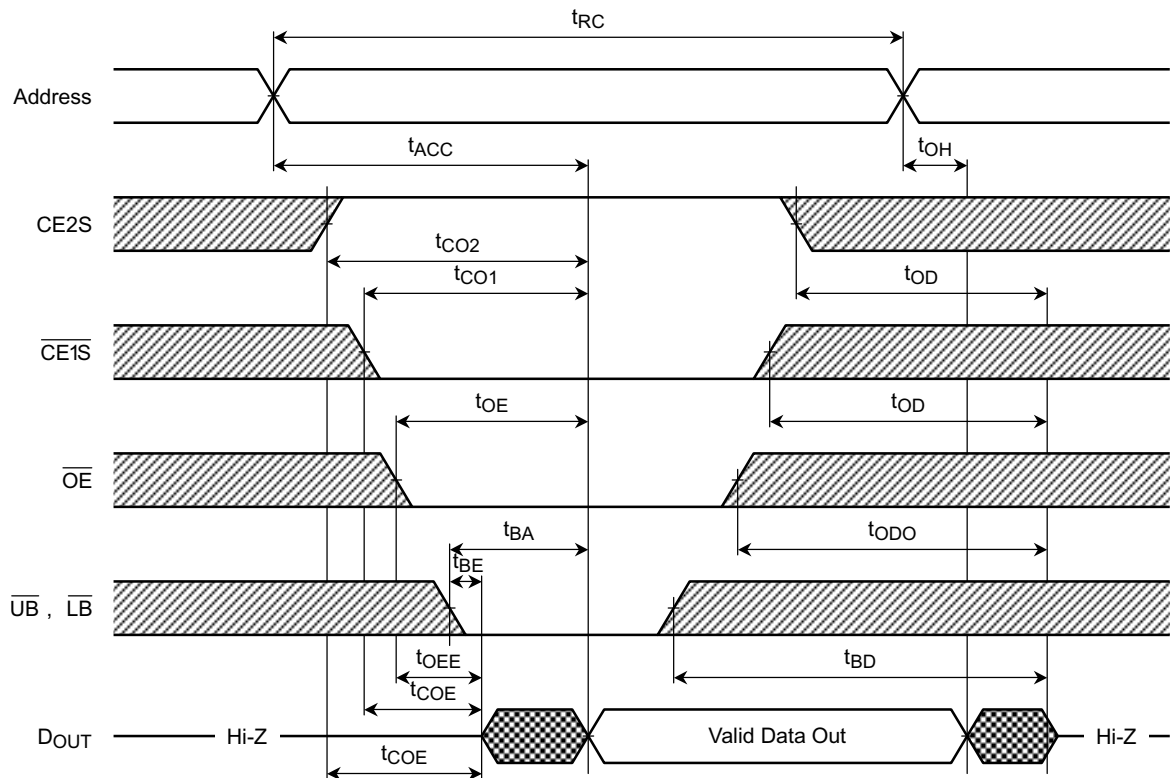
TIMING DIAGRAMS



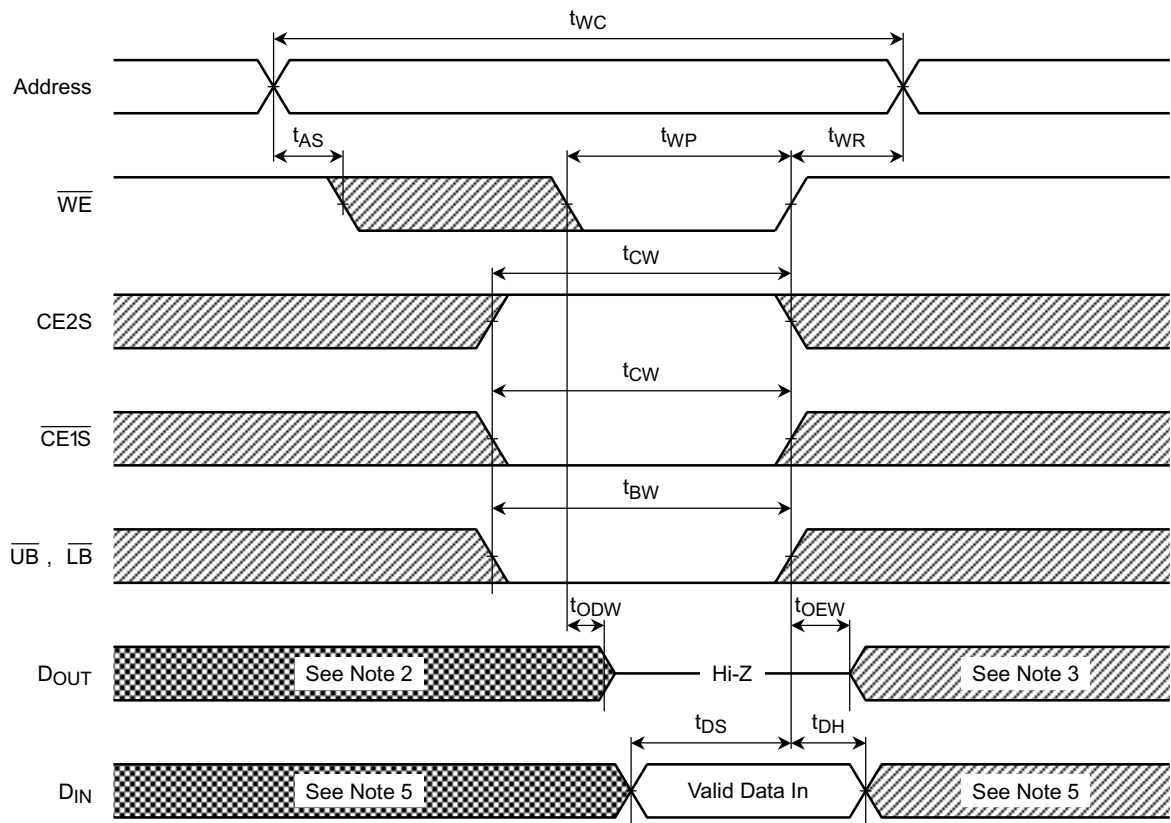
FLASH READ/ID READ OPERATION



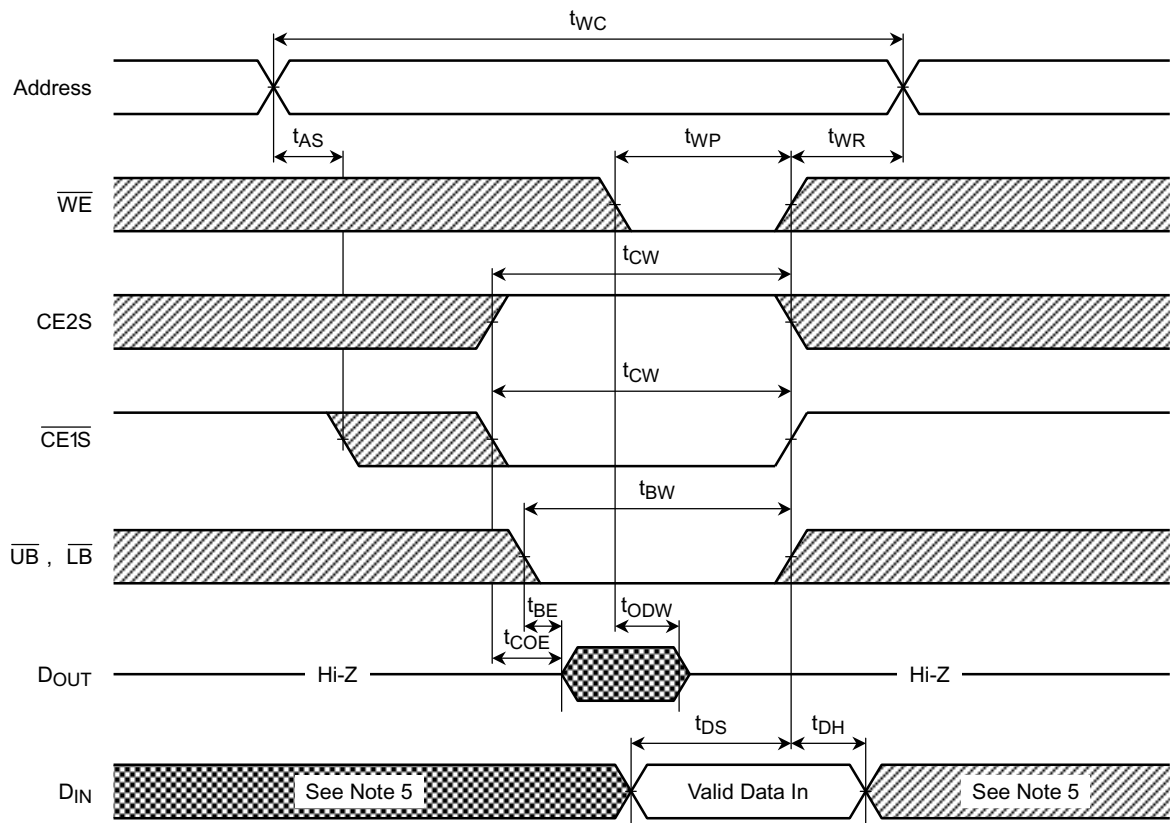
SRAM READ CYCLE (see Note 1)



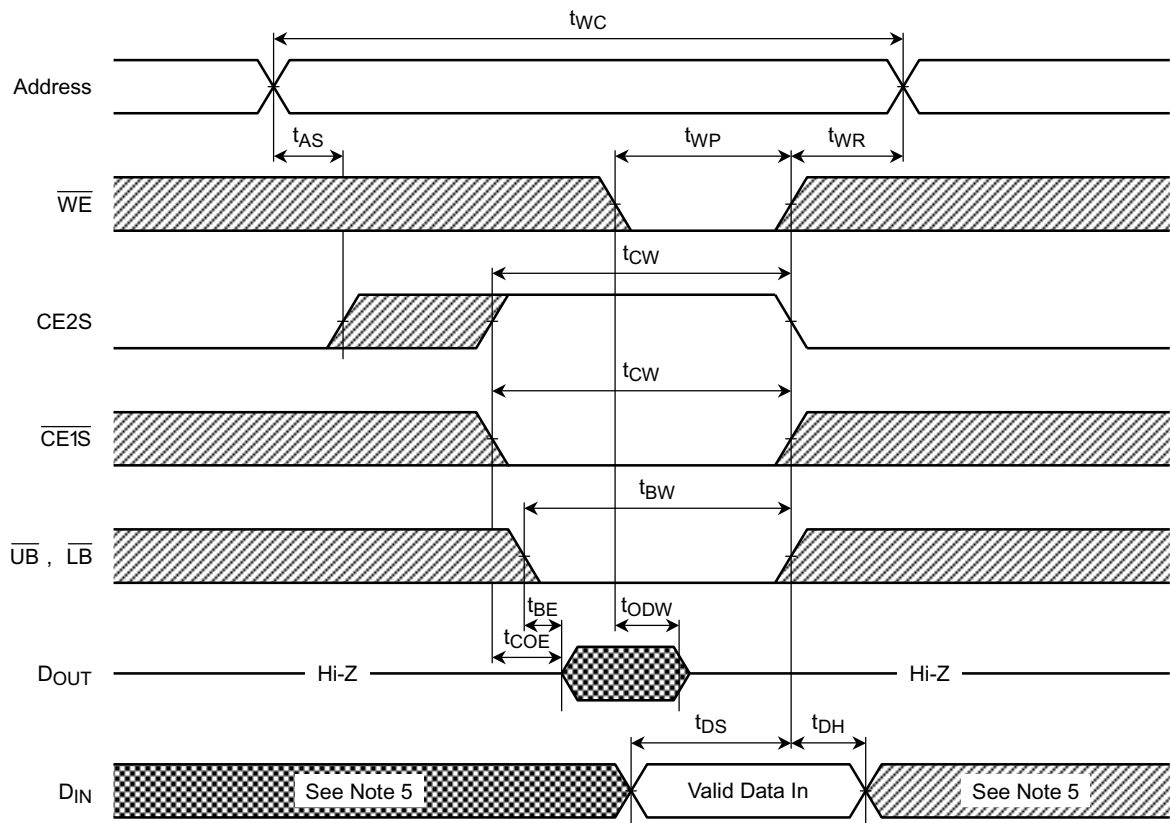
SRAM WRITE CYCLE 1 (\overline{WE} -CONTROLLED) (see Note 4)



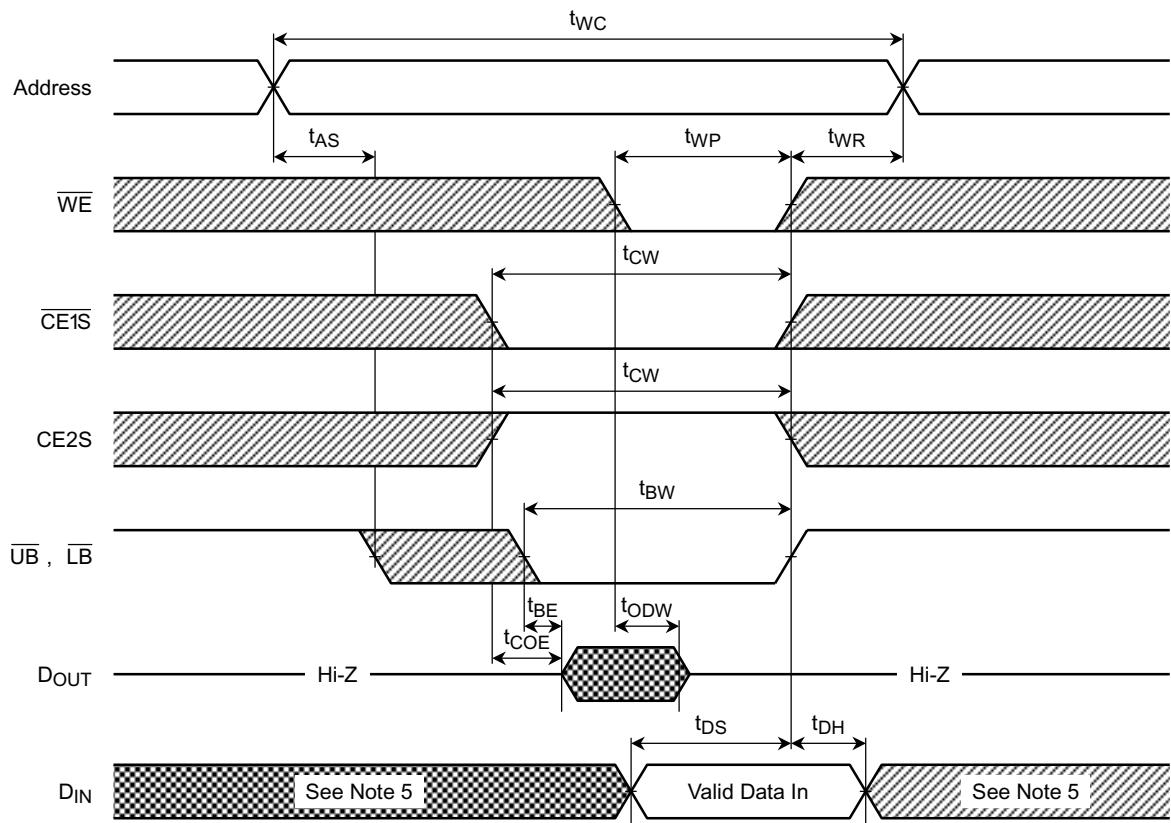
SRAM WRITE CYCLE 2 ($\overline{CE1S}$ -CONTROLLED) (see Note 4)



SRAM WRITE CYCLE 3 (CE2S-CONTROLLED) (see Note 4)



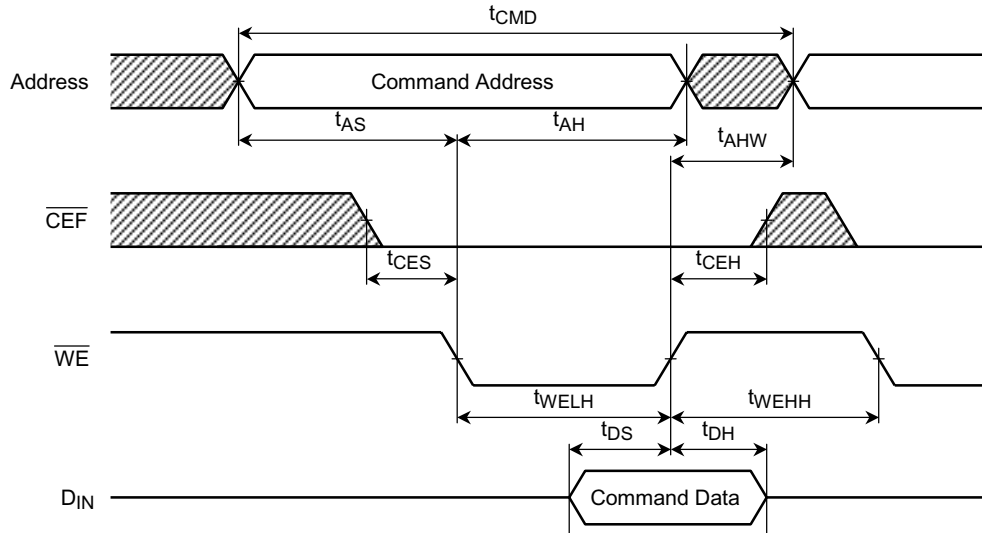
SRAM WRITE CYCLE 4 (\overline{UB} - and \overline{LB} -CONTROLLED) (see Note 4)



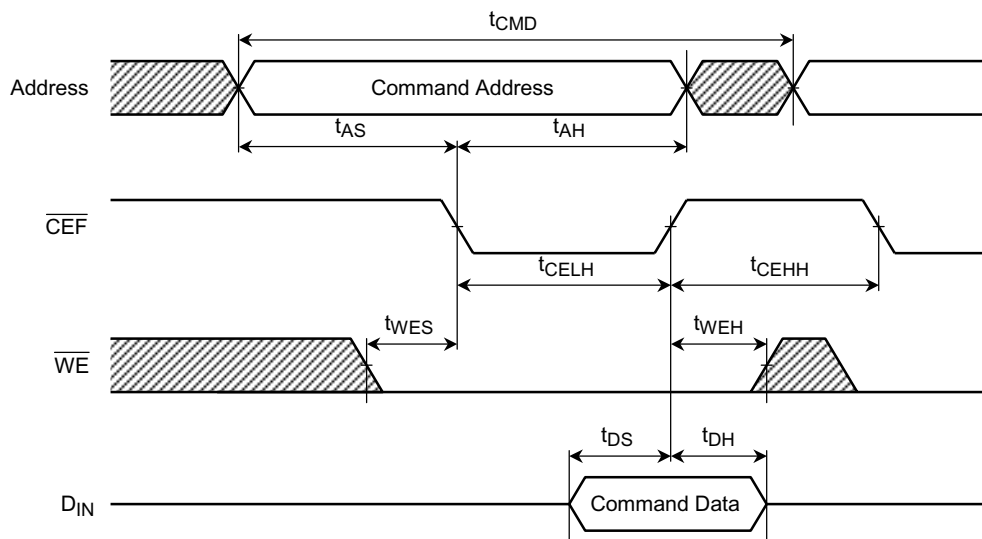
FLASH COMMAND WRITE OPERATION

This is the timing of the Command Write Operation. The timing which described follow pages is typically same as this page's.

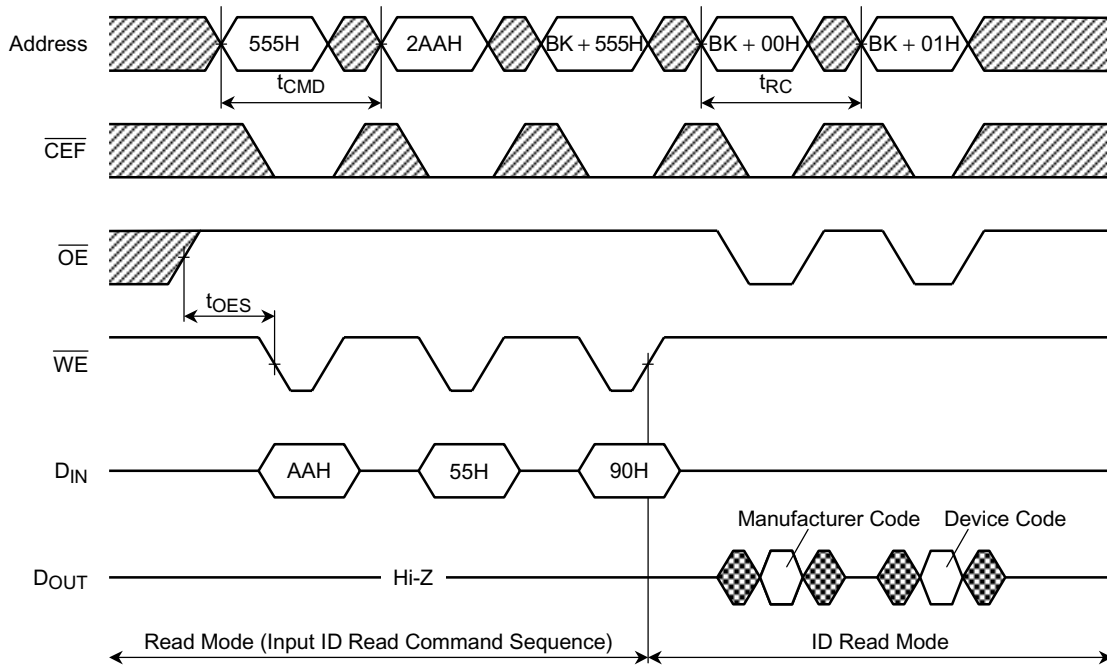
- \overline{WE} Control



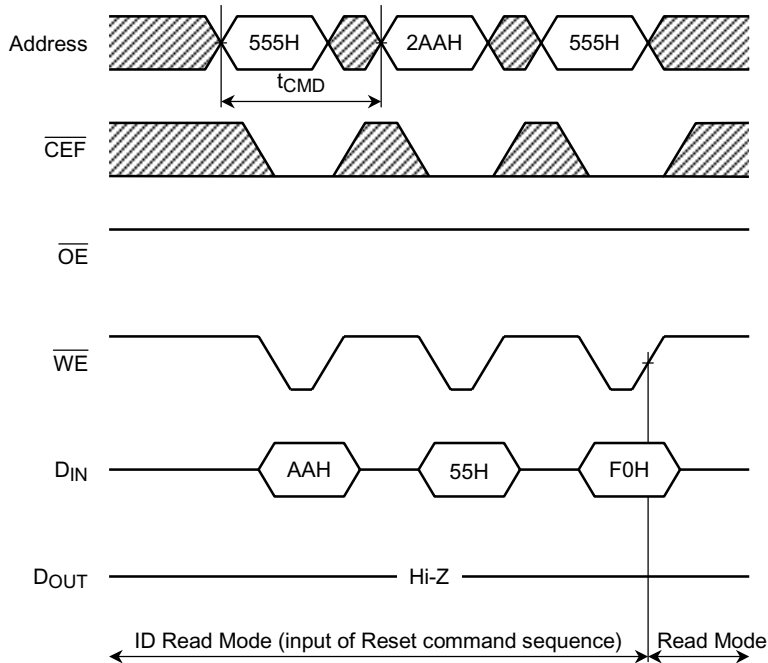
- $\overline{CE\overline{F}}$ Control



FLASH ID READ OPERATION (Input command sequence)

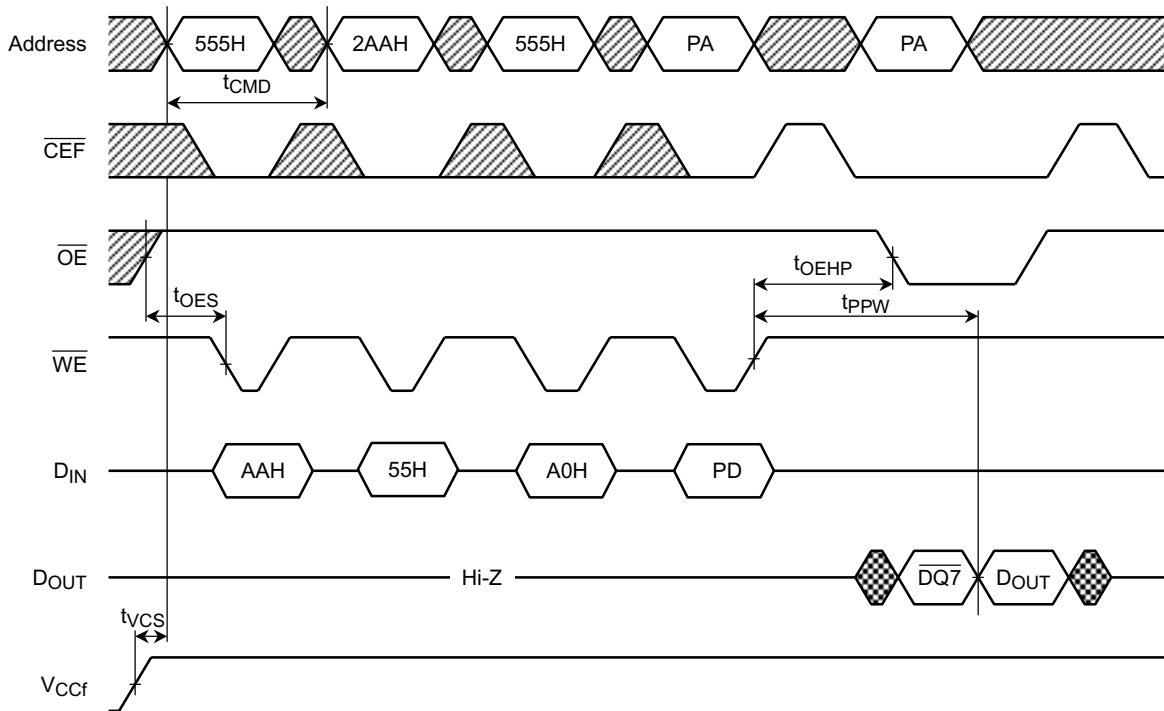


(Continued)



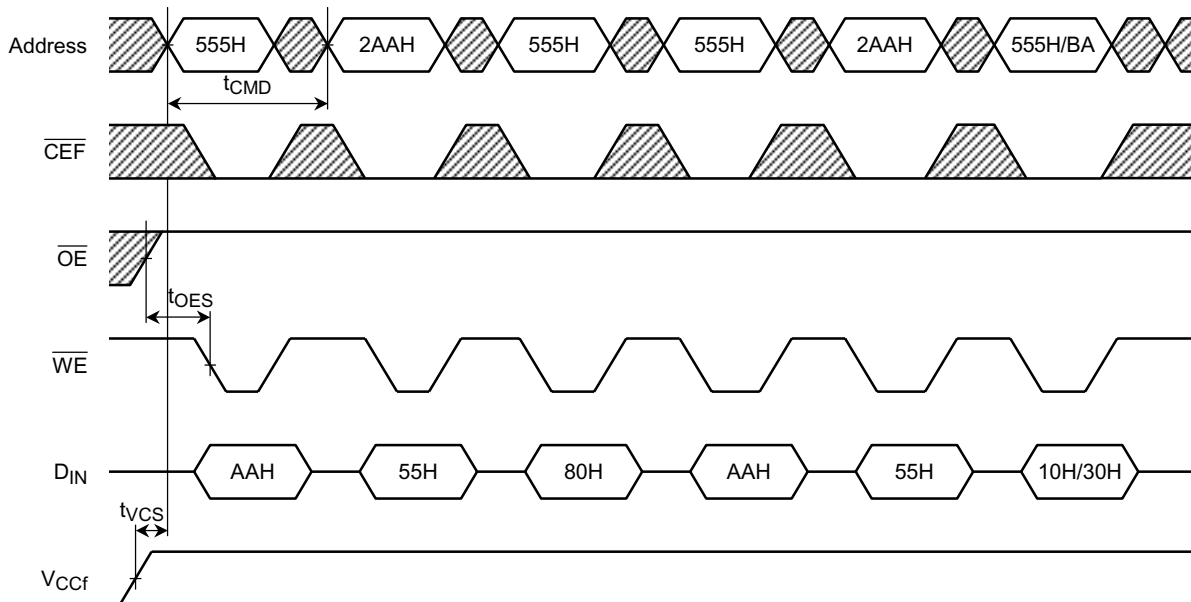
Notes: Word mode address shown
BK: Bank address

FLASH AUTO-PROGRAM OPERATION (\overline{WE} -CONTROLLED)



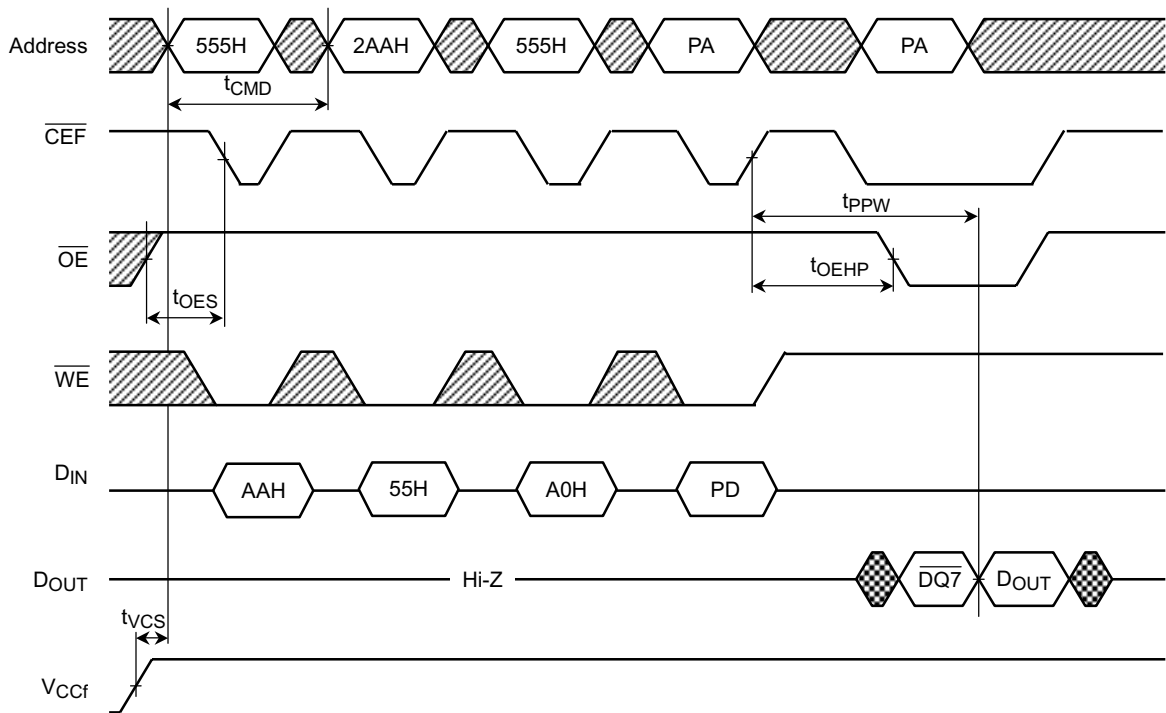
Note: Word Mode address shown.
 PA: Program address
 PD: Program data

FLASH AUTO CHIP ERASE/AUTO BLOCK ERASE OPERATION (\overline{WE} -CONTROLLED)



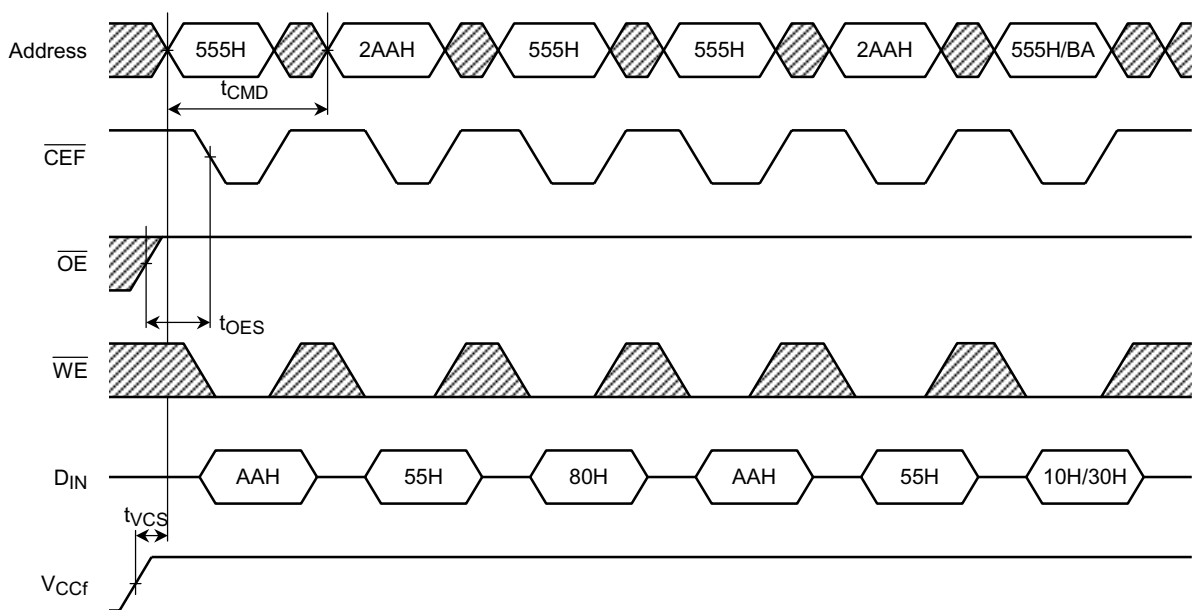
Notes: Word mode address shown
 BA: Block address for Auto Block Erase operation

FLASH AUTO-PROGRAM OPERATION ($\overline{\text{CE}}\overline{\text{F}}$ -CONTROLLED)



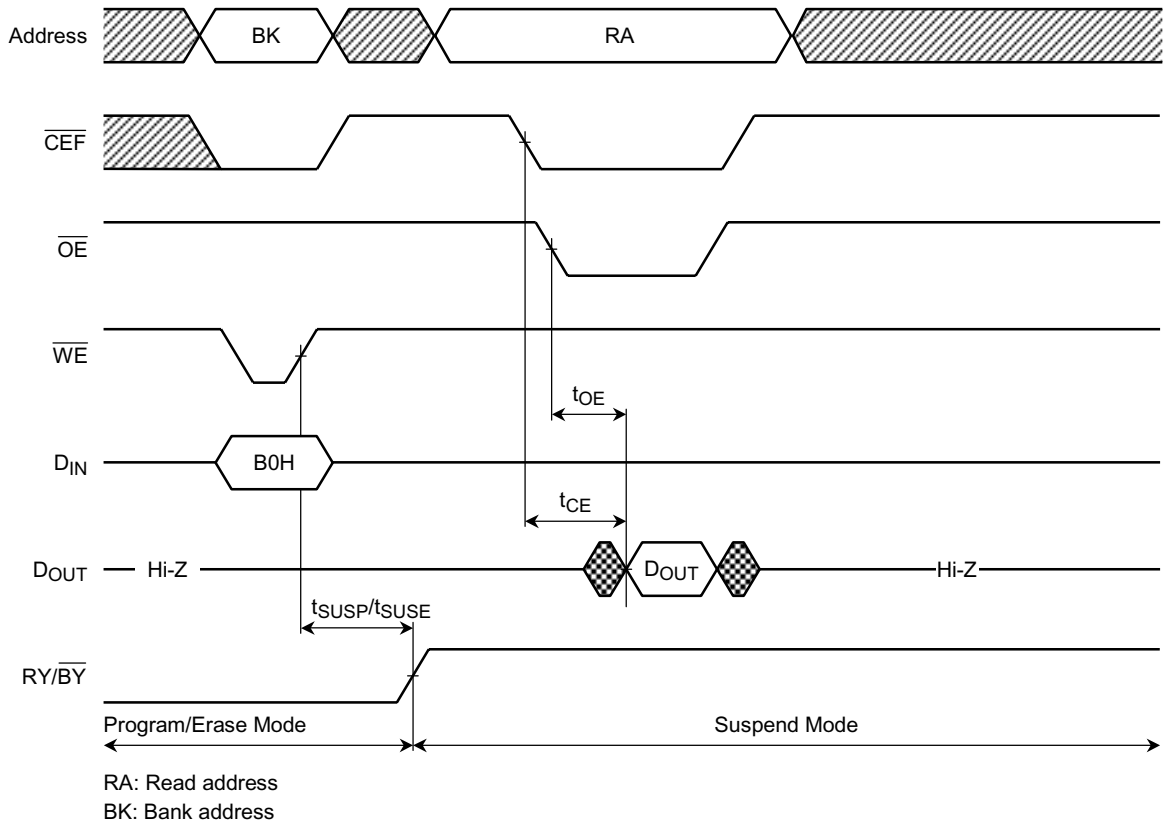
Notes: Word mode address shown
 PA: Program address
 PD: Program data

FLASH AUTO CHIP ERASE/AUTO BLOCK ERASE OPERATION ($\overline{\text{CE}}\overline{\text{F}}$ -CONTROLLED)

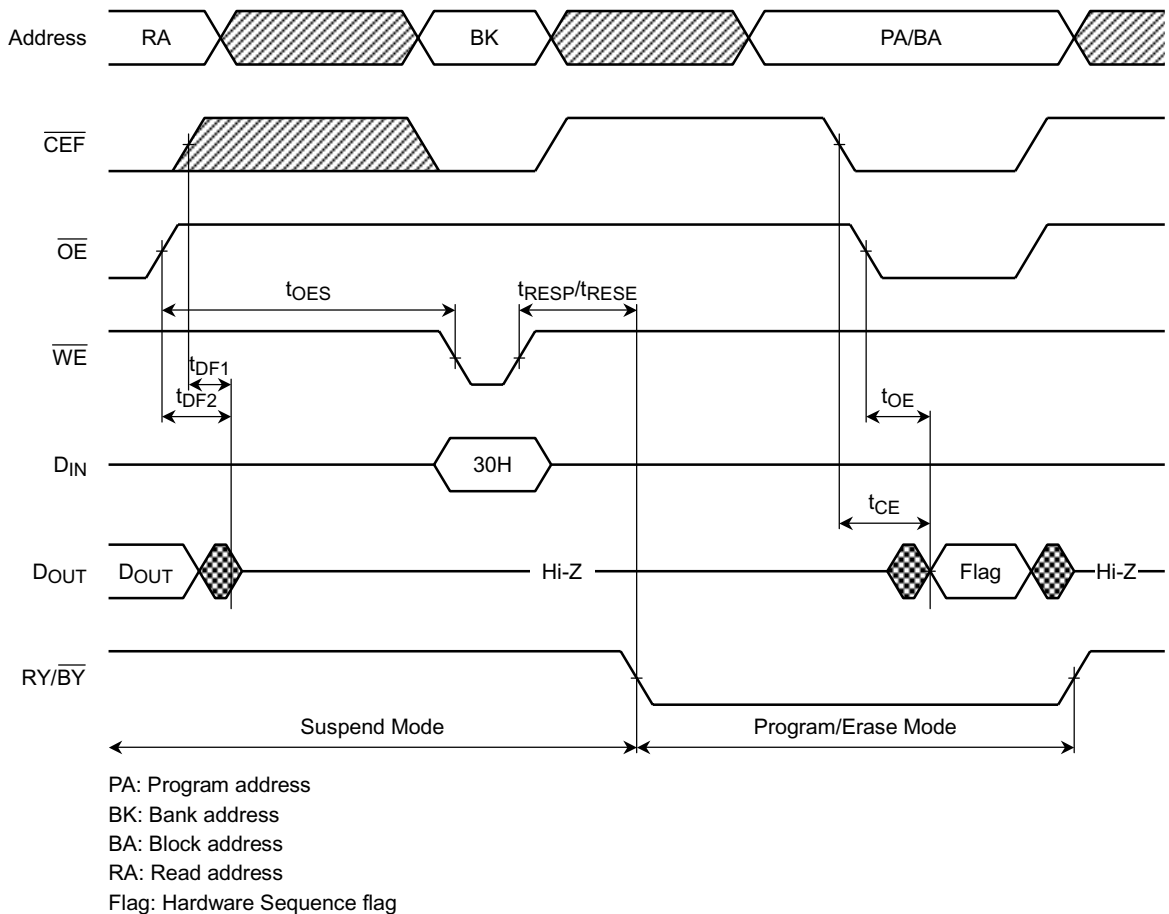


Note: Word Mode address shown.
 BA: Block address for Auto Block Erase operation

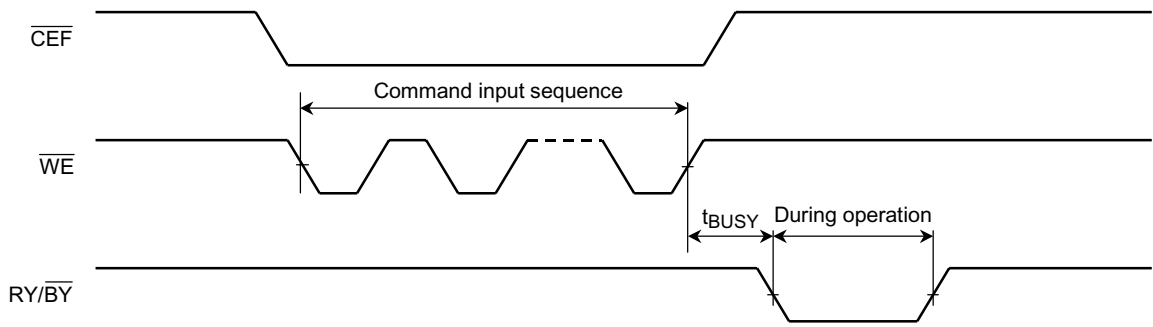
FLASH PROGRAM/ERASE SUSPEND OPERATION



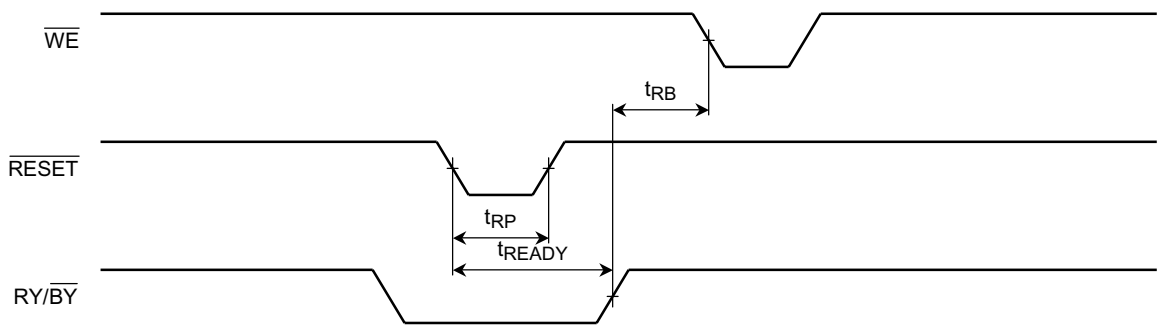
FLASH PROGRAM/ERASE RESUME OPERATION



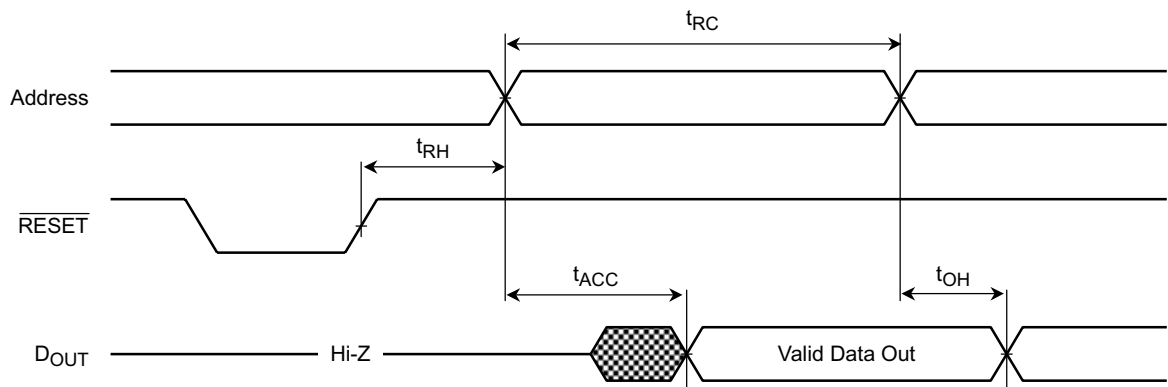
FLASH RY/ $\overline{\text{BY}}$ DURING AUTO-PROGRAM/ERASE OPERATION



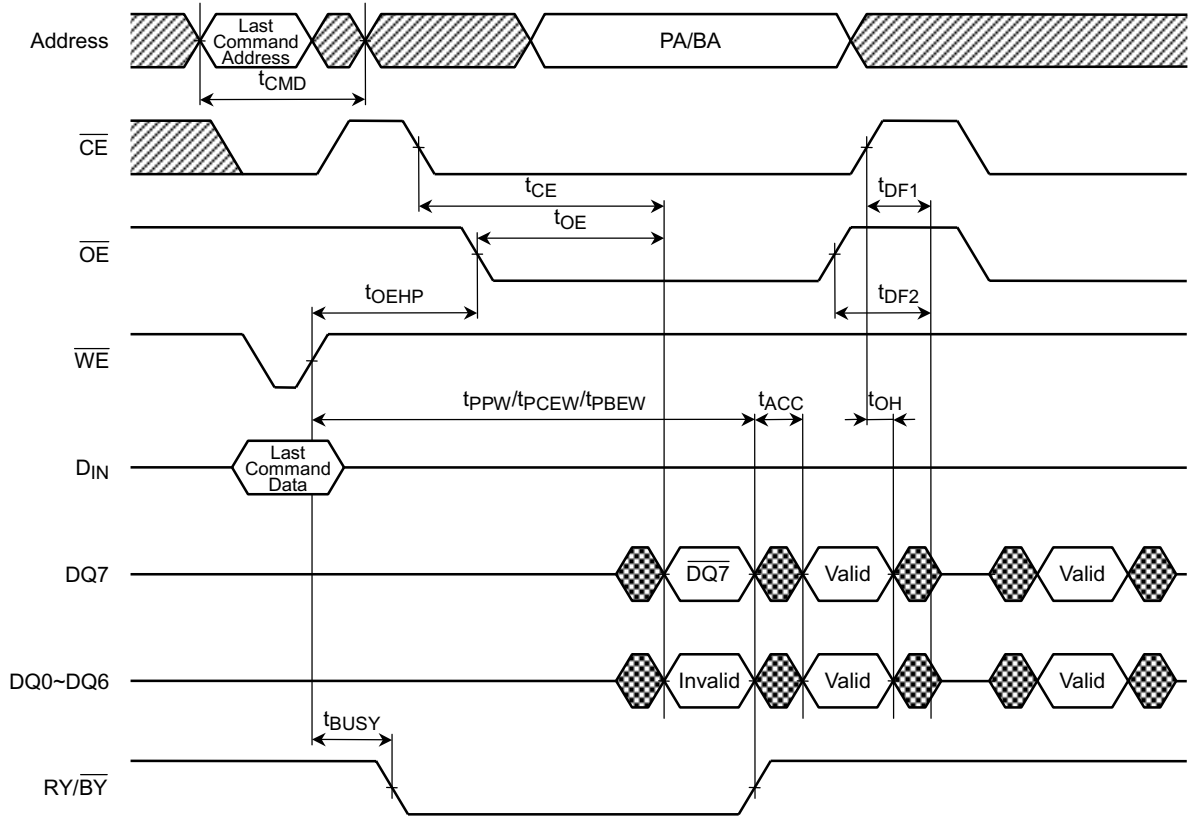
FLASH HARDWARE RESET OPERATION



FLASH READ AFTER $\overline{\text{RESET}}$

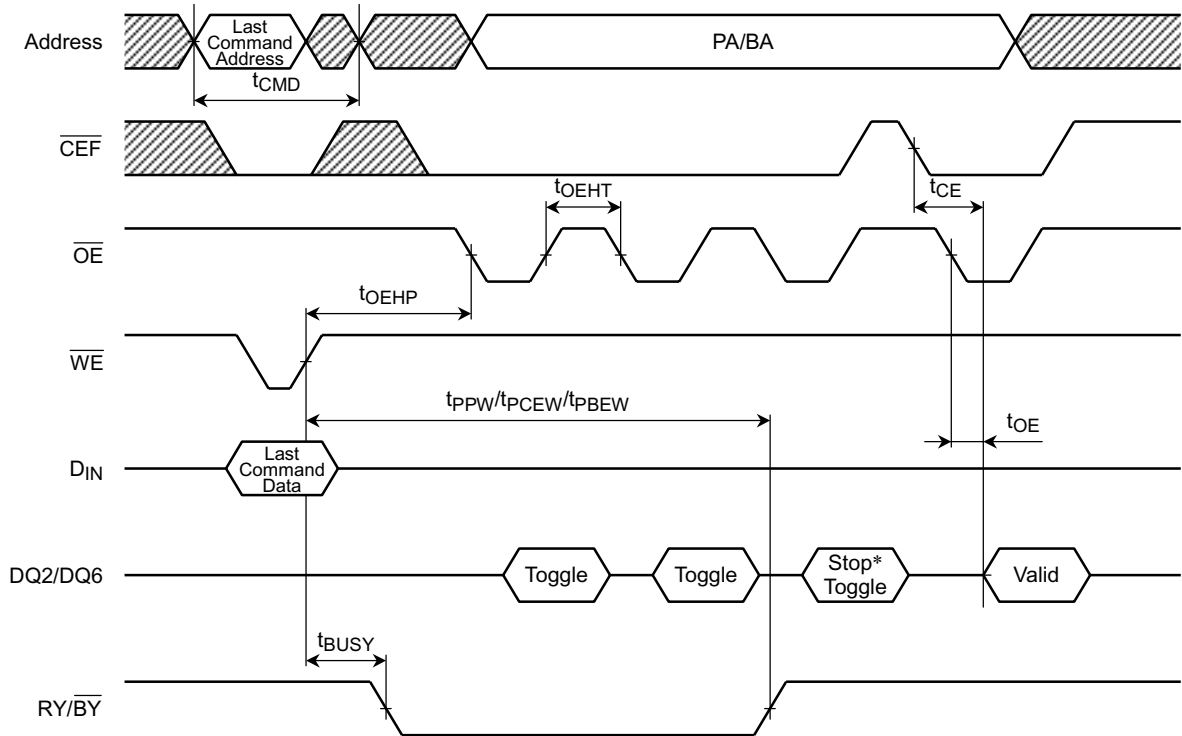


FLASH HARDWARE SEQUENCE FLAG (DATA Polling)



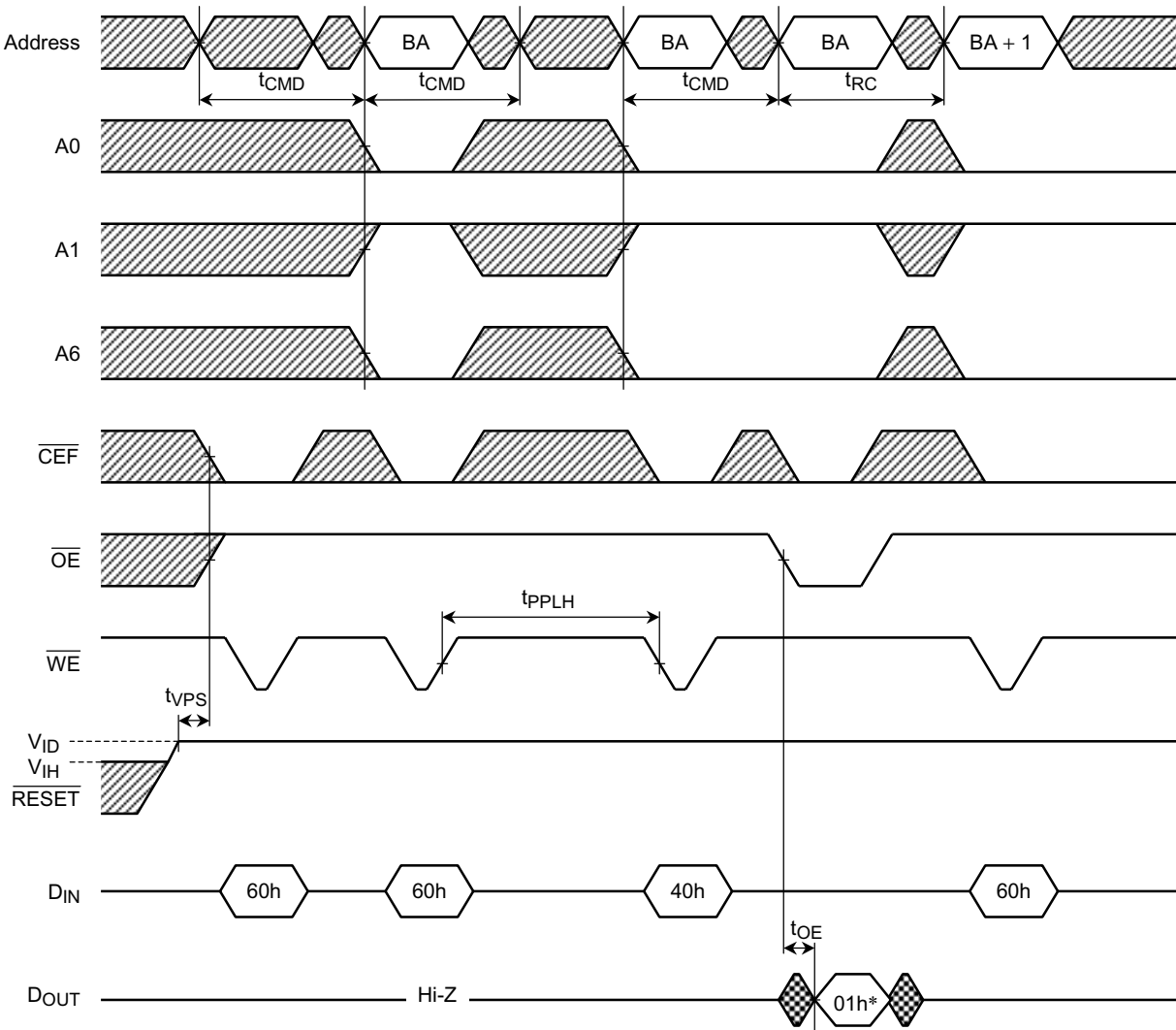
PA: Program address
BA: Block address

FLASH HARDWARE SEQUENCE FLAG (Toggle Bit)

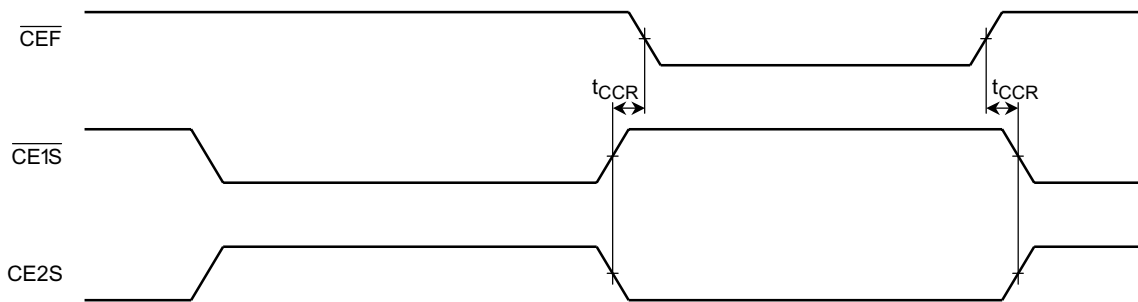


PA: Program address
BA: Block address
*DQ2/DQ6 stops toggling when auto operation has been completed.

FLASH BLOCK PROTECT OPERATION



Notes: BA : Block address
 BA + 1: Next Block address
 * : 01h indicates that block is protected.

TIMING FOR SWITCHING BETWEEN FLASH AND SRAM MODES

Notes:

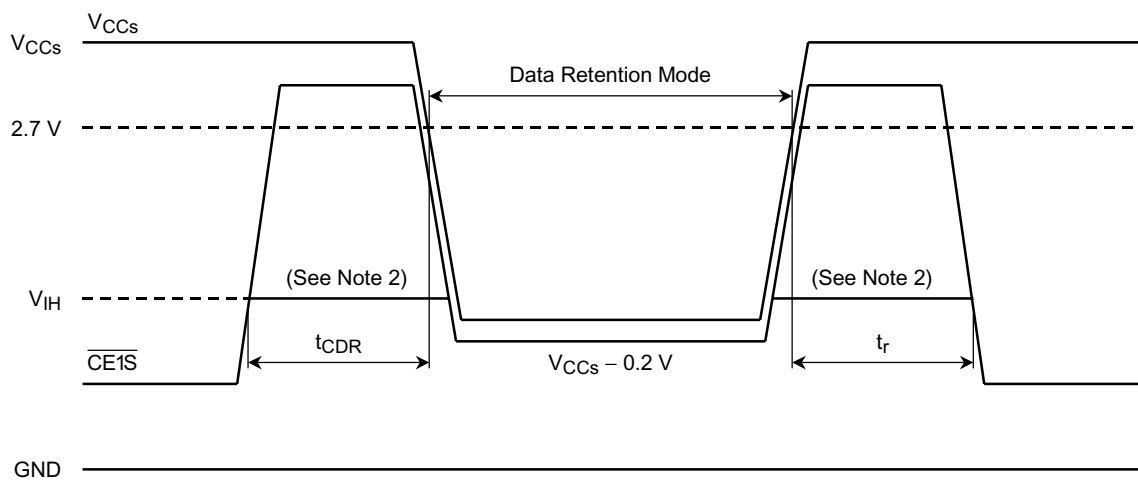
- (1) \overline{WE} remains High during a Read cycle.
- (2) If $\overline{CE1\overline{S}}$ goes Low (or $CE2\overline{S}$ goes High) at the same time as or after \overline{WE} goes Low, the outputs will remain High-Impedance.
- (3) If $\overline{CE1\overline{S}}$ goes High (or $CE2\overline{S}$ goes Low) at the same time as or before \overline{WE} goes High, the outputs will remain High-Impedance.
- (4) If \overline{OE} is High during a Write cycle, the outputs will remain High-Impedance.
- (5) Because I/O pins may be in Output state at this point, input signals of the opposite value must not be applied.
- (6) DOUT6 stops toggling when the last command has been completed.

SRAM DATA RETENTION CHARACTERISTICS (Ta = -30°~85°C)

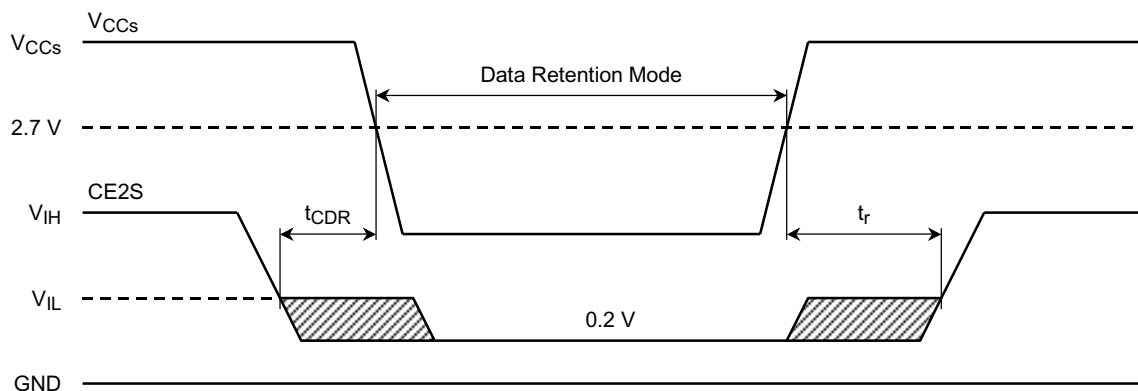
| SYMBOL | PARAMETER | | MIN | TYP. | MAX | UNIT | |
|-------------------|---|-------------------------|--------------------------------|------|-----|------|----|
| V _{DH} | Data Retention Supply Voltage for SRAM | | 1.5 | — | 3.3 | V | |
| I _{CCS4} | SRAM Standby Current | V _{DH} = 3.3 V | Ta = -30°~85°C | — | — | 10 | μA |
| | | V _{DH} = 3.0 V | Ta = -30°~40°C | — | — | 1 | |
| | | | Ta = -30°~85°C | — | — | 5 | |
| t _{CDR} | Chip-Deselect-to-Data-Retention-Mode Time | | 0 | — | — | ns | |
| t _r | Recovery Time | | t _{RC} ⁽¹⁾ | — | — | ns | |

(1) Read cycle time

CE1S-CONTROLLED DATA RETENTION MODE (see Note 1)



CE2S-CONTROLLED DATA RETENTION MODE (see Note 3)

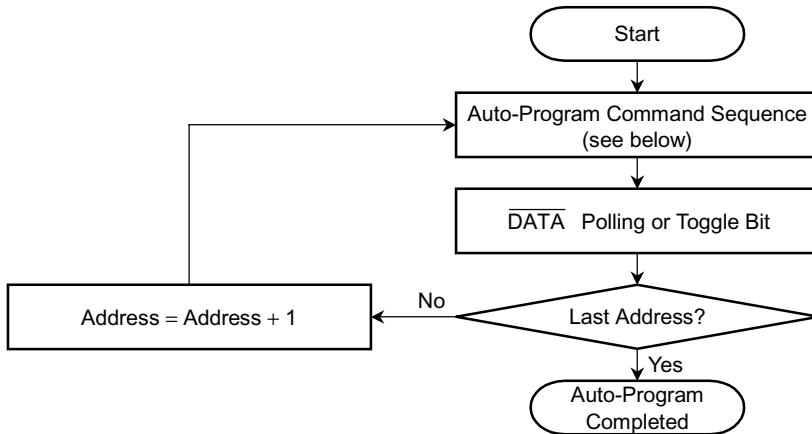


Notes:

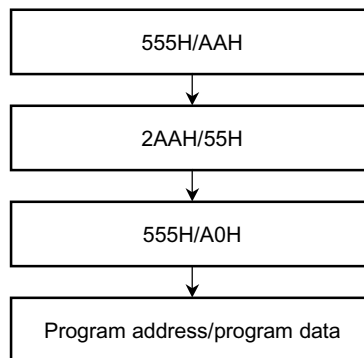
- (1) In $\overline{\text{CE1S}}$ -Controlled Data Retention Mode, Minimum Standby Current Mode is entered when $\overline{\text{CE2S}} \leq 0.2 \text{ V}$ or $\overline{\text{CE2S}} \geq V_{\text{CCS}} - 0.2 \text{ V}$.
- (2) When $\overline{\text{CE1S}}$ is operating at the V_{IH} level, the SRAM standby current is the same as I_{CCS3} during the transition of V_{CCS} from 2.67 V to 2.3 V.
- (3) In CE2S-Controlled Data Retention Mode, Minimum Standby Current Mode is entered when $\text{CE2S} \leq 0.2 \text{ V}$.

FLOWCHARTS OF FLASH MEMORY OPERATIONS

Auto-Program

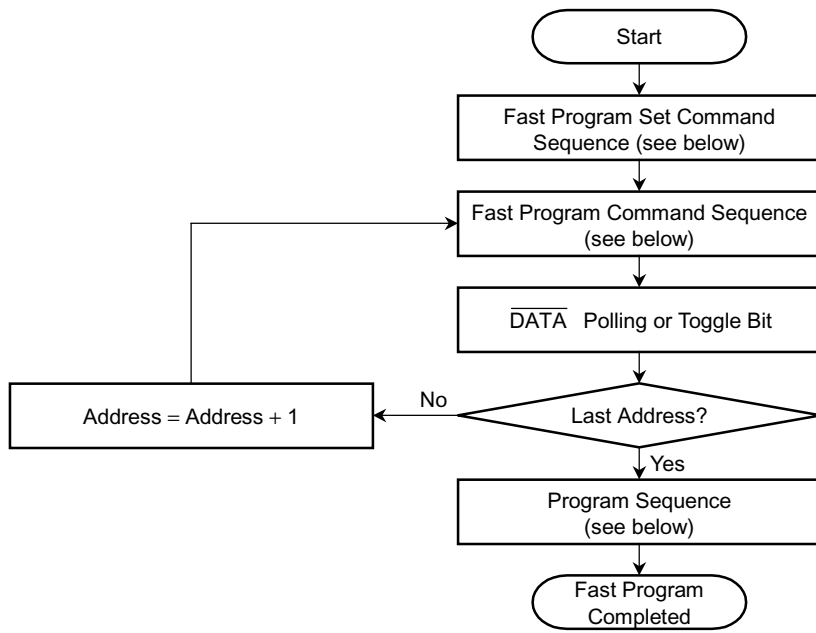


Auto-Program command sequence (address/data)

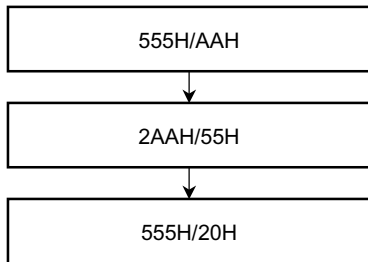


Note: Word mode command sequence is shown.

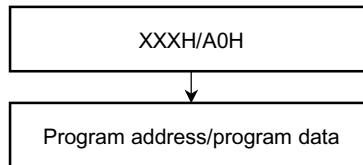
Fast Program



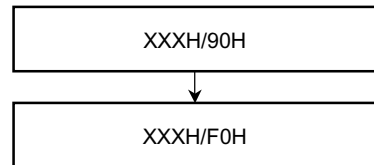
Fast Program Set command sequence (address/data)



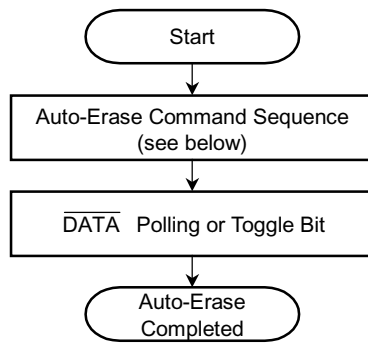
Fast Program command sequence (address/data)



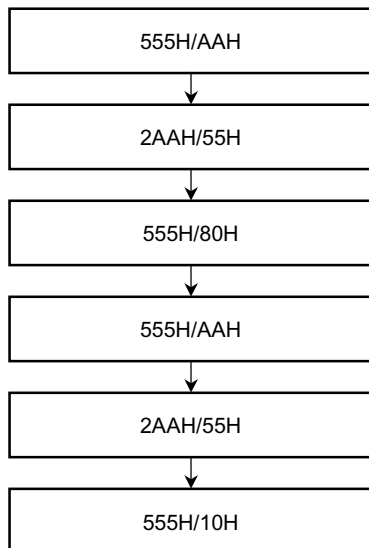
Fast Program Reset command sequence (address/data)



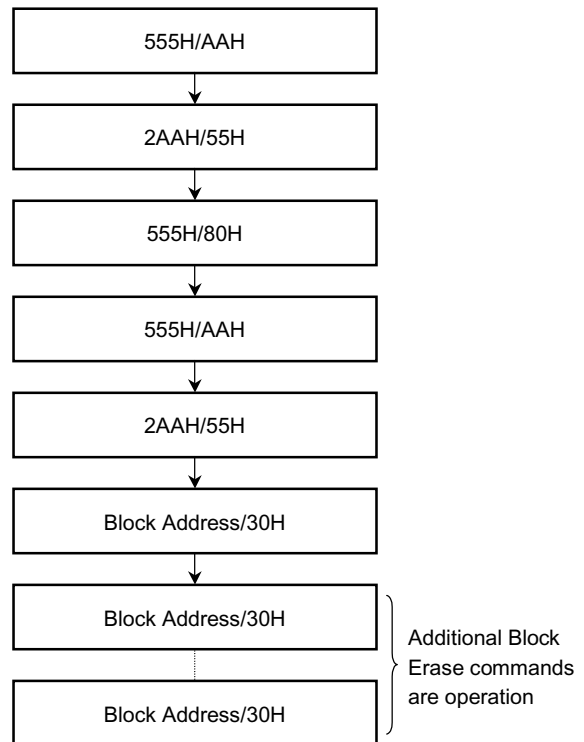
Auto-Erase



Auto Chip Erase command sequence
(address/data)

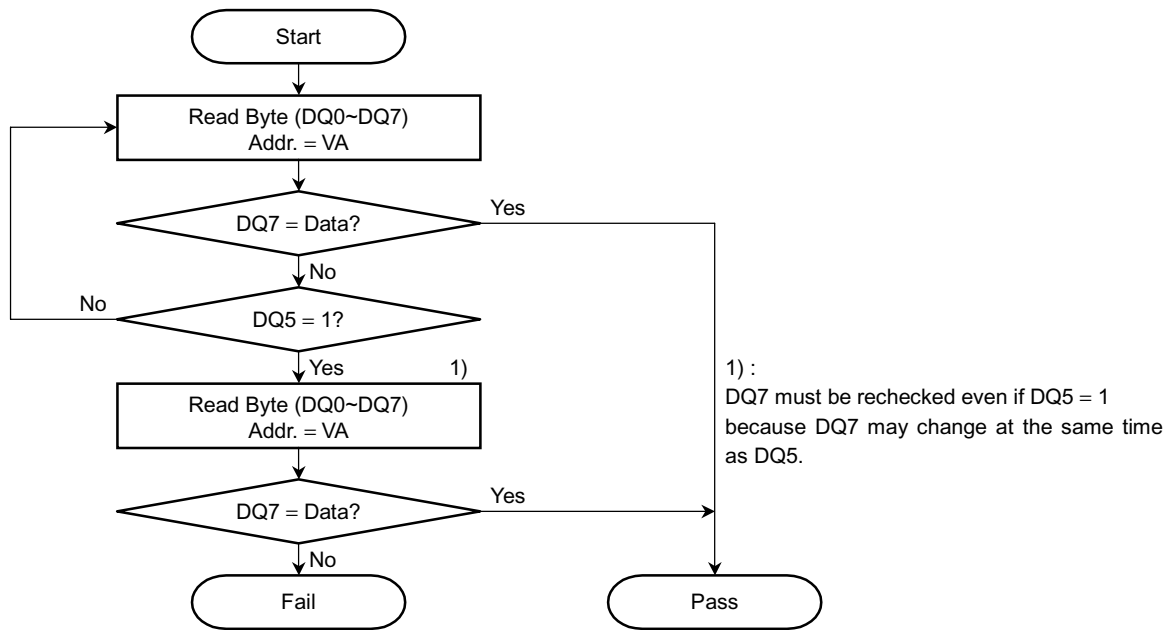


Auto Block Erase / Multiple-Block Erase command
sequence (address/data)

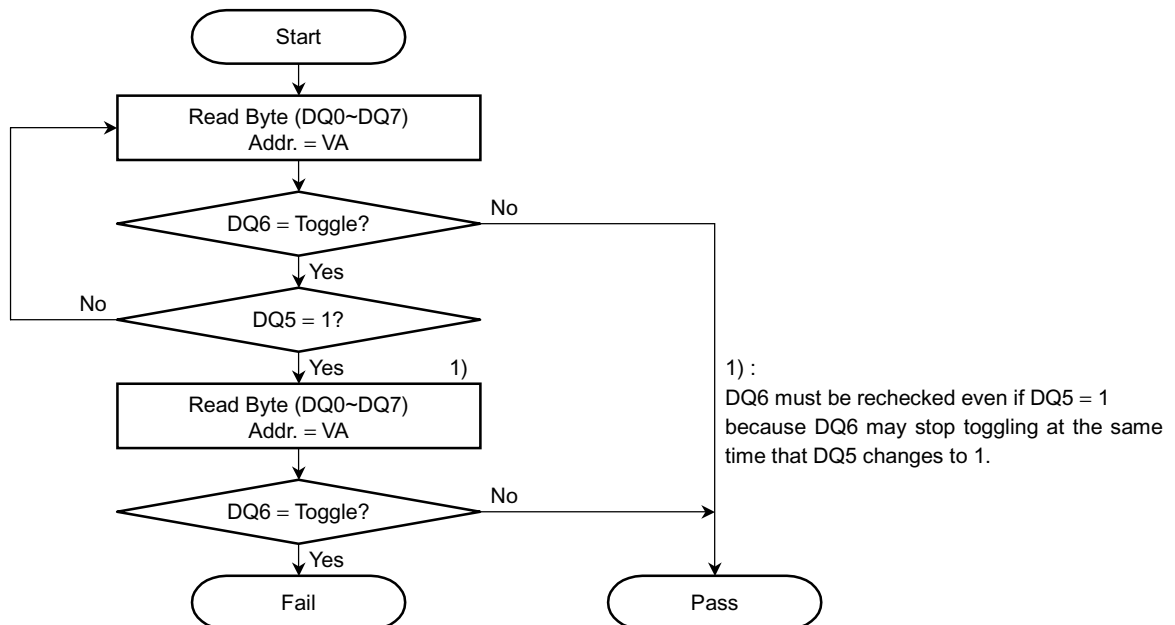


Note: Word mode command sequence is shown.

DQ7 ($\overline{\text{DATA}}$ Polling)



DQ6 (Toggle bit)



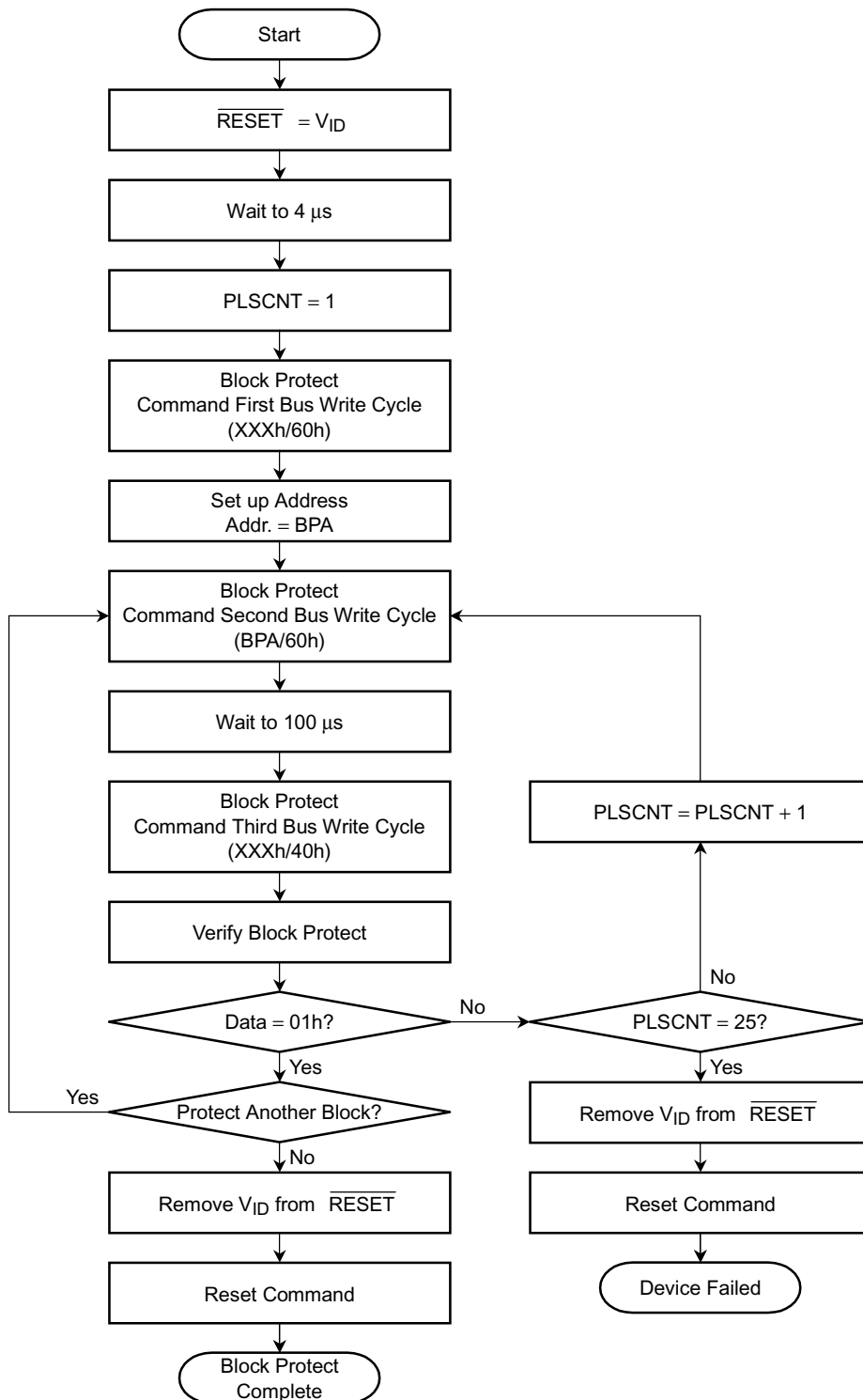
VA: Byte address for programming.

Any of the addresses within the block being erased during a Block Erase operation.

Don't care during a Chip Erase operation.

Any address not within the current block during an Erase Suspend operation.

Block Protect



BPA: Block Address and ID Read Address (A6, A1, A0)
 ID Read Address = (0, 1, 0)

PACKAGE DIMENSIONS

Unit: mm

P-FBGA69-1209-0.80A3

