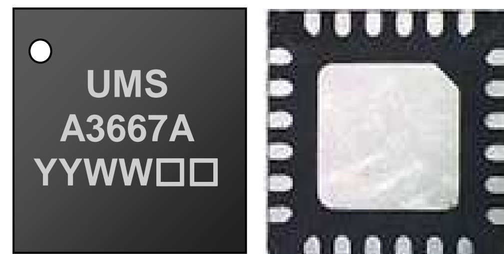
7-20GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD package

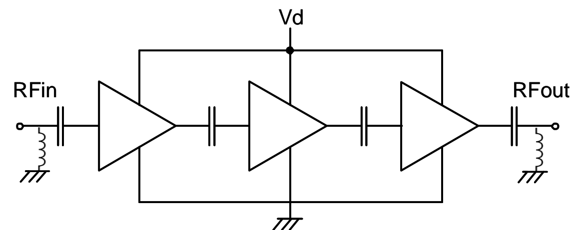
Description

The CHA3667aQDG is a wide band monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a Power-pHEMT process, 0.15µm gate length, via hole through the substrate.
It is ESD protected on RF ports thanks to DC specific filter circuits.
It is available in lead-free SMD package.



Main Features

- ■ Broadband performance 7-20GHz
- ■ Self-biased
- ■ 23dB gain @ 2.7dB noise figure
- ■ 20dBm Output power @1dBcp
- ■ DC power consumption, 175mA @ 4.2V
- ■ 24L-QFN4X4 SMD package
- ■ MSL1



Main Characteristics

Tamb = +25℃, Vd= 4.2V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Input frequency range	7		20	GHz
G	Small signal gain	21	23		dB
NF	Noise Figure		2.7	3.5	dB
P-1dB	Output power at 1dB gain compression	18.5	20		dBm
Id	Bias current	130	175	220	mA

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb = +25℃, Vd= 4.2V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		20	GHz
G	Gain				
	(7-8GHz)	19	20		dB
	(8-19GHz)	21	23		dB
	(19-20GHz)	19	20		dB
NF	Noise figure (7-18GHz)		2.7	3.5	dB
RLin	Input Return Loss				
	(7-19.5GHz)		-10	-8	dB
	(19.5-20GHz)		-8	-6	dB
RLout	Output Return Loss		-10	-8	dB
OIP3	Output IP3		28		dBm
P1dB	Pout at 1dB gain compression				
	(7-13GHz)		20		dBm
	(13-20GHz)		21		dBm
Isol	Reverse isolation		40		dB
Vd	Drain bias voltage		4.2		V
Id	Drain bias current	130	175	220	mA

These values are representative of on board measurements as defined on the drawing in paragraph “Evaluation board”.

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Absolute Maximum Ratings [1]

Tamb = +25℃

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Id	Power supply quiescent current	240	mA
Pin	RF input power (2)	3	dBm
Top	Operating temperature range	-40 to +85	℃
Tj	Junction temperature (3)	175	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration<1s

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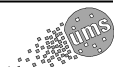


Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

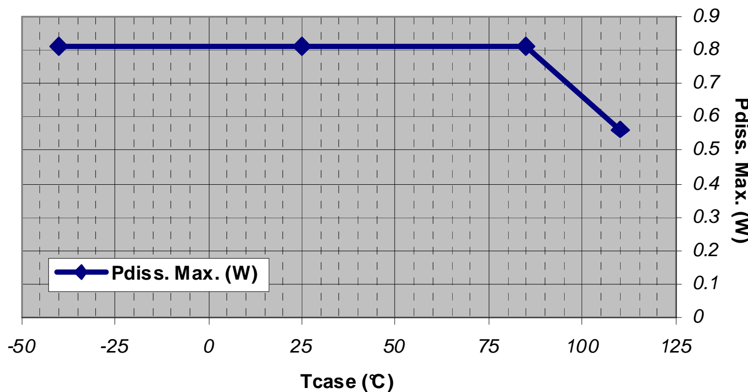
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

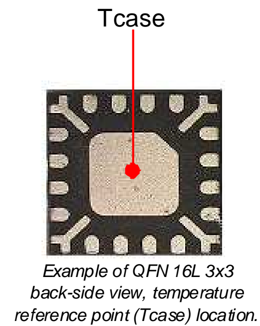
DEVICE THERMAL SPECIFICATION : CHA3667aQDG				
Recommanded max. junction temperature (Tj max)			:	167 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power @ Tcase=	85	°C	:	0.81 W
=> Pdiss derating above Tcase[(1)]=	85	°C	:	10 mW/°C
Junction-Case thermal resistance (Rth J-C)[(2)]			:	<100 °C/W
Min. package back side operating temperature[(3)]			:	-40 °C
Max. package back side operating temperature[(3)]			:	85 °C
Min. storage temperature			:	-55 °C
Max. storage temperature			:	125 °C

(1) Derating at junction temperature constant = Tj max

(2) Rth J-C is calculated for a worst case where the ***hotter junction*** *of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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Typical Package Sij parameters

Tamb = +25°C, Vd= 4.2V, Typical Id=175mA

FREQ (GHz)	S11 (dB)	Ph(S11) (°)	S21 dB	Ph(S21) (°)	S12 dB	Ph(S12) (°)	S22 dB	Ph(S22) (°)
1	-1.6	91.1	-64.6	-77.9	-74.9	-11.4	-1.7	95.7
2	-1.2	12.0	-43.4	-51.5	-80.6	-71.0	-1.6	16.6
3	-1.0	-57.5	-24.6	-99.2	-65.2	138.5	-1.8	-58.8
4	-1.1	-126.1	3.1	143.8	-65.6	11.7	-6.5	-120.6
5	-4.3	135.4	16.3	5.1	-67.4	59.6	-8.6	-144.5
6	-16.0	-42.1	19.8	-122.8	-70.3	4.7	-9.6	-173.4
7	**-12.7**	**-135.1**	**20.7**	**147.2**	**-74.9**	**173.9**	**-11.5**	**157.3**
8	**-13.2**	**-172.1**	**21.7**	**70.9**	**-61.5**	**94.7**	**-14.6**	**133.6**
9	**-15.4**	**167.2**	**22.3**	**2.8**	**-63.6**	**55.3**	**-18.9**	**122.4**
10	**-17.1**	**162.1**	**23.0**	**-62.5**	**-61.1**	**-4.2**	**-21.7**	**137.8**
11	**-16.2**	**155.7**	**23.3**	**-125.7**	**-63.3**	**-15.4**	**-19.7**	**141.6**
12	**-15.3**	**140.5**	**23.3**	**174.7**	**-69.4**	**-84.6**	**-19.8**	**124.6**
13	**-15.4**	**116.5**	**23.2**	**116.2**	**-66.5**	**140.1**	**-20.9**	**95.1**
14	**-16.4**	**93.2**	**22.8**	**61.6**	**-69.7**	**138.0**	**-27.5**	**33.8**
15	**-17.4**	**63.7**	**22.8**	**7.5**	**-60.5**	**161.0**	**-29.4**	**-74.4**
16	**-19.3**	**15.4**	**23.1**	**-46.7**	**-53.7**	**109.5**	**-22.8**	**-112.8**
17	**-18.0**	**-55.1**	**23.1**	**-103.7**	**-57.1**	**54.6**	**-20.4**	**-122.7**
18	**-13.3**	**-122.2**	**23.0**	**-163.7**	**-51.1**	**90.9**	**-17.0**	**-134.8**
19	**-9.1**	**-176.6**	**22.5**	**133.0**	**-48.0**	**48.6**	**-12.7**	**-149.2**
20	**-7.0**	**130.0**	**20.7**	**67.8**	**-47.3**	**13.1**	**-9.8**	**178.1**
21	-6.6	81.5	18.1	6.9	-55.3	-22.0	-8.8	144.9
22	-6.9	39.1	15.1	-50.4	-58.1	-24.0	-8.2	111.5
23	-7.3	0.9	12.1	-105.2	-47.8	92.8	-7.8	78.6
24	-7.6	-34.0	8.8	-161.0	-44.6	29.3	-7.4	48.1
25	-6.7	-68.1	4.8	140.6	-46.8	-7.3	-6.6	16.8
26	-6.0	-117.3	-2.4	86.8	-45.4	-8.8	-6.4	-19.3

The Sij measurement calibration planes are defined in the paragraph “Definition of the Sij reference planes”.

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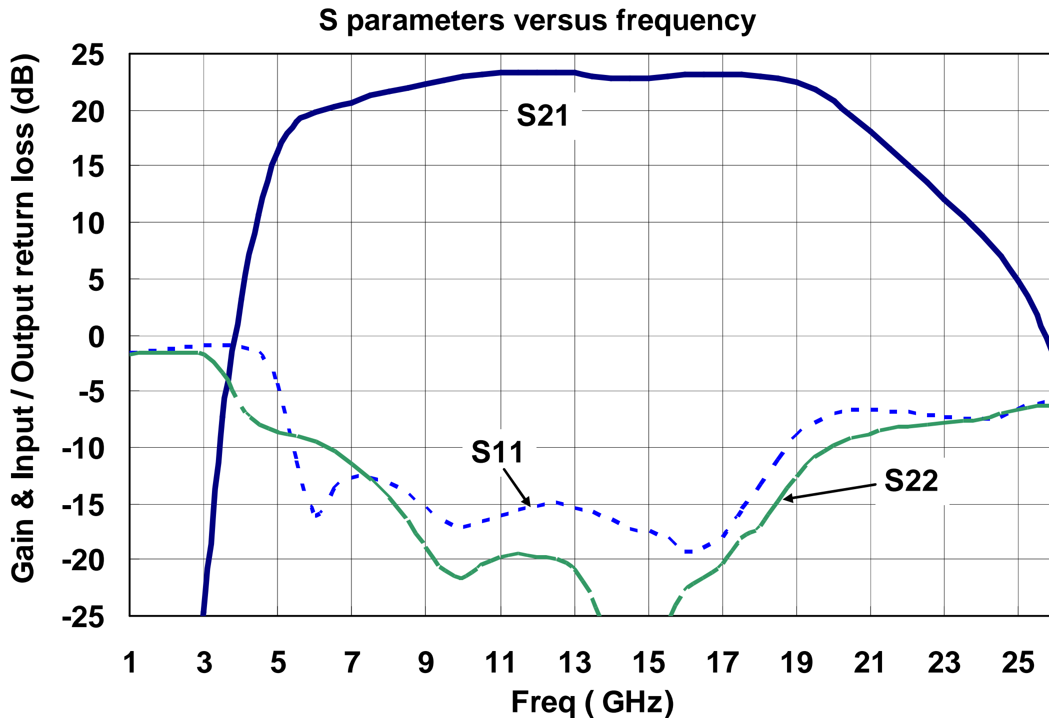
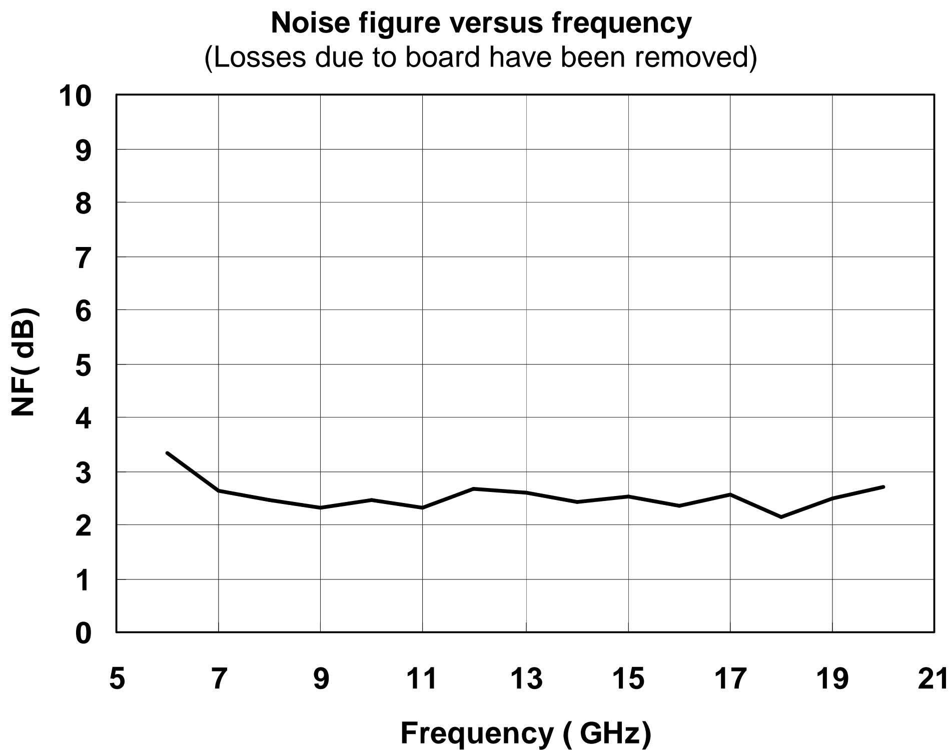
Typical Measured Performances

Tamb = +25℃, Vd= 4.2V, Typical Id=175mA
Measurements in the <u>package access plan</u>, using the proposed land pattern & board, as defined in paragraph *"Evaluation mother board:"*.





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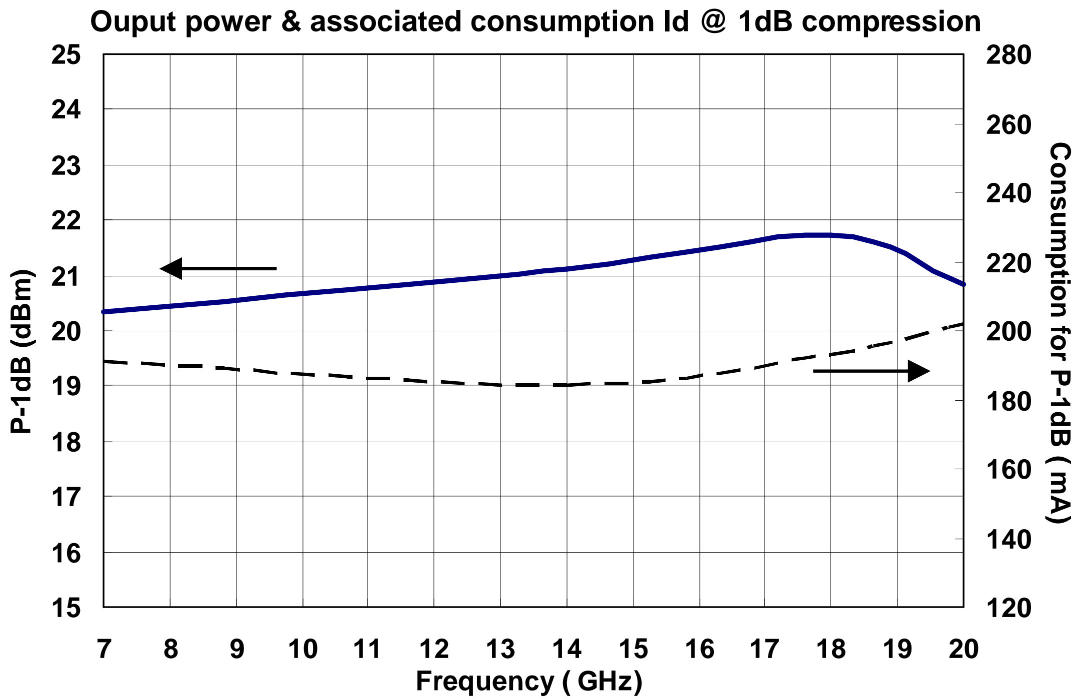
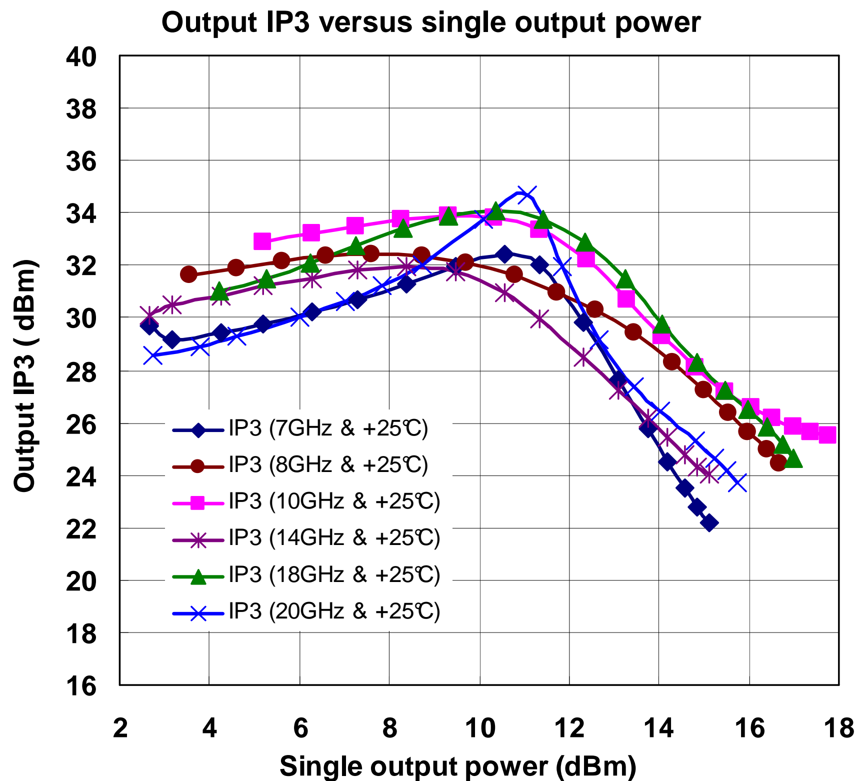
Typical Measured Performances

Tamb = +25°C, Vd= 4.2V, Typical Id=175mA
Measurements in the plan of the connectors, using the proposed land pattern & board, as defined in paragraph *"Evaluation mother board:".*





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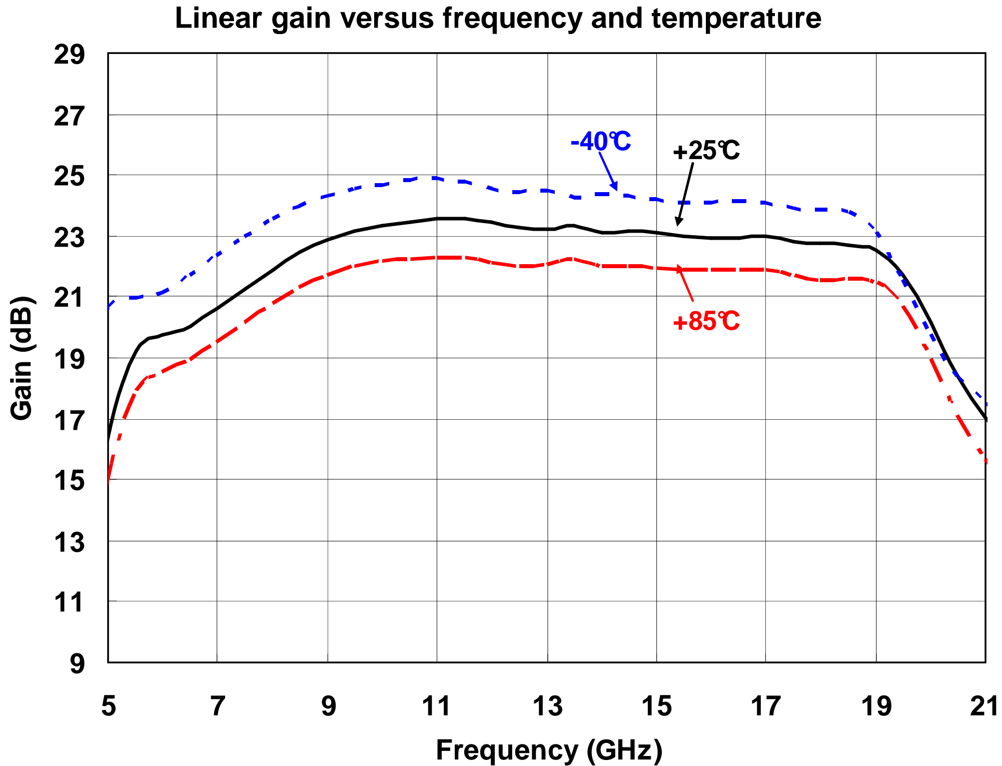
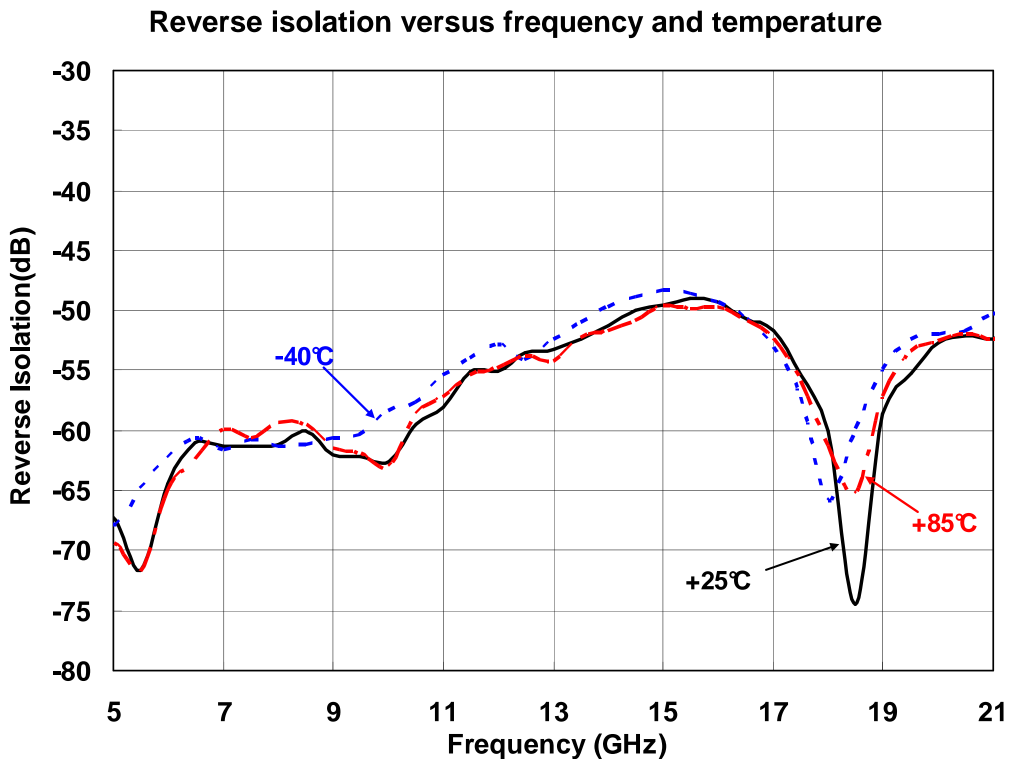
Typical Measured Performances in Temperature

Tamb = -40℃, +25℃, +85℃, Vd= 4.2V, Typical Id=17 5mA
Measurements in the plan of the connectors, using the proposed land pattern & board, as defined in paragraph *"Evaluation mother board:"*.





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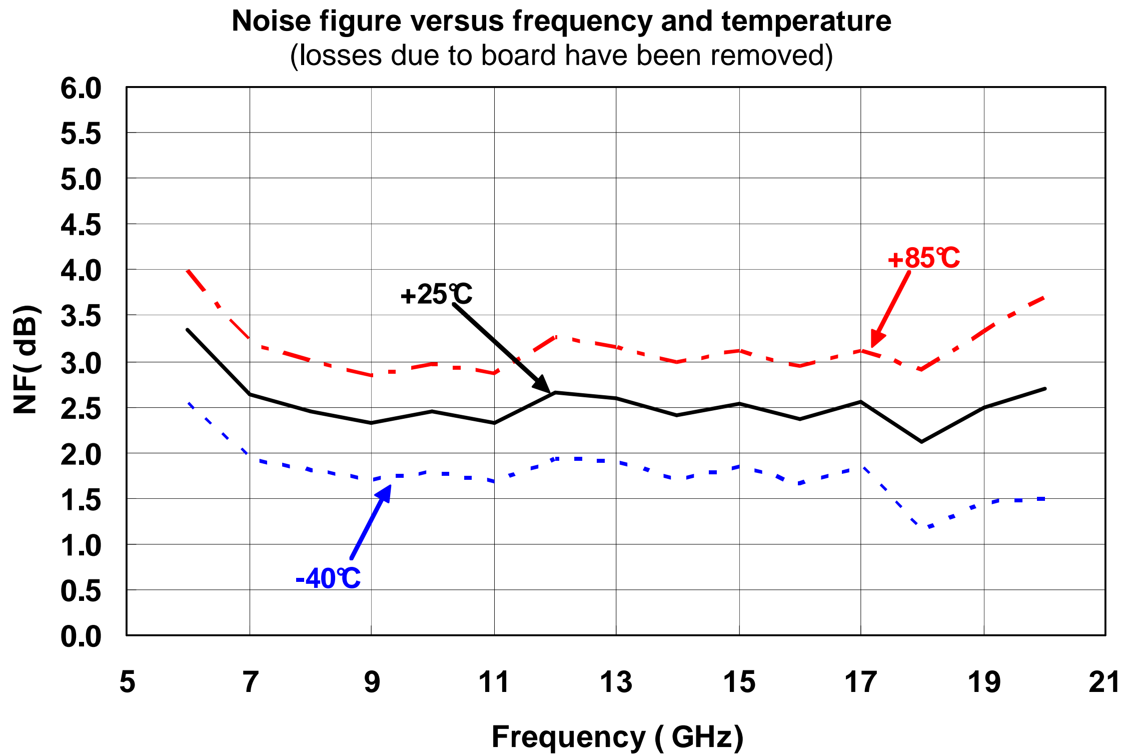

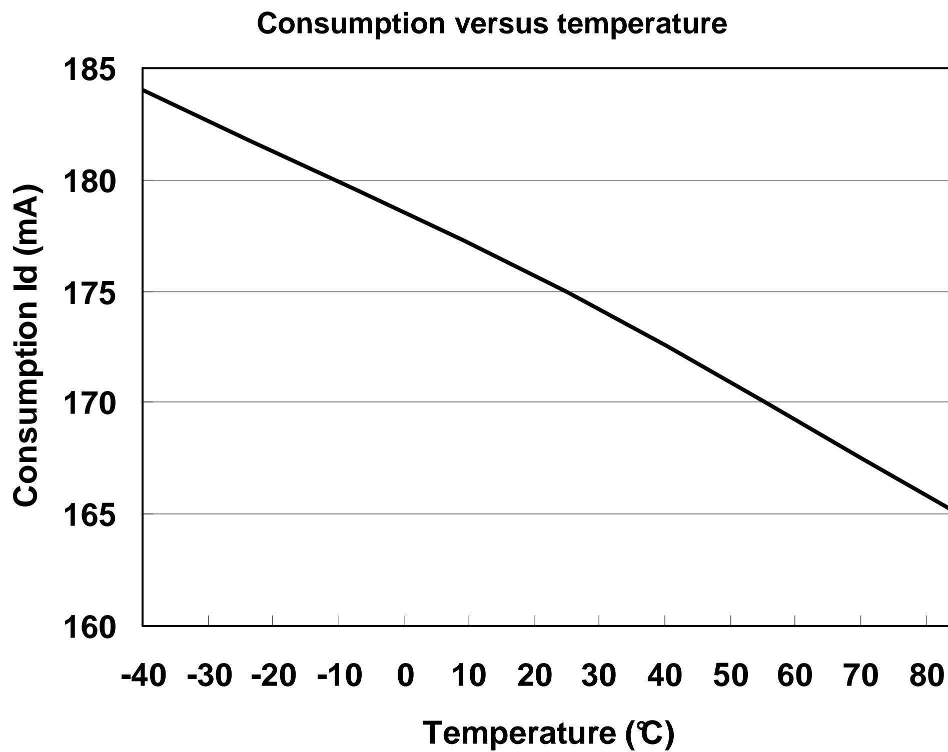

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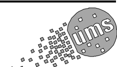

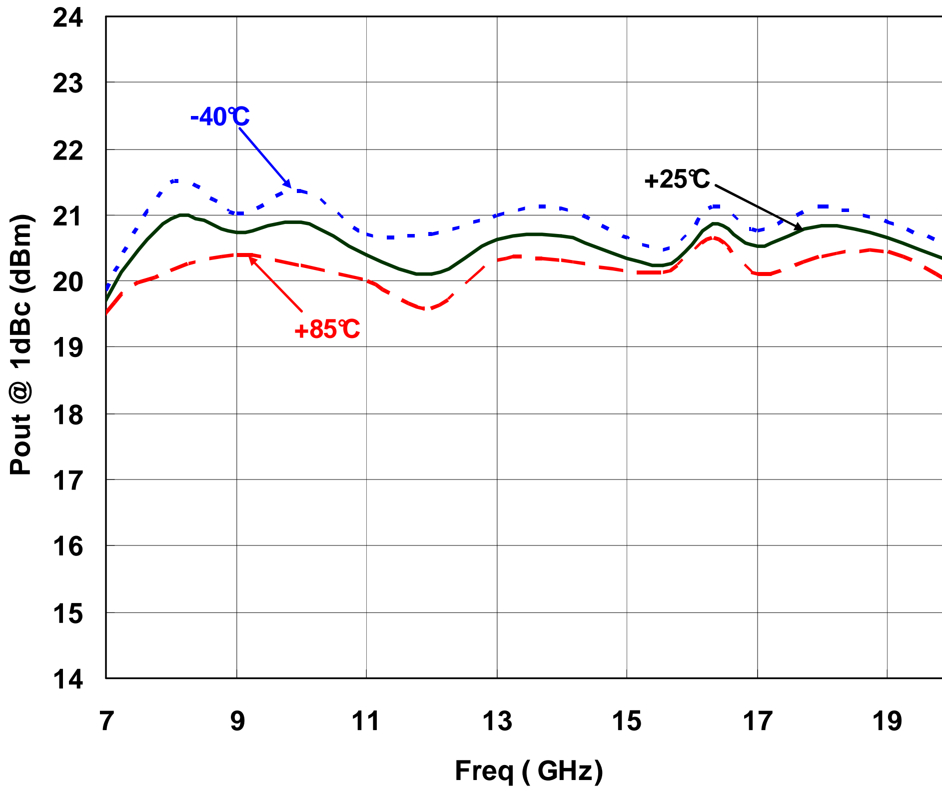

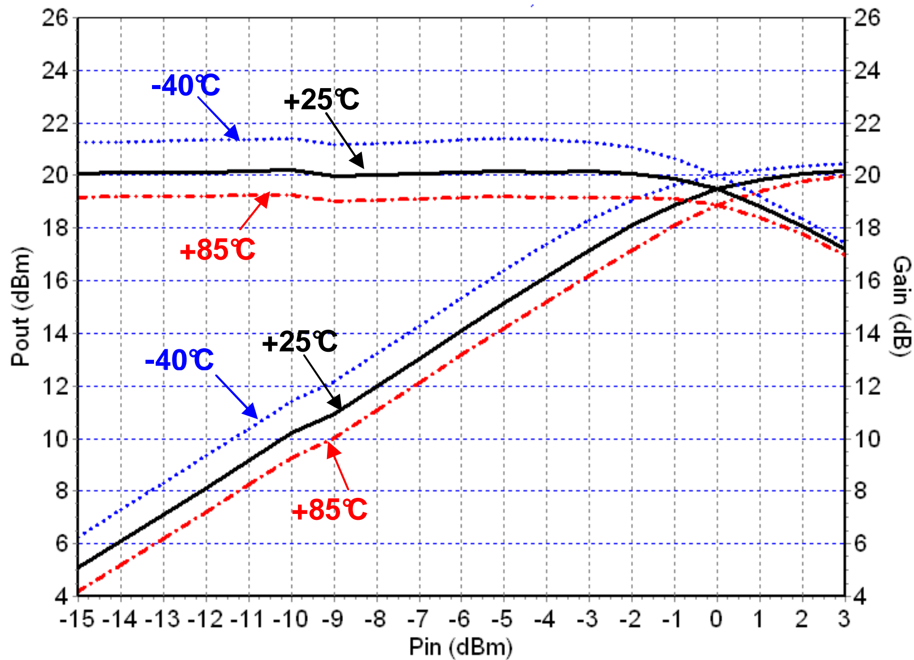

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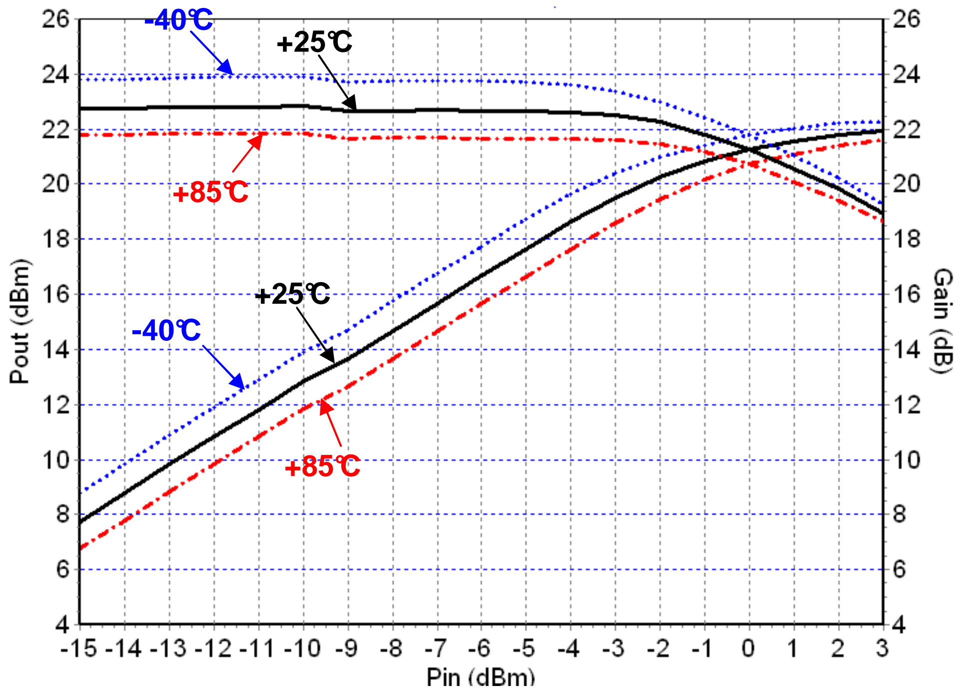
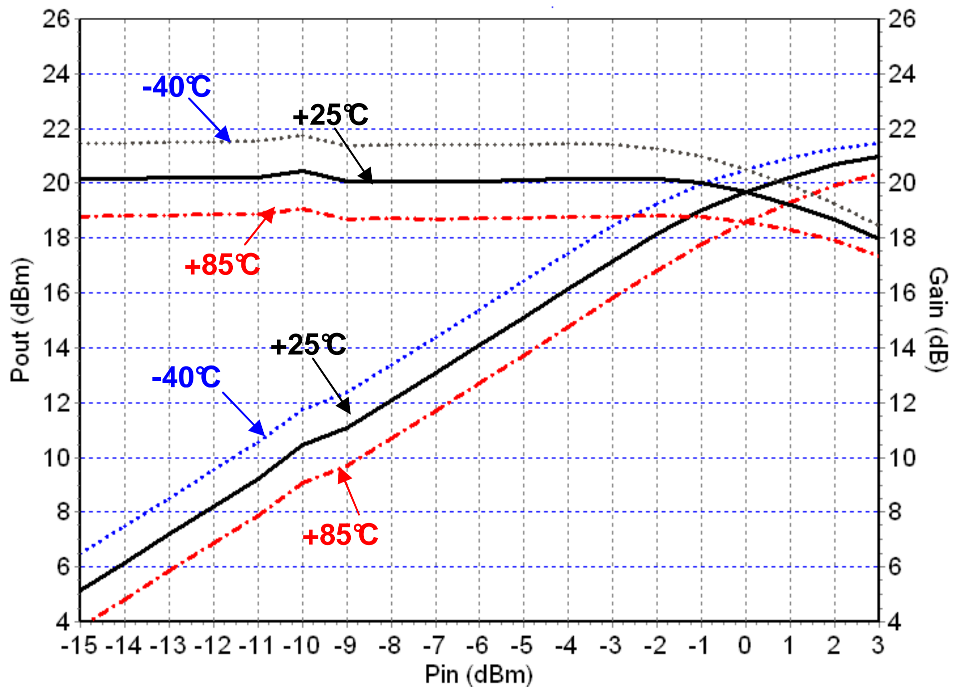
Gain and Pout versus frequency and temperature @ 16GHz



Gain and Pout versus frequency and temperature @ 20GHz



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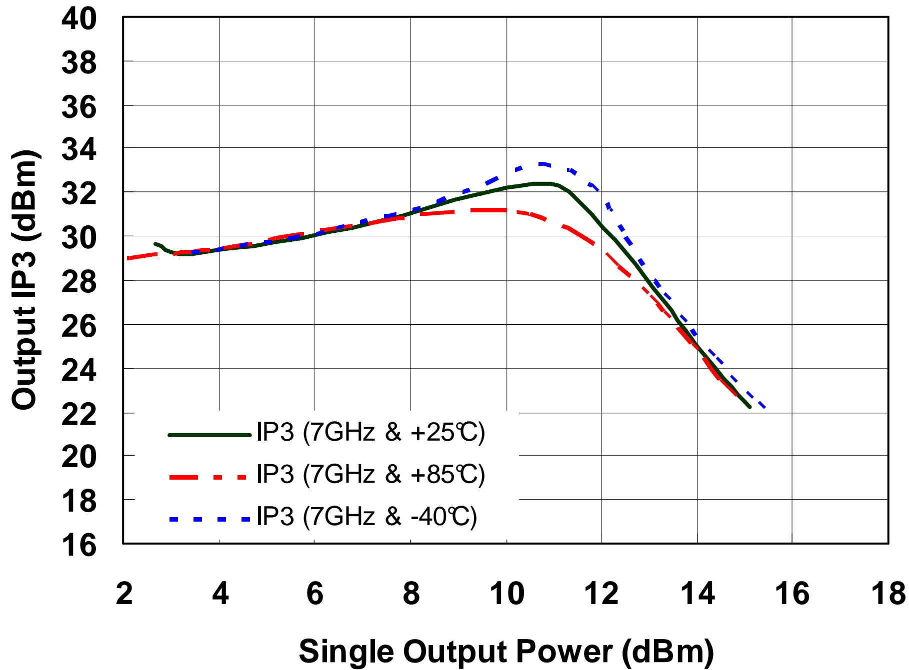
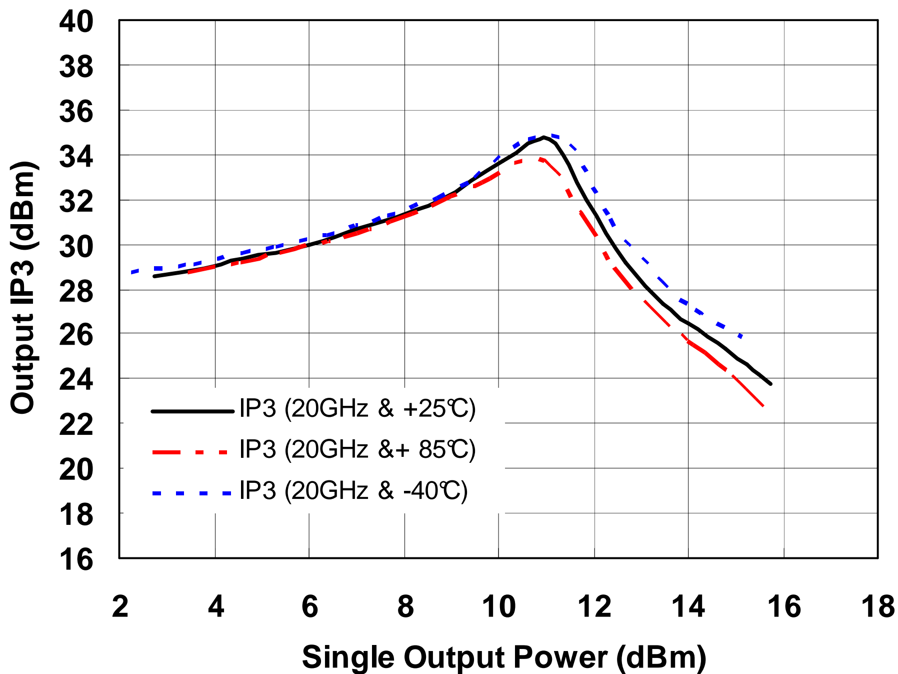
Output IP3 versus single output power and temperature @ 7GHz



Output IP3 versus single output power and temperature @ 20GHz



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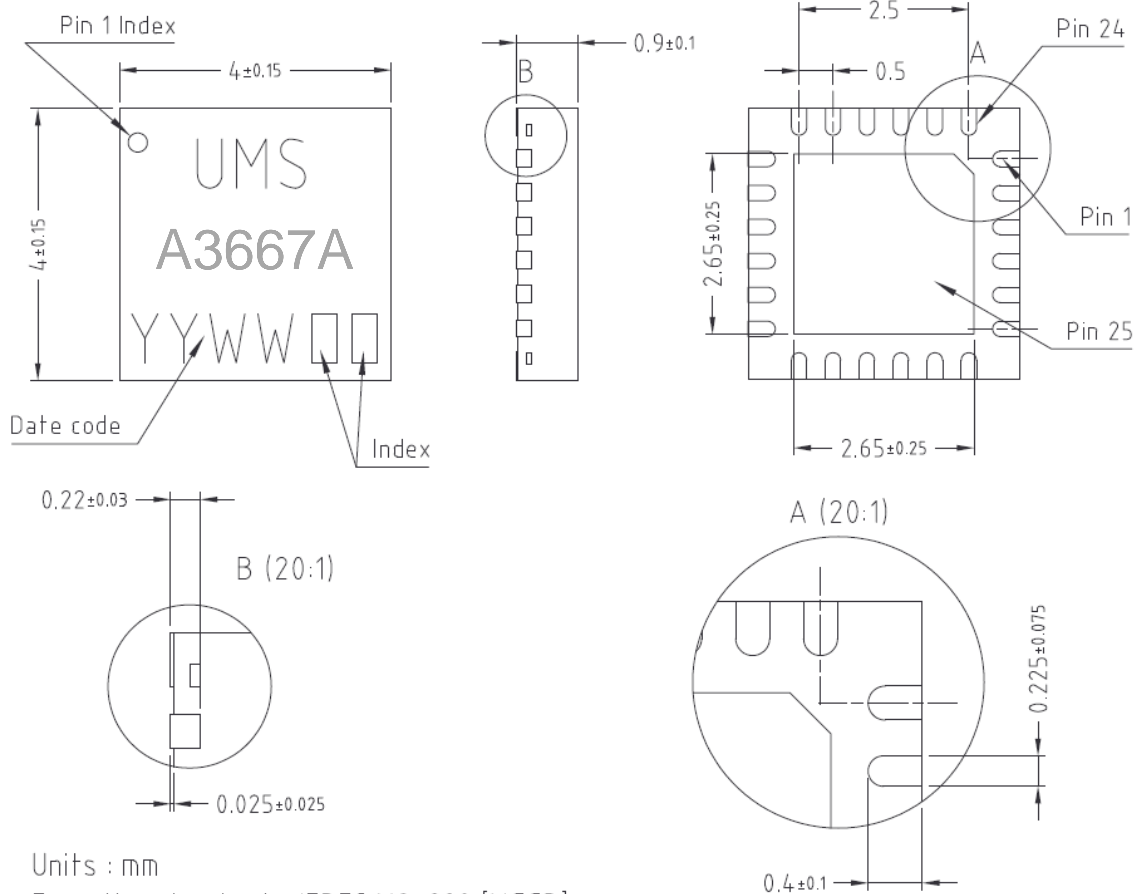
Package outline [1]



Matt tin, Lead Free	(Green)	1-	Nc	13-	Nc
Units	mm	2-	Nc	14-	Gnd
From the standard	JEDEC MO-220	3-	Gnd	15-	RF OUT
	(VGGD)	4-	RF IN	16-	Gnd
25- GND		5-	Gnd	17-	Nc
		6-	Nc	18-	Nc
		7-	Nc	19-	Nc
		8-	Nc	20-	VD
		9-	Nc	21-	Nc
		10-	Nc	22-	Nc
		11-	Nc	23-	Nc
		12-	Nc	24-	Nc

[1]The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.
It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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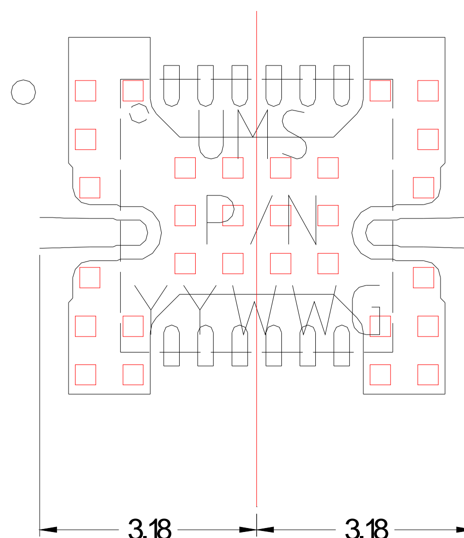
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

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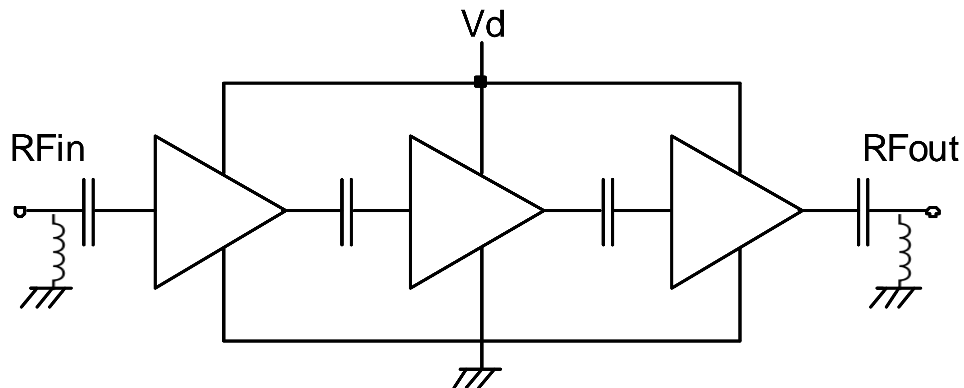
Notes

Due to ESD protection circuits, RFin and RFout are DC grounded and an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

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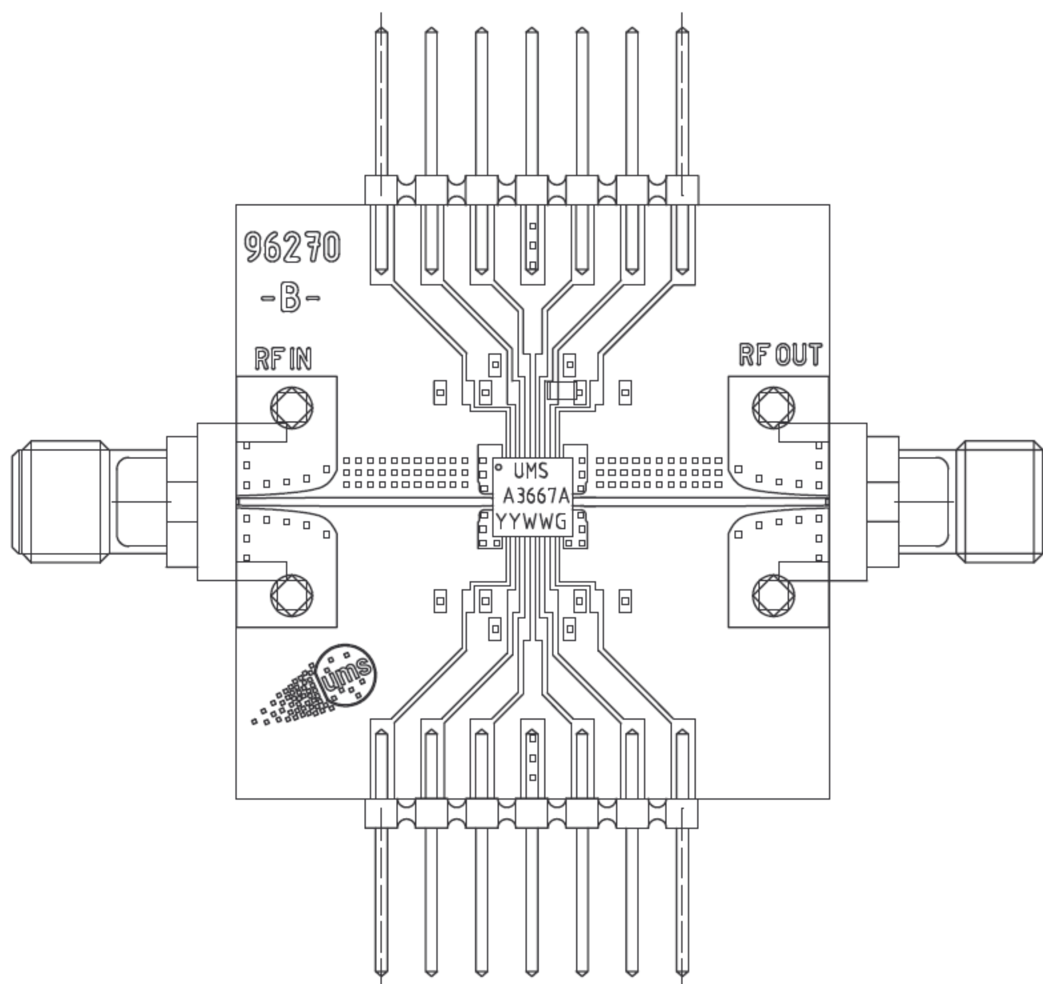
Evaluation mother board:

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



Ordering Information

QFN 4x4 RoHS compliant package: CHA3667aQDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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