POSEICO
POSEICO SPA
POwer SEmiconductors Italian COrporation

POSEICO SPA
Via Pillea 42-44, 16153 Genova - ITALY
Tel. + 39 010 8599400 - Fax + 39 010 8682006
Sales Office:
Tel. + 39 010 8599400 - Fax + 39 010 8681180

FAST SWITCHING THYRISTOR

ATF530

Repetitive voltage up to	**2000 V**
Mean on-state current	**1100 A**
Surge current	**15 kA**
Turn-off time	**50 µs**

TARGET SPECIFICATION

apr 06 - ISSUE : 0

Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	2000	V
V_{RSM}	Non-repetitive peak reverse voltage		125	2100	V
V_{DRM}	Repetitive peak off-state voltage		125	2000	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	75	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	75	mA
CONDUCTING					
$I_{T(AV)}$	Mean on-state current	180° sin, 50 Hz,Th=55°C, doubl e side cooled		1100	A
$I_{T(AV)}$	Mean on-state current	180° sin, 1 kHz,Tc=85°C, doub le side cooled		900	A
I_{TSM}	Surge on-state current, non repetitive	sine wave, 10 ms	125	15	kA
I^2t	I^2t	without reverse voltage		1125 x1E3	A^2s
V_T	On-state voltage	On-state current = 2000 A	25	2,25	V
$V_{T(TO)}$	Threshold voltage		125	1,30	V
r_T	On-state slope resistance		125	0,410	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min	From 50% VDRM	125	800	A/µs
dv/dt	Critical rate of rise of off-state voltage, min	Linear ramp up to 70% of VDRM	125	500	V/µs
td	Gate controlled delay time, typical	VD=VDRM, gate source 20V, 20 ohm , tr=0.1 µs	25	1,5	µs
tq	Circuit commutated turn-off time	di/dt = 20 A/µs, I = 800 A dV/dt = 200 V/µs , up to 75% VDRM	125	50	µs
Q rr	Reverse recovery charge	di/dt = 60 A/µs, I = 1000 A	125	620	µC
I rr	Peak reverse recovery current	VR = 50 V		300	A
I_H	Holding current, typical	VD=5V, gate open circuit	25	500	mA
I_L	Latching current, typical	VD=5V, tp=30µs	25	1000	mA
GATE					
V_{GT}	Gate trigger voltage	VD=6V	25	3,0	V
I_{GT}	Gate trigger current	VD=6V	25	150	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,3	V
V_{FGM}	Peak gate voltage (forward)		25	30	V
I_{FGM}	Peak gate current		25	10	A
V_{RGM}	Peak gate voltage (reverse)		25	5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs	25	200	W
$P_{G(AV)}$	Average gate power dissipation		25	3	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		26	°C/kW
$R_{th(c-h)}$	Thermal impedance, DC	Case to heatsink, double side cooled		6	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			14.0 / 17.0	kN
	Mass			500	g

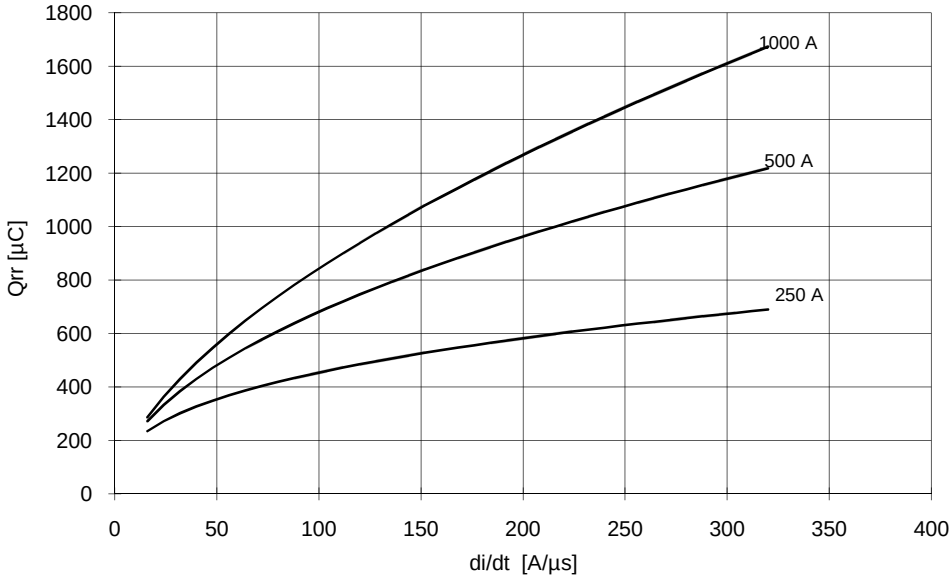
ORDERING INFORMATION : ATF530 S 20 S — tq code; standard specification; VDRM&VRRM/100

tq code

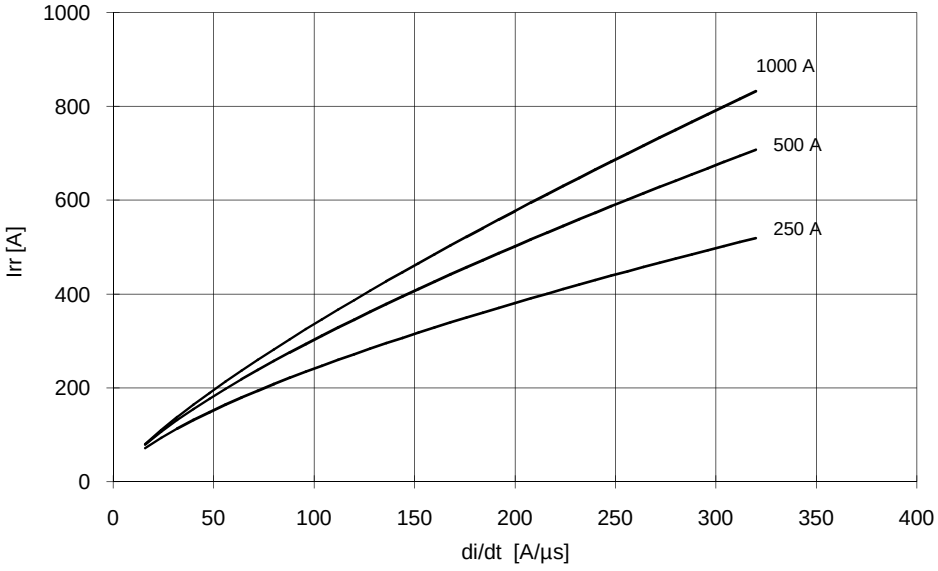
D 10 µs	C 12 µs	B 15 µs	A 20 µs	L 25 µs
M 30 µs	N 35 µs	P 40 µs	R 45 µs	S 50 µs
T 60 µs	U 70 µs	W 80 µs	X 100µs	Y 150µs

SWITCHING CHARACTERISTICS

REVERSE RECOVERY CHARGE
Tj = 125 °C



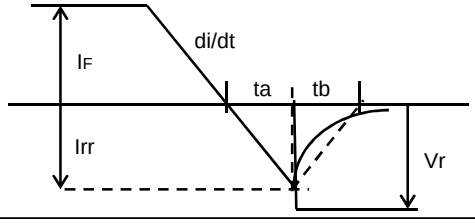
REVERSE RECOVERY CURRENT
Tj = 125 °C



ta = Irr / (di/dt) tb = trr - ta

Softness (s factor) s = tb / ta

Energy dissipation during recovery Er = Vr · (Qrr - Irr ·ta / 2)

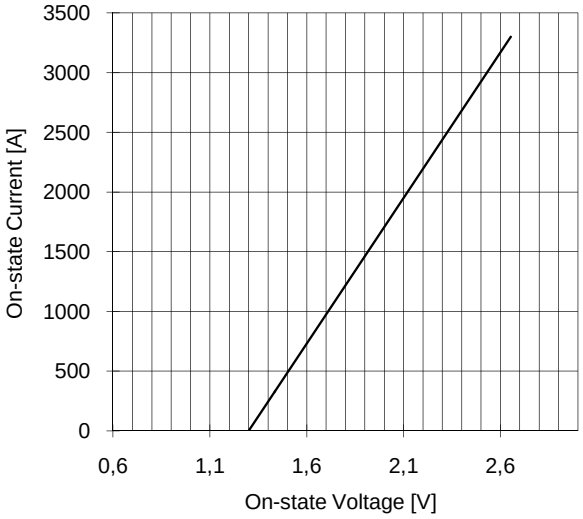


ATF530 FAST SWITCHING THYRISTOR

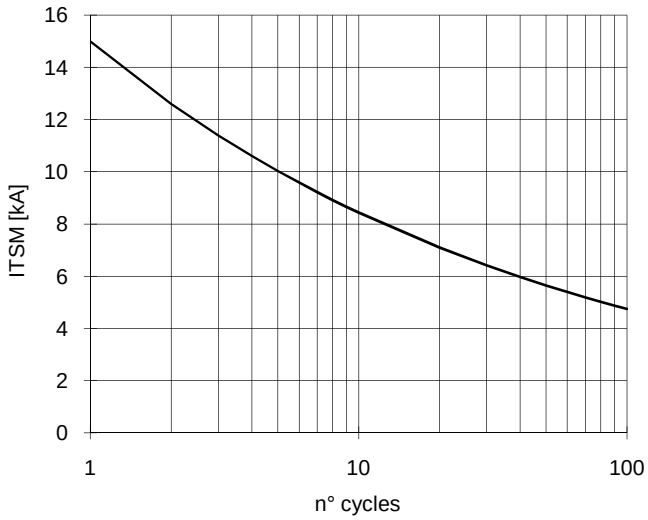
POSEICO SPA
POwer SEmiconductors Italian COrporation

TARGET SPECIFICATION apr 06 - ISSUE : 0

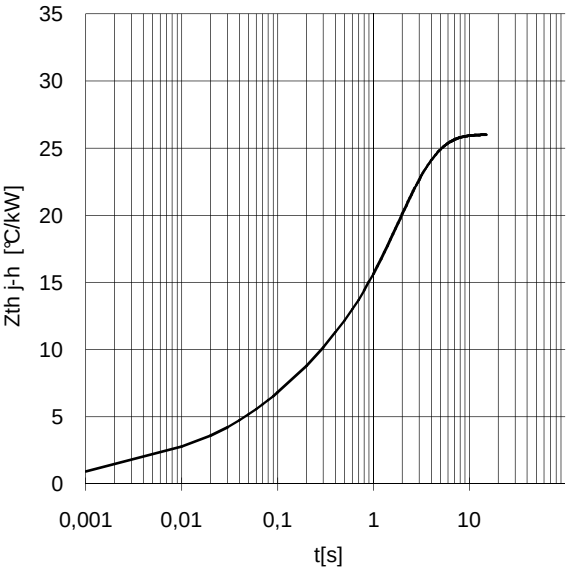
ON-STATE CHARACTERISTIC
Tj = 125 ℃

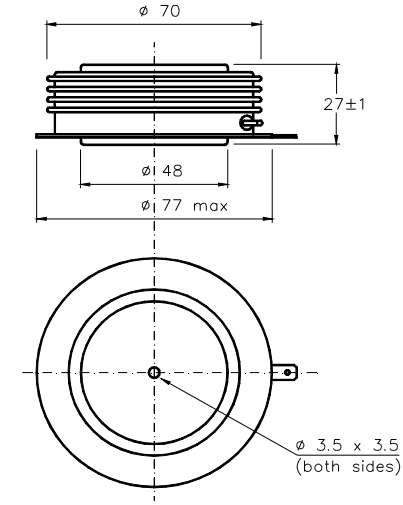


SURGE CHARACTERISTIC
Tj = 125 ℃



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Dimensions in mm

Cathode terminal type DIN 46244 - A 4.8 - 0.8
Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

Distributed by