

25mW Stereo Cap-Free Headphone Driver

Features

- **Operating Voltage: 2.4V~5.5V**
- **Supply Current**
 - $I_{DD}=2.1\text{mA}$ at $V_{DD}=3.6\text{V}$
- **Low Shutdown Current**
 - $I_{DD}=0.7\text{mA}$ at $V_{DD}=3.6\text{V}$
- **Ground Reference Output**
 - **No Output Capacitor Required (for DC Blocking)**
 - **Save the PCB Space**
 - **Reduce the BOM Costs**
 - **Improve the Low Frequency Response**
- **Output Power**
 - 25mW/Ch into 16 Ω at $V_{DD}=3.6\text{V}$, THD+N=0.04%**
 - 20mW/Ch into 32 Ω at $V_{DD}=3.6\text{V}$, THD+N=0.02%**
- **High PSRR: 90dB at 217Hz**
- **Fast Start-Up Time: 4ms**
- **Integrate the De-pop Circuitry**
- **Thermal Protection**
- **Surface-Mount Packaging**
 - WLCSP1.6x1.6-16**
 - TQFN3x3-16**

Applications

- **Handsets**
- **PDA's**
- **Portable Multimedia Devices**
- **Notebooks**

General Description

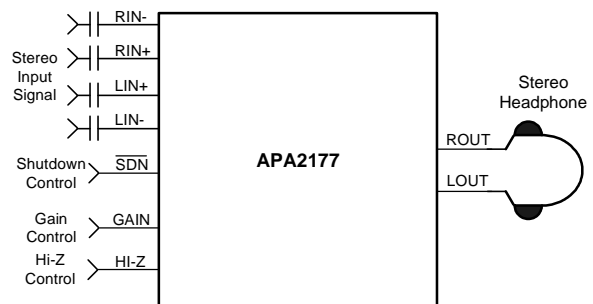
The APA2177 is a stereo, fixed gain, single supply, and cap-free headphone driver, which is available in a WLCSP-16 packages.

The APA2177 is ground-reference output, and no need the output capacitors for DC blocking. The advantages of eliminating the output capacitor are saving the cost, eliminating component height, and improving the low frequency response.

The internal selectable gain (0dB or 6dB) can minimize the external component counts and save the PCB space. High PSRR provides increased immunity to noise and RF rectification.

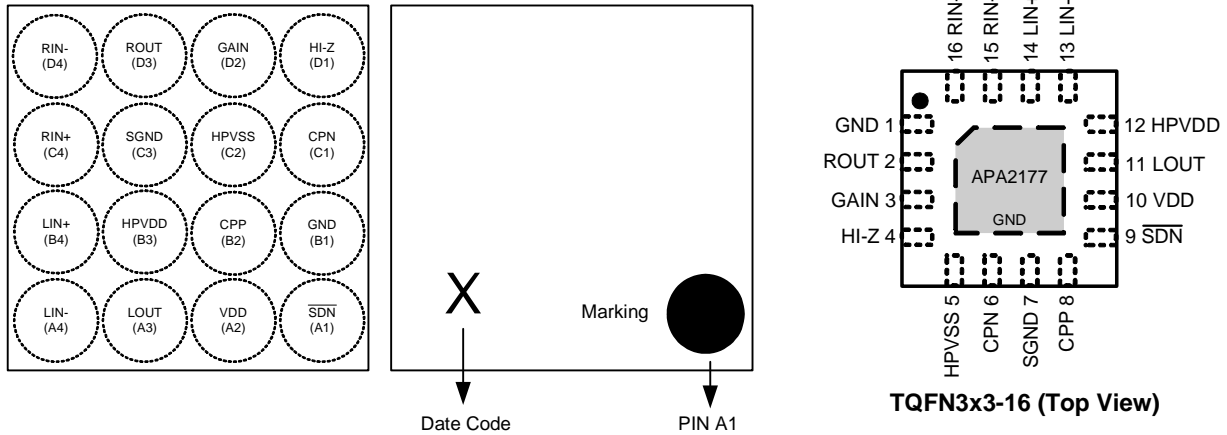
The APA2177 is capable of driving 25mW at 3.6V into 16 Ω load and provides thermal protection.

Simplified Application Circuit



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration



Ordering and Marking Information

<p>APA2177 □□□-□□□</p> <ul style="list-style-type: none"> — Assembly Material — Handling Code — Temperature Range — Package Code 	<p>Package Code HA: WLCSP-16 QB: TQFN3x3-16 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device</p>
<p>APA2177 HA : </p>	<p>X - Date Code</p>
<p>APA2177 QB : </p>	<p>XXXXX - Date Code</p>

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{PGND_GND}	PGND to GND Voltage	-0.3 to 0.3	V
V_{DD}	Supply Voltage (VDD to GND and SGND)	-0.3 to 6.0	
HPV_{DD}	Headphone Amplifier Supply Voltage (HPV _{DD} to GND and SGND)	-0.3 to 2.3	
V_{SDN}	Input Voltage (/SDN to GND)	GND-0.3 to V _{DD} +0.3	
V_{GAIN}	Input Voltage (GAIN to GND)	GND-0.3 to V _{DD} +0.3	
V_{HI-Z}	Input Voltage (HI-Z to GND)	GND-0.3 to V _{DD} +0.3	
HPV_{SS}	HPV _{SS} to GND and SGND Voltage	-2.3 to 0.3	

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
V _{OUT}	ROUT and LOU to GND Voltage	HPV _{SS} -0.3 to HPV _{DD} +0.3	V
V _{CPP}	CPP to GND Voltage	GND-0.3 to HPV _{DD} +0.3	
V _{CPN}	CPN to GND Voltage	HPPV _{SS} -0.3 to GND+0.3	
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-65 to +150	
T _{SDR}	Maximum Soldering Temperature Range	260, 10 seconds	
P _D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ _{JA}	Thermal Resistance - Junction to Ambient ^(Note 2)	WLCSP-16	160
		TQFN3x3-16	55

Note 2: Please refer to "Thermal Consideration". 2 layered printed circuit boards with 2oz trace and copper through several thermal vias. The thermal pad is soldered on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit	
V _{DD}	Supply Voltage	2.4 ~ 5.5	V	
V _{IH}	High Level Threshold Voltage	SDN, GAIN, HI-Z		1.3 ~ V _{DD}
V _{IL}	Low Level Threshold Voltage	SDN, GAIN, HI-Z		0 ~ 0.6
	Voltage applied to Output; OUTR, OUTL (when SDN = 0 V)			-0.3 ~ 3.6
	Voltage applied to Output; OUTR, OUTL (when SDN ≥ 1.3 V and HI-Z ≥ 1.3 V)			-1.8 ~ 1.8
T _A	Operating Ambient Temperature Range		-40 ~ 85	°C
T _J	Operating Junction Temperature Range		-40 ~ 125	
R _L	Headphone Resistance		16 ~ 100k	Ω

Electrical Characteristics

V_{DD}=3.6V, V_{GND}=V_{PGND}=0V, V_{/SDN}=V_{DD}, C_{CPF}=C_{CPO}=1μF, C_i=1μF, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2177			Unit
			Min.	Typ.	Max.	
I _{DD}	V _{DD} Supply Current		-	2.5	3.5	mA
I _{SD}	V _{DD} Shutdown Current	V _{SDN} =0V	-	1	2	μA
I _i	Input current	SDN	-	0.1	-	
CHARGE PUMP						
f _{OSC}	Switching Frequency		400	500	600	kHz
R _{eq}	Equivalent Resistance		-	15	-	Ω

Electrical Characteristics (Cont.)

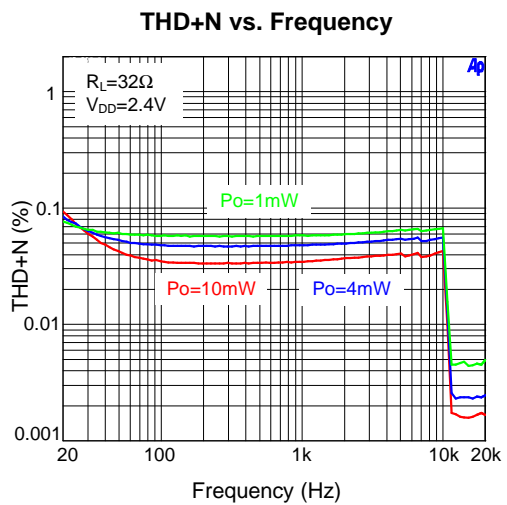
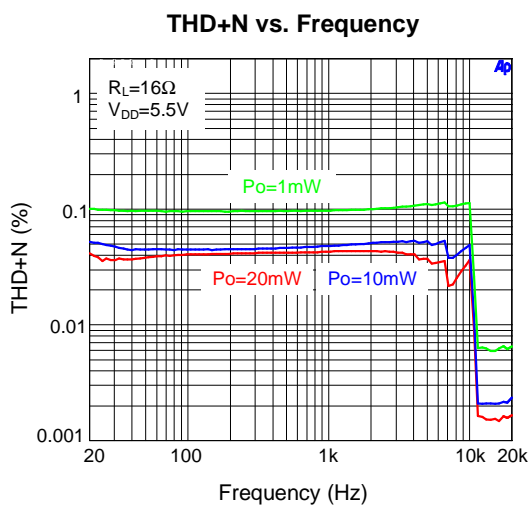
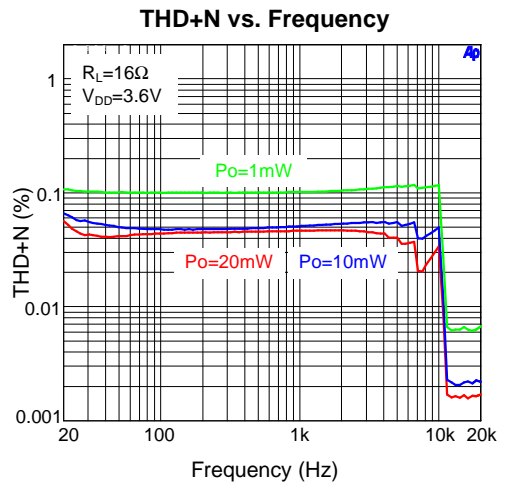
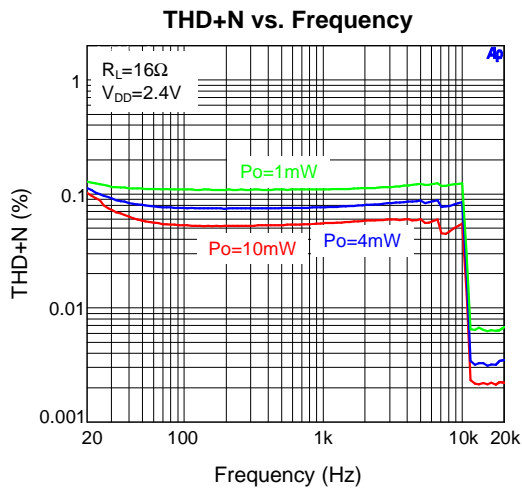
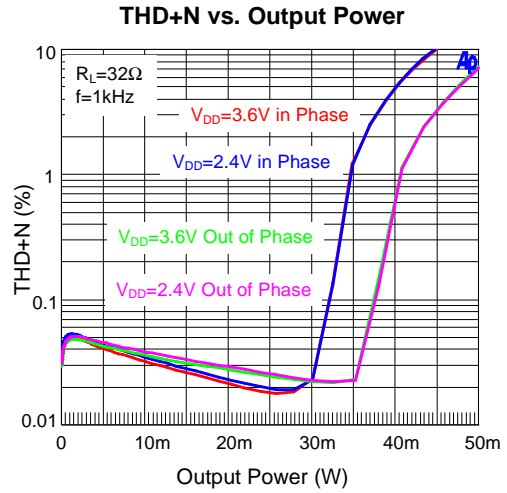
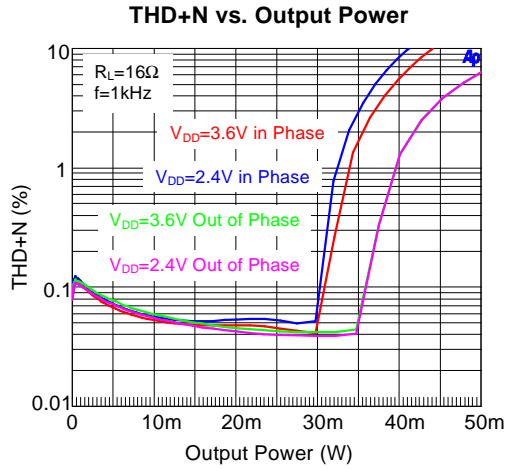
$V_{DD}=3.6V$, $V_{GND}=V_{PGND}=0V$, $V_{/SDN}=V_{DD}$, $C_{CPF}=C_{CPO}=1\mu F$, $C_i=1\mu F$, $T_A=25^\circ C$ (unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
Drivers							
A_V	Internal Voltage Gain	$V_{GAIN}=0V$, No Load	-0.95	-1.0	-1.05	V/V	
		$V_{GAIN} \geq 1.3V$, No Load	-1.95	-2.0	-2.05		
ΔA_V	Gain Matching		-	1	-	%	
R_i	Input Resistance	GAIN = 0V(0dB)	-	19.8	-	k Ω	
		GAIN $\geq 1.3V$ (6dB)	-	13.2	-		
	Input Resistance in shutdown	SDN = 0V	-	10	-		
Z_o	Output Impedance	SDN = HI-Z $\geq 1.3V$, $f_{in}=10kHz$	-	35	-	k Ω	
		SDN = HI-Z $\geq 1.3V$, $f_{in}=1MHz$	-	17	-		
		SDN = 0 V (shutdown mode)	-	25	-	Ω	
V_{OS}	Output Offset Voltage	$V_{DD}=2.5V$ to $5.5V$, $R_L = 16\Omega$	-	0.5	-	mV	
V_N	Output Noise		-	7	-	μV_{RMS}	
PSRR	Power Supply Rejection Ratio	$V_{tr}=0.2V_{PP}$, $R_L=16\Omega$, input AC-Ground	$f_{in}= 217Hz$	-	-90	-	dB
			$f_{in}= 10kHz$	-	-80	-	
C_L	Maximum Capacitive Load		-	220	-	pF	
$T_{start-up}$	Start up time		-	4	-	ms	
V_{ESD}	ESD Protection	OUTR, OUTL	-	8	-	kV	
P_o	Output Power (Stereo, In Phase)	THD+N=1%, $f_{in}=1kHz$	$R_L=16\Omega$	-	25	-	mW
			$R_L=32\Omega$	-	22	-	
V_o	Output Voltage (Stereo, In Phase)	THD+N=1%, $f_{in}=1kHz$, $R_L=100\Omega$	-	1.1	-	V_{RMS}	
THD+N	Total Harmonic Distortion Pulse Noise	$P_o=20mW$, $R_L=16\Omega$, $f_{in}=1kHz$	-	0.04	-	%	
		$P_o=25mW$, $R_L=32\Omega$, $V_{DD}=5.5V$, $f_{in}=1kHz$	-	0.02	-		
Crosstalk	Channel separation	$P_o=20mW$, $R_L=16\Omega$ $f_{in}=1kHz$	-	80	-	dB	
$Att_{shutdown}$	Shutdown Attenuation	$f_{in} = 1kHz$, $R_L=16\Omega$, $V_{in}=1V_{rms}$	-	80	-		
S/N		$P_o=20mW$, $R_L=16\Omega$ GAIN = 0V(AV=0dB), With A-weighting Filter	-	95	-		

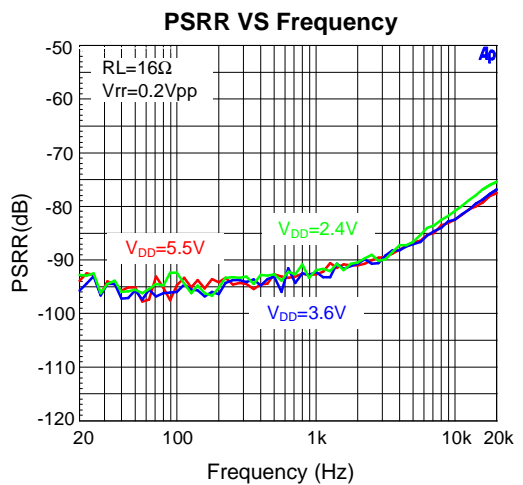
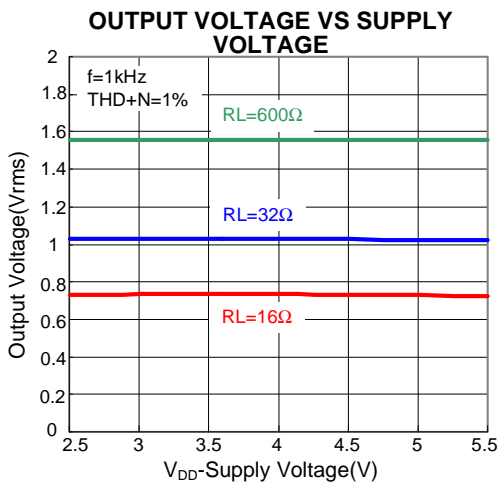
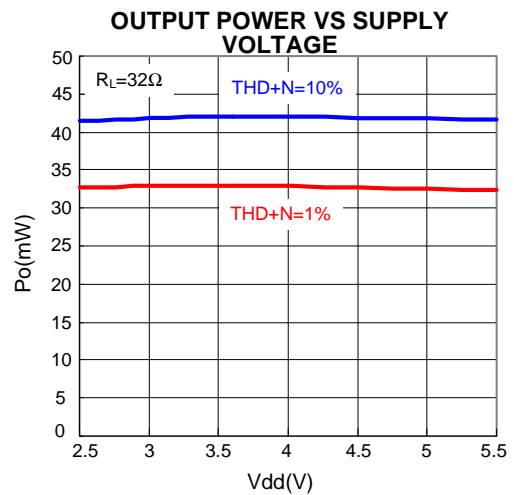
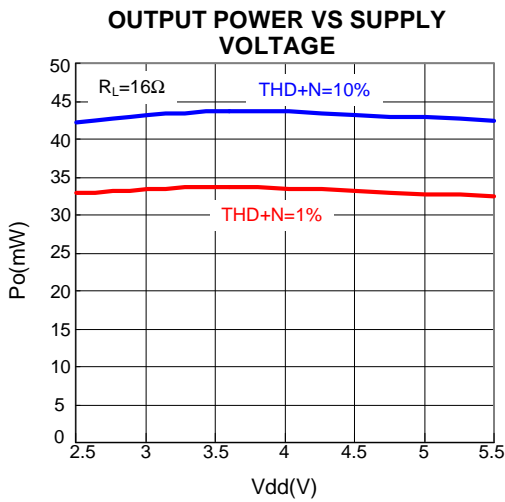
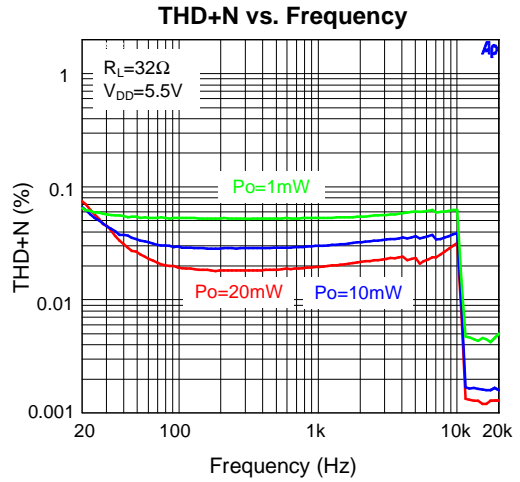
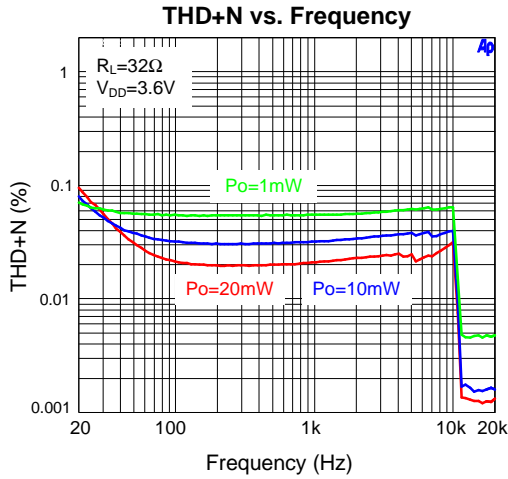
Pin Description

PIN			I/O/P	Function Description
TQFN3x3-16	WLCSP	Name		
9	A1	$\overline{\text{SDN}}$	I	Shutdown mode control pin. A low-level voltage applied on this pin shuts off the headphone driver.
10	A2	VDD	P	Supply voltage input pin.
11	A3	LOUT	O	Left channel output for headphone.
13	A4	LIN-	I	Left channel audio signal inverting input pin.
1	B1	GND	P	Ground connection for circuitry.
8	B2	CPP	P	Charge pump flying capacitor positive connection.
12	B3	HPVDD	P	Positive power supply for headphone amplifiers.
14	B4	LIN+	I	Left channel audio signal non-inverting input pin.
6	C1	CPN	P	Charge pump flying capacitor negative connection.
5	C2	HPVSS	P	Charge pump output.
7	C3	SGND	I	Amplifier reference voltage.
15	C4	RIN+	I	Right channel audio signal non-inverting input pin.
4	D1	HI-Z	I	Output impedance select. Set to logic LOW for normal operation and logic HIGH for high output impedance.
3	D2	GAIN	I	Gain select. Set to logic LOW for a gain of 0dB and to HIGH for a gain of 6dB.
2	D3	ROUT	O	Right channel output for headphone.
16	D4	RIN-	I	Right channel audio signal inverting input pin.

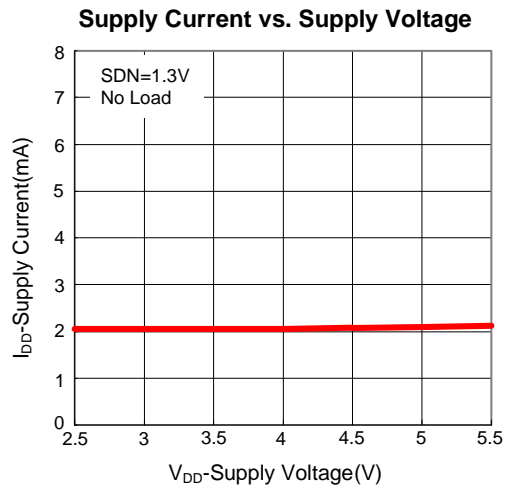
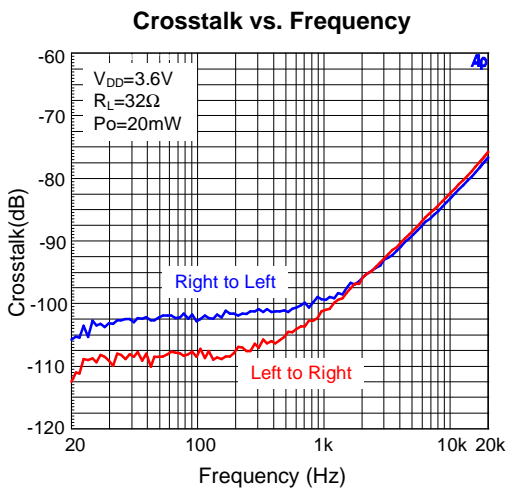
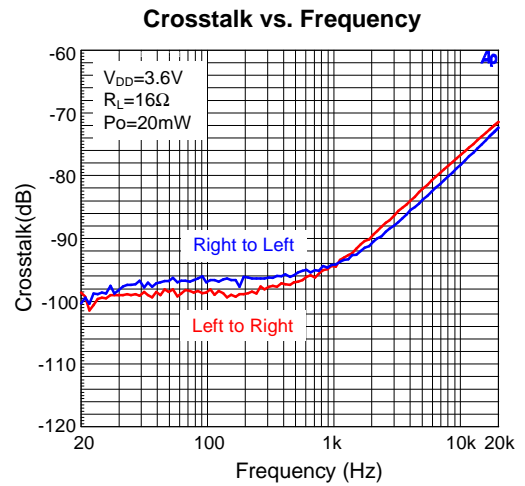
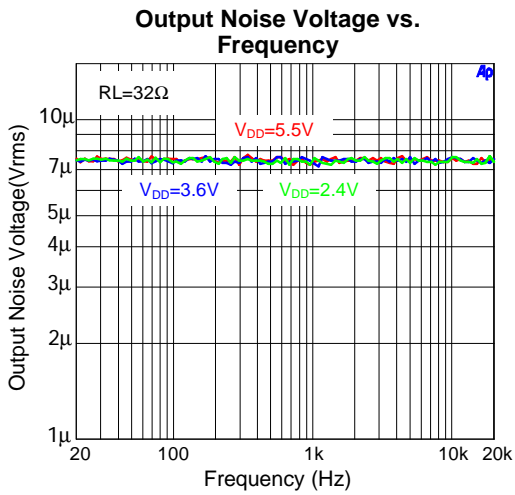
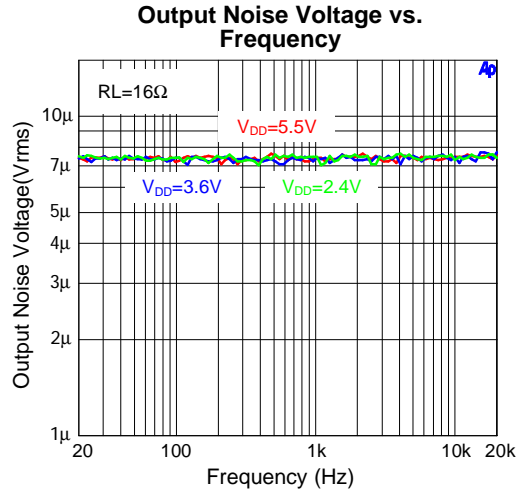
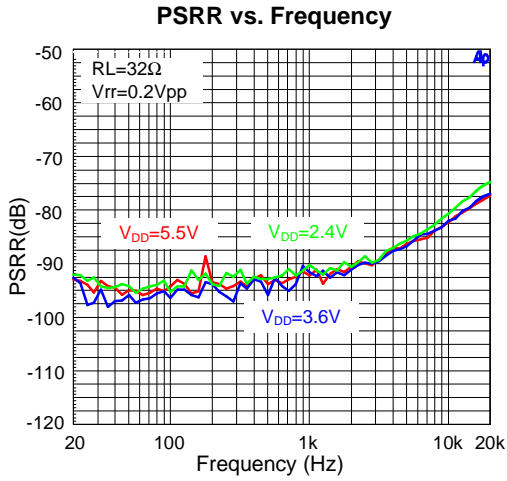
Typical Operating Characteristics



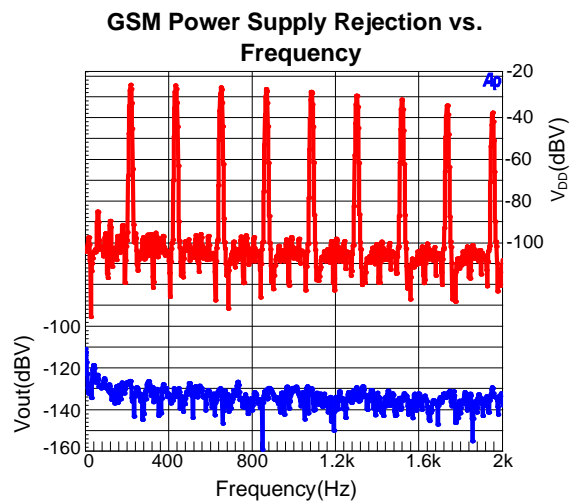
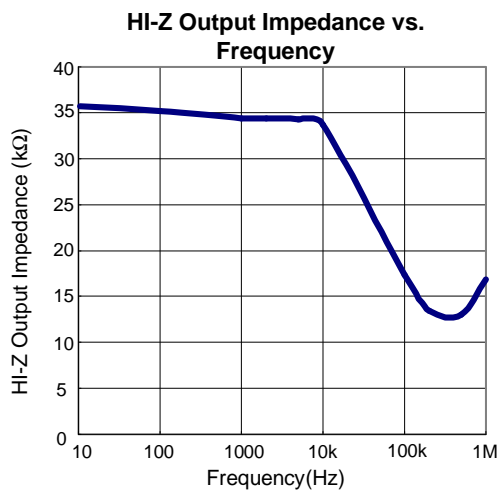
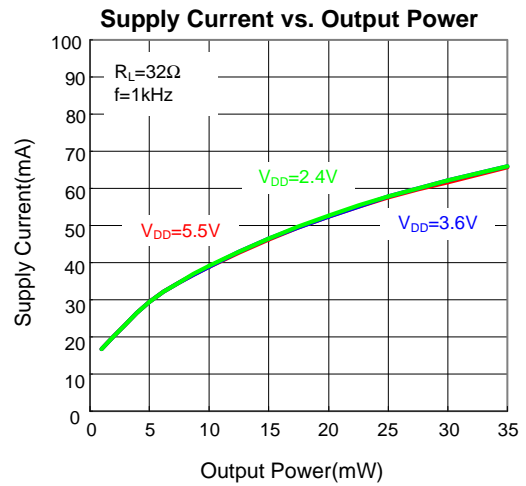
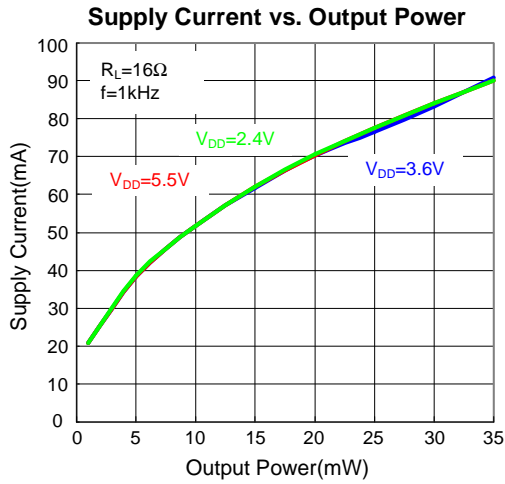
Typical Operating Characteristics



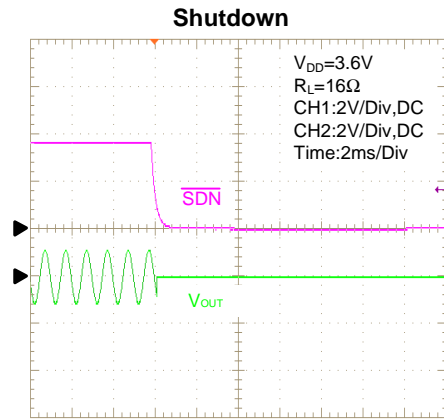
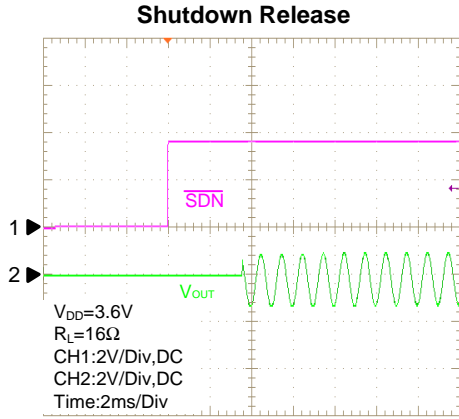
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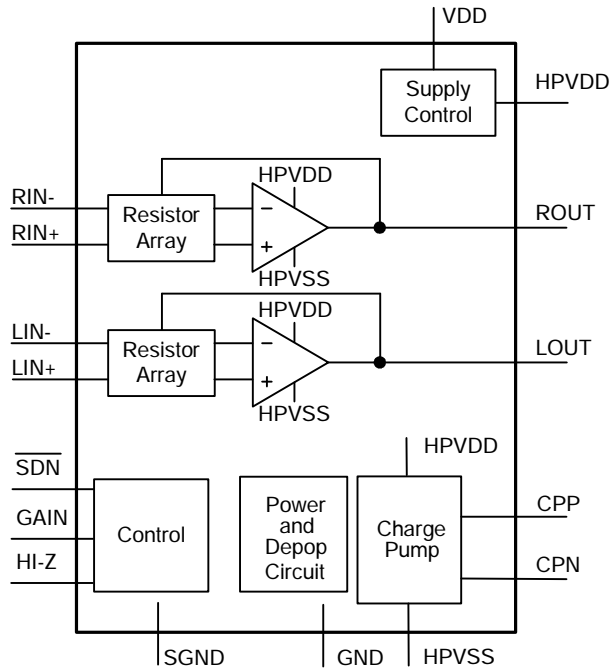
Typical Operating Characteristics



Operating Waveforms

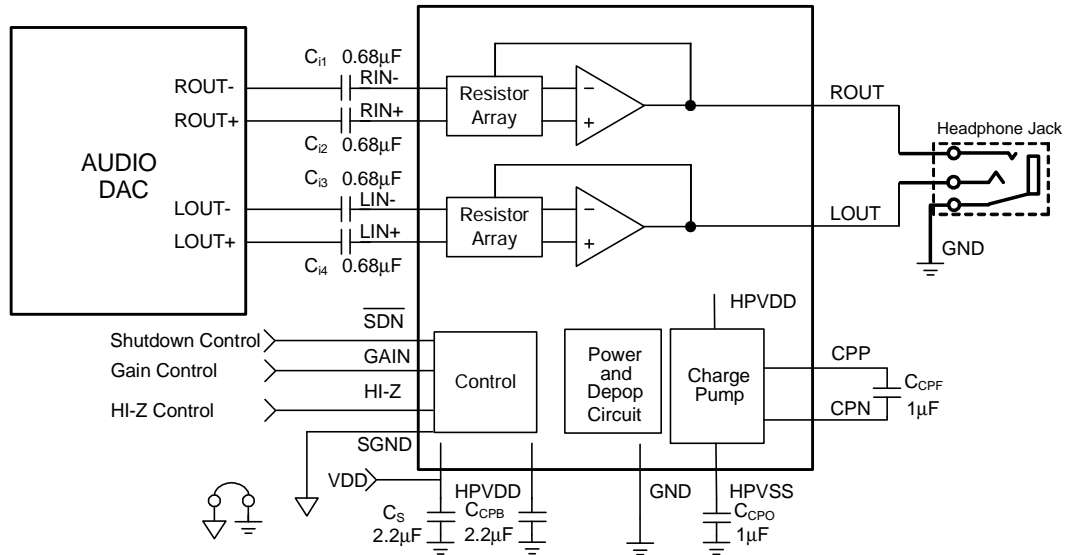


Block Diagram

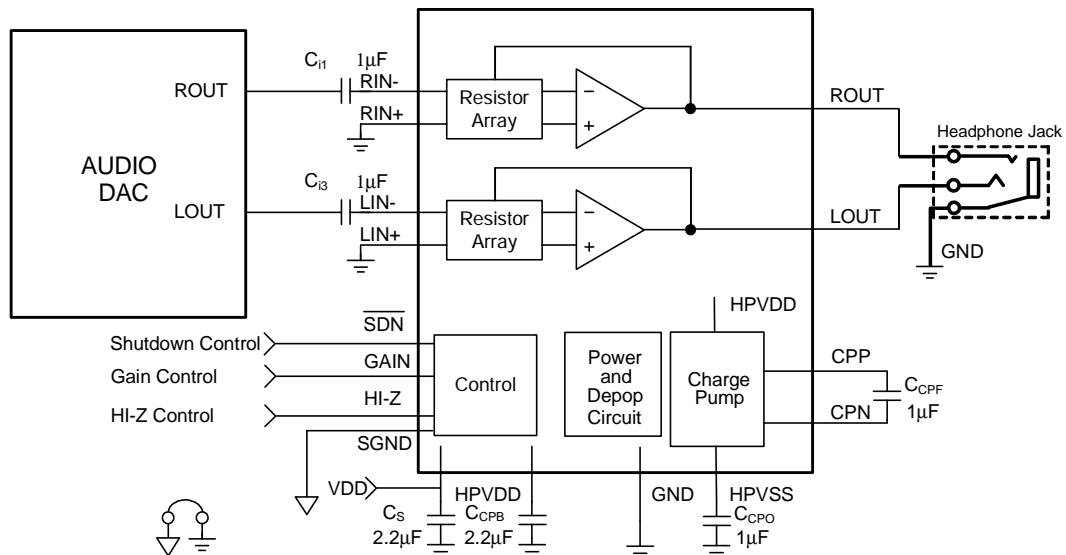


Typical Application Circuit

Differential Input



Single-Ended Input



Function Description

Headphone Driver Operation

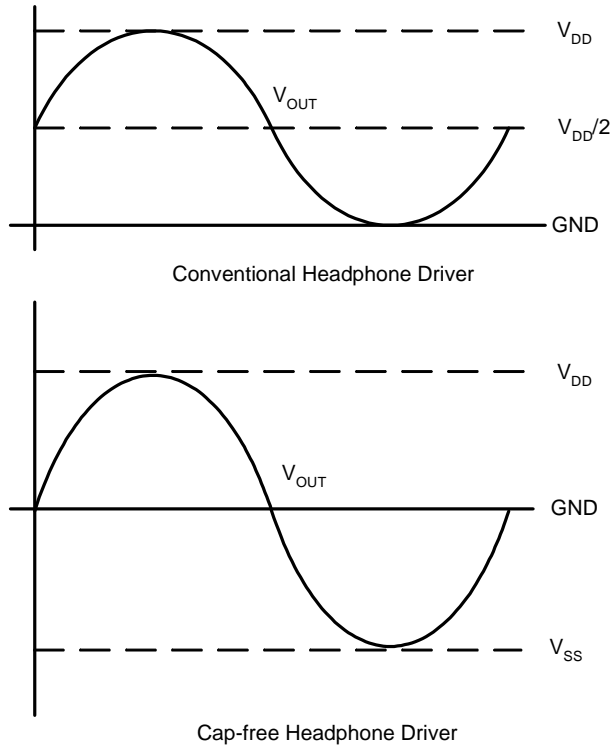


Figure 1. Cap-free Operation

The APA2177's headphone drivers use a charge pump to invert the positive power supply (V_{DD}) to negative power supply (V_{SS}), see figure1. The headphone drivers operate at this bipolar power supply (V_{DD} and V_{SS}) and the outputs reference refers to the ground. This feature eliminates the output capacitor that is using in conventional single-ended headphone drive amplifier. Compare with the single power supply amplifier, the power supply range has almost doubled.

Thermal Protection

The thermal protection circuit limits the junction temperature of the APA2177. When the junction temperature exceeds $T_j = +150^\circ\text{C}$, a thermal sensor turns off the driver, allowing the devices to cool. The thermal sensor allows the driver to start-up after the junction temperature down about 125°C . The thermal protection is designed with a 25°C hysteresis to lower the average T_j during continuous thermal overload conditions, increasing lifetime of the ICs.

Shutdown Function

In order to reduce power consumption while not in use, the APA2177 contains shutdown controllers to externally turns off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{\text{SDN}}$ pins for the APA2177. The trigger point between a logic high is 1.0V and logic low level is 0.35V. It is recommended to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the $\overline{\text{SDN}}$ pins to a low level, the amplifier enters a low-consumption current circumstance, charge pump is disabled, and I_{DD} for the APA2177 is in shutdown mode. In normal operating, the APA2177's $\overline{\text{SDN}}$ pins should be pulled to a high level to keep the IC out of the shutdown mode. The $\overline{\text{SDN}}$ pins should be tied to a definite voltage to avoid unwanted circumstance changes.

Application Information

Input Capacitor, C_i

In the typical application, an input capacitor, C_i , is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i from a high-pass filter with the corner frequency are determined in the following equation:

$$f_{C(\text{highpass})} = \frac{1}{2\pi R_i f_{C_i}} \quad (1)$$

The value of C_i is important to consider as it directly affects the low frequency performance of the circuit. R_i is the internal input resistance that typical value is 13.2K Ω at 6dB and the specification calls for a flat bass response down to 20Hz. Equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_C} \quad (2)$$

Consider to input resistance variation, the C_i is 0.6 μF so one would likely choose a value in the range of 0.6 μF to 1 μF . A further consideration for this capacitor is the leakage path from the input source through the input network ($R_i + R_f, C_i$) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the negative side of the capacitor should face the amplifier input in most applications as the DC level there is held at GND, which is likely lower than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling (C_s)

The APA2177 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitor that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically 0.1 μF , is placed as close as possible to the device VDD lead for the best performance. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 1 μF or greater placed near the audio power amplifier is recommended.

Charge pump flying capacitor, C_{CPF}

The flying capacitor affects the load transient of the charge pump. If the capacitor's value is too small, then that will degrade the charge pump's current driver capability and the performance of headphone drive amplifier.

Increasing the flying capacitor's value will improve the load transient of charge pump. It is recommend using the low ESR ceramic capacitors (X7R type is recommended) above 1 μF .

Charge pump output capacitor, C_{CPO}

The output capacitor's value affects the power ripple directly at HPVSS. Increasing the value of output capacitor reduce the power ripple. The ESR of output capacitor affects the load transient of HPVSS. Lower ESR and greater than 1 μF ceramic capacitor is recommendation.

Application Information

Layout Recommendation

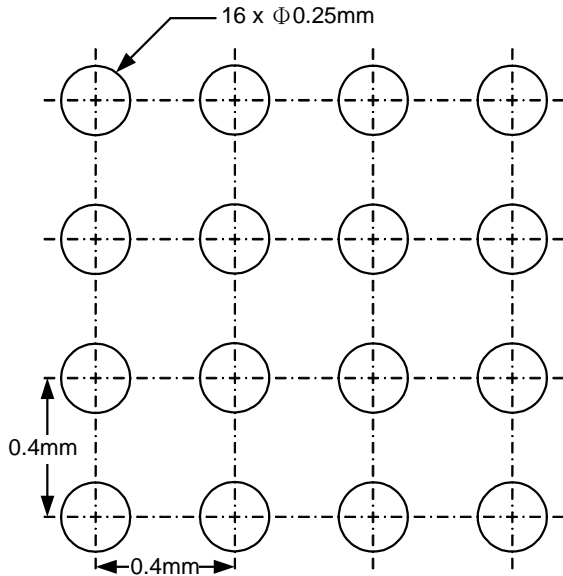


Figure : WLCSP-16 land pattern recommendation

Recommended Minimum Footprint

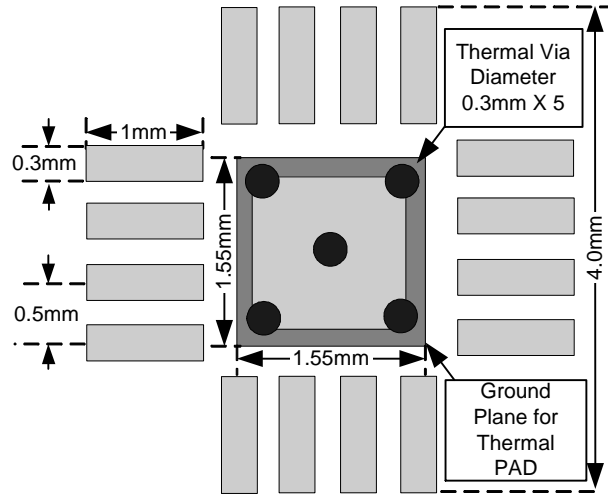
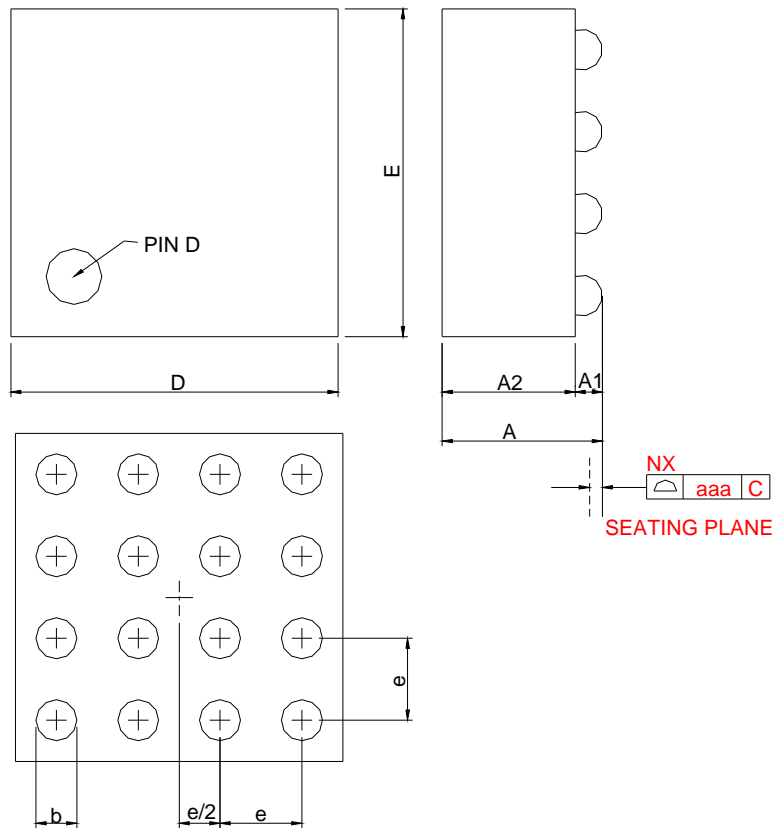


Figure : TQFN3x3-16 Layout Recommendation

1. All components should be placed close to the APA2177. For example, the input capacitor (CiR, CiL) should be close to APA2177 input pins to avoid causing noise coupling to APA2177 high impedance inputs; the decoupling capacitor (CS) should be placed by the APA2177 power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should be greater than 50mil.
5. The input trace and output trace should be away from CCPF and CCPB possible.

Package Information

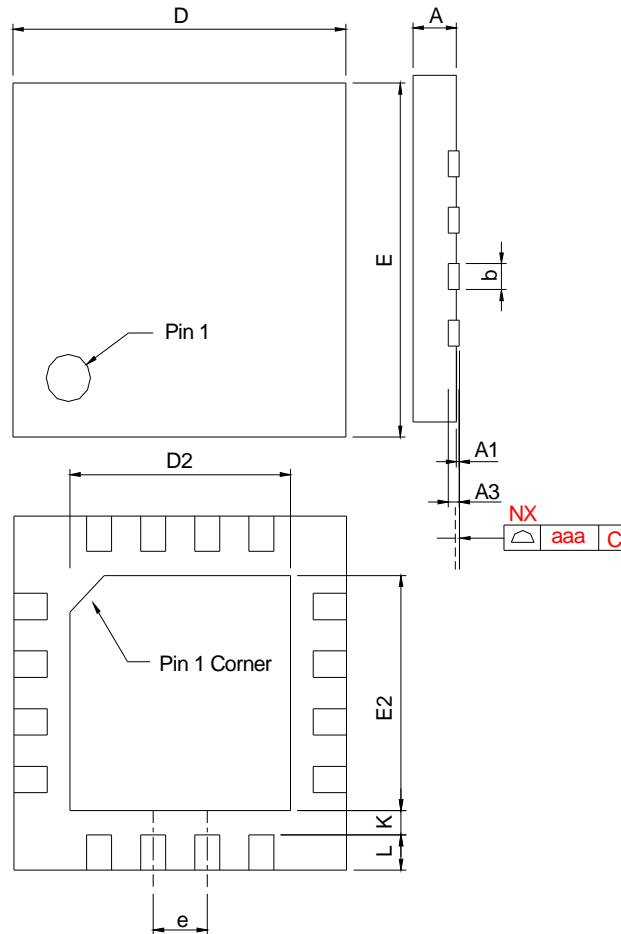
WLCSP1.6x1.6-16



SYMBOL	WLCSP1.6x1.6-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		0.63		0.025
A1	0.12	0.30	0.005	0.012
A2	0.27	0.33	0.011	0.013
b	0.20	0.30	0.008	0.012
D	1.54	1.60	0.061	0.063
E	1.54	1.60	0.061	0.063
e	0.4 BSC		0.016 BSC	
aaa	0.05		0.002	

Package Information

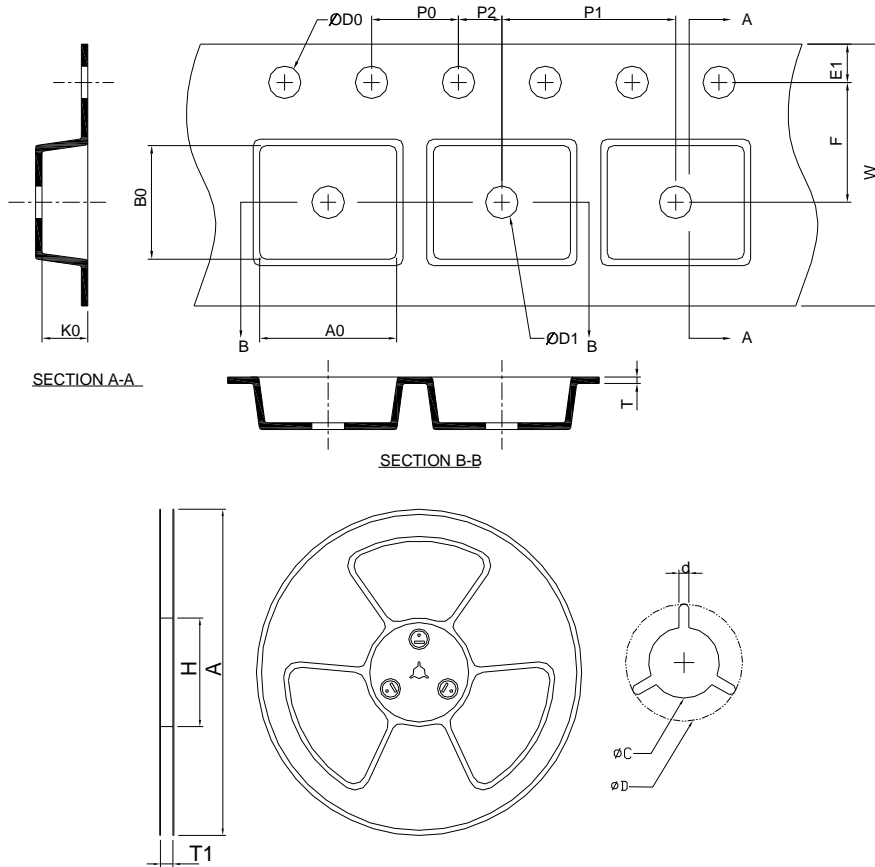
TQFN3x3-16



SYMBOL	TQFN3*3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEED-4.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP1.6x1.6-16	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.75±0.15	1.75±0.15	0.75±0.10
Application	A	H	T1	C	d	D	W	E1	F
TQFN 3x3-16	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20

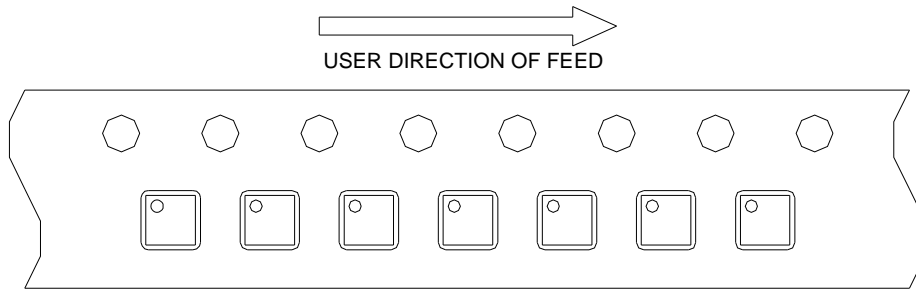
(mm)

Devices Per Unit

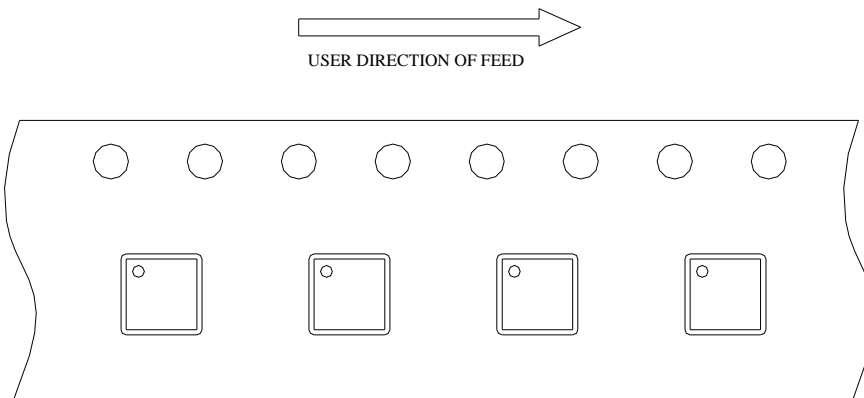
Package Type	Unit	Quantity
WLCSP1.6x1.6-16	Tape & Reel	3000
TQFN3x3	Tape & Reel	2500

Taping Direction Information

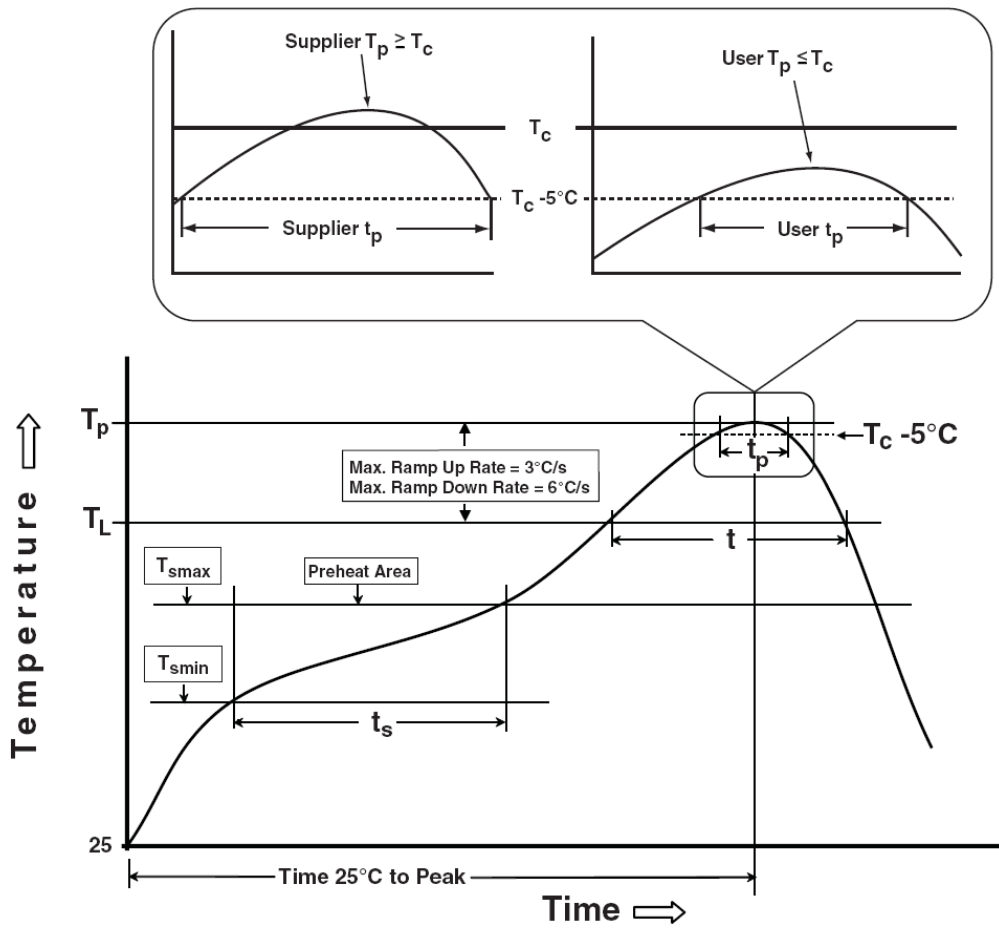
WLCSP1.6x1.6-16



TQFN3x3-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

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