# ACET4445B

**N-Channel Enhancement Mode Field Effect Transistor**

## Description

The ACET4445B uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device is suitable for use as a high side switch in SMPS and general purpose applications.

ACET4445B is electrically identical.

RoHS Compliant

## Features

- $V_{DS}$ (V) = 30V
- $I_D$ = 38A (VGS = 10V)
- $R_{DS(ON)}$ =6.2mΩ ($V_{GS}$ = 10V，Typ)
- $R_{DS(ON)}$ < 8.9mΩ ($V_{GS}$ = 4.5V，Typ)
- Low Qg
- 100% Delta Vsd Tested
- 100% $R_g$ Tested

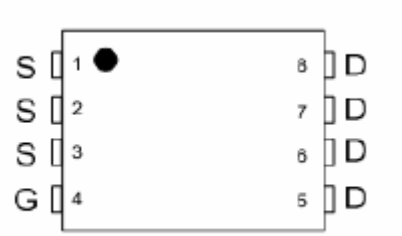
## Absolute Maximum Ratings

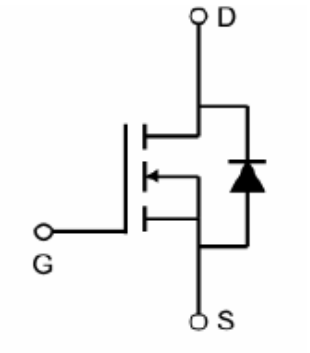
| Parameter | | Symbol | Max | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 30 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±20 | V |
| Drain Current (Continuous) | $T_C$=25°C | $I_D$ | 38 | A |
| | $T_C$=100°C | | 18 | |
| Drain Current (Pulse) [C] | | $I_{DM}$ | 60 | |
| Drain Current (Continuous) | $T_A$=25°C | $I_{DSM}$ | 11 | A |
| | $T_A$=70°C | | 8 | |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 5 | W |
| | $T_C$=100°C | | 3.2 | |
| Power Dissipation [A] | $T_A$=25°C | $P_{DSM}$ | 2 | W |
| | $T_A$=70°C | | 1.3 | |
| Operating and Storage Temperature Range | | $T_J$,$T_{STG}$ | -55 to 150 | °C |

| Thermal Characteristics | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Max** | **Units** |
| Maximum Junction-to-Ambient [A] | t≦10s | $R_{\theta JA}$ | 25 | ℃/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 60 | ℃/W |
| Maximum Junction-to-Case | Steady-State | $R_{\theta JC}$ | 4.2 | ℃/W |

## Packaging Type

DFN5*6-8-EP




## Ordering information

ACET4445B XX + H

- Halogen - free
- Pb - free
- PN : DFN5*6-8-EP

# ACET4445B

## N-Channel Enhancement Mode Field Effect Transistor

**Electrical Characteristics** $T_A$=25 °C unless otherwise noted

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0V, $I_D$=250μA | 30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 30 V , $V_{GS}$ = 0V | | | 1 | μA |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$=$V_{DS}$ ,$I_{DS}$=250μA | 1 | | 3 | V |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V , $V_{DS}$=0V | | | 100 | nA |
| Drain-Source On-state Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10V , $I_D$ = 12A | | 6.2 | 8.5 | mΩ |
| | | $V_{GS}$ =4.5V , $I_D$ = 10A | | 8.9 | 13 | |
| Forward Transconductance | $g_{FS}$ | VDS=10V, ID=12A | 30 | | | S |
| Diode Forward Voltage | $V_{SD}$ | ISD=2A , VGS=0V | | 0.71 | 1.0 | V |
| Maximum Body-Diode Continuous Current | IS | | | | 2 | A |
| Switching | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=15V, $I_D$=12A $V_{GS}$=5V | | 7.5 | | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 1.3 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 4.5 | | |
| Turn-On Delay Time | $T_{d(on)}$ | $V_{DS}$=15V, $V_{GS}$=10V $R_{GEN}$=6Ω, $R_L$=15Ω | | 10 | | ns |
| Turn-On Rise Time | $t_f$ | | | 8 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 30 | | |
| Turn-Off Fall Time | $t_f$ | | | 5 | | |
| Dynamic | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=15V, $V_{GS}$=0V f=1MHz | | 680 | | pF |
| Output Capacitance | $C_{oss}$ | | | 150 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 70 | | |

Note:

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C

## Typical Performance Characteristics

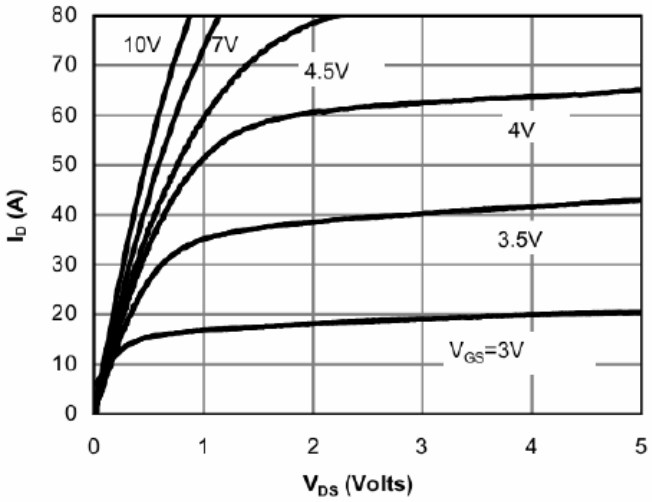



Fig 1: On-Region Characteristics (Note E)

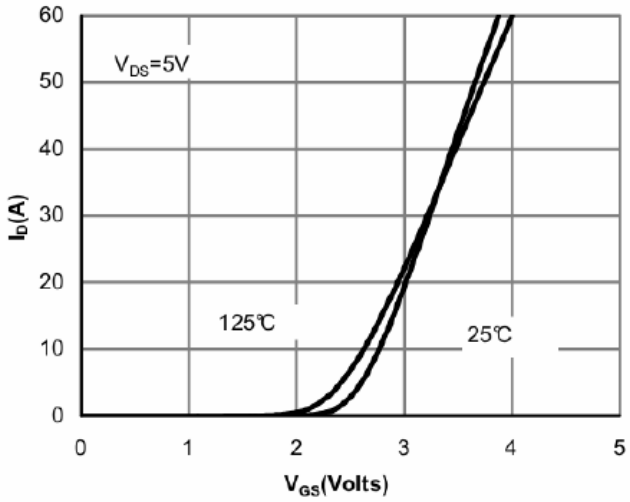



Figure 2: Transfer Characteristics (Note E)

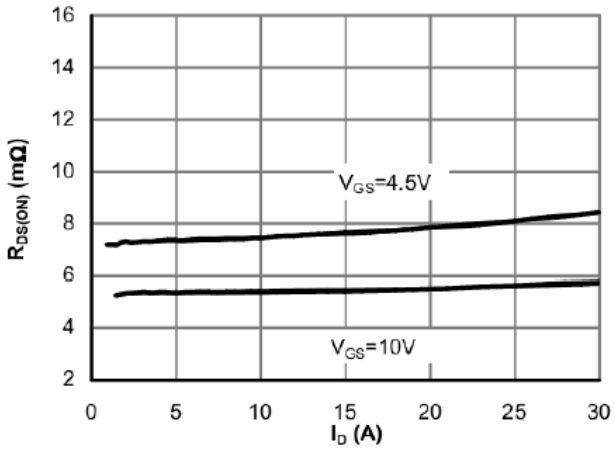



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

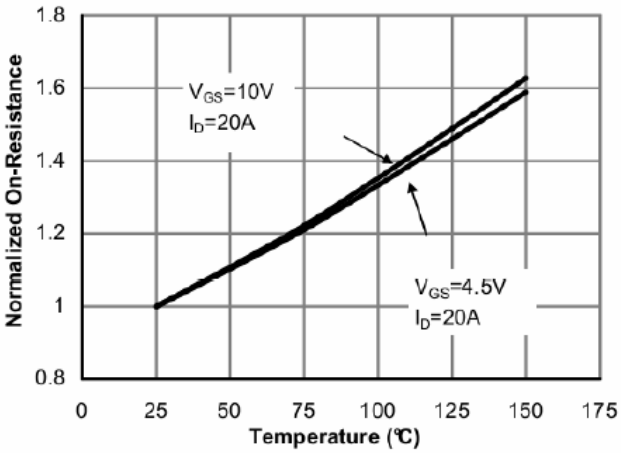



Figure 4: On-Resistance vs. Junction Temperature (Note E)

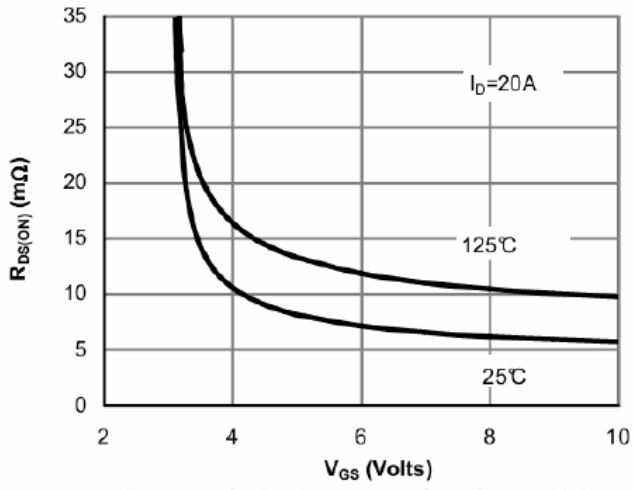



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

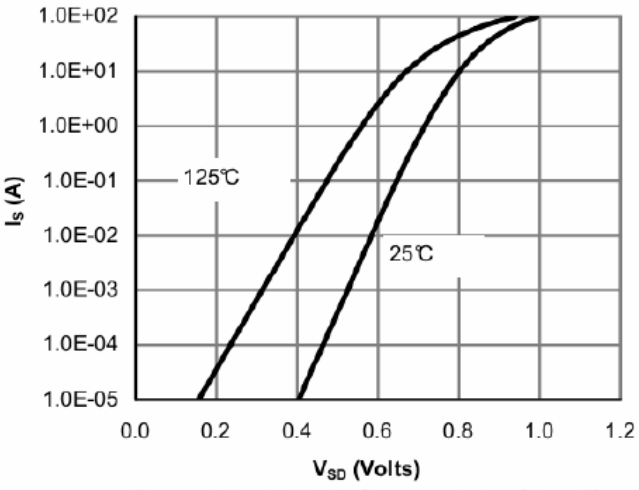



Figure 6: Body-Diode Characteristics (Note E)

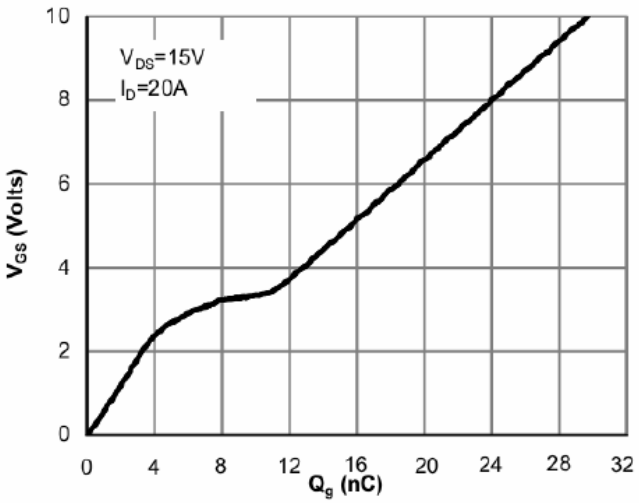



Figure 7: Gate-Charge Characteristics

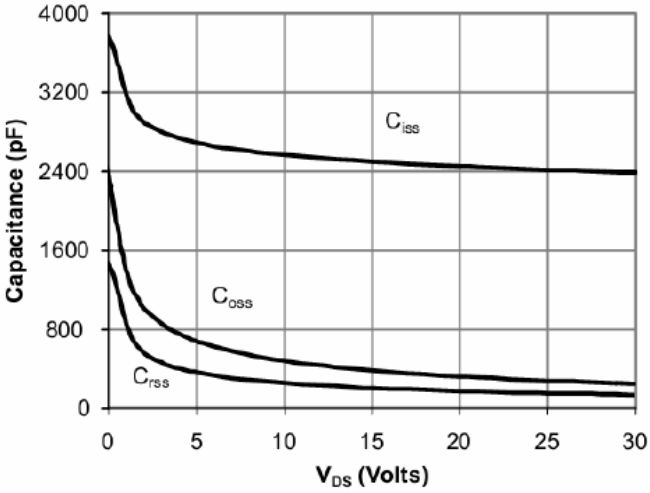



Figure 8: Capacitance Characteristics

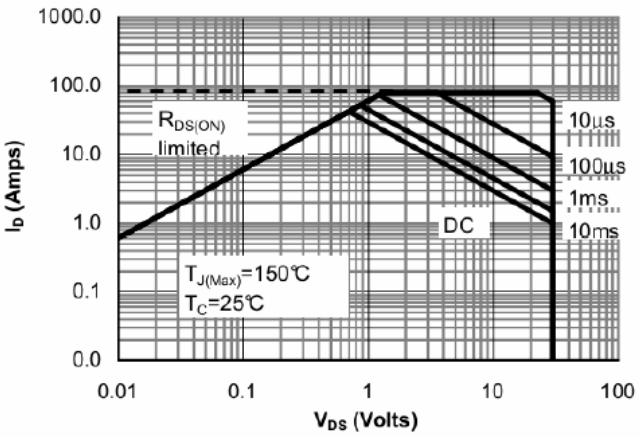



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

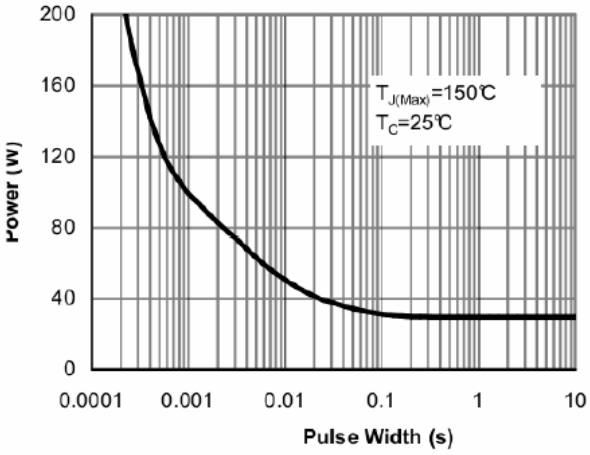



Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

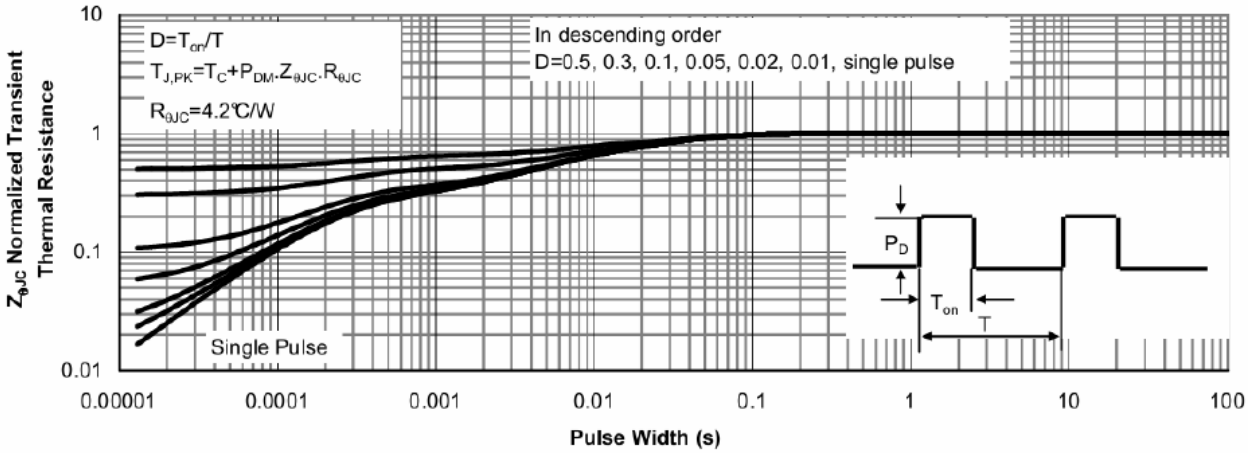



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

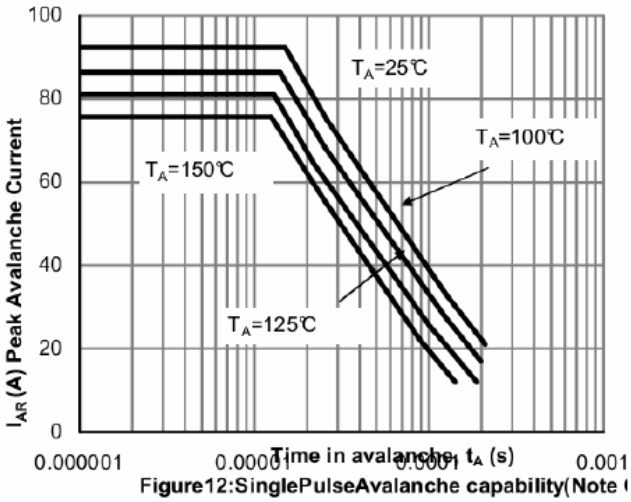


Figure12:SinglePulseAvalanche capability(Note

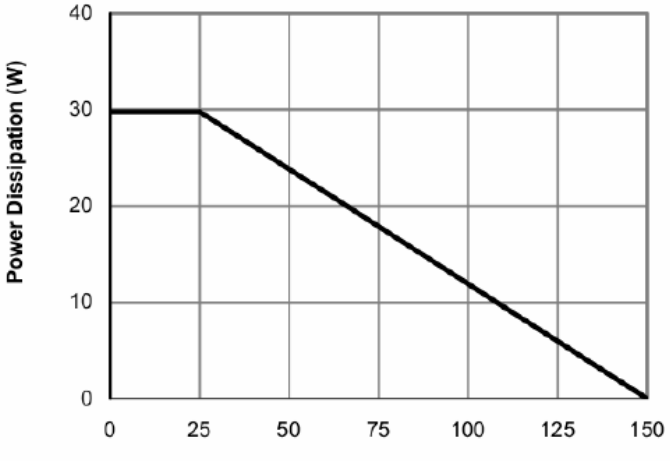


Figure 13: Power De-rating (Note F)

## Typical Performance Characteristics

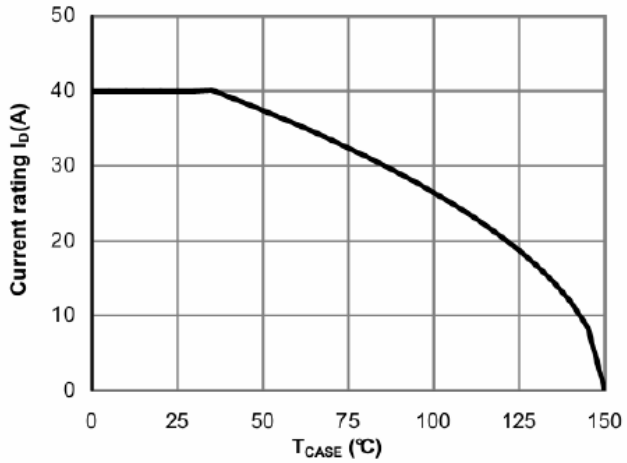


Figure 14: Current De-rating (Note F)

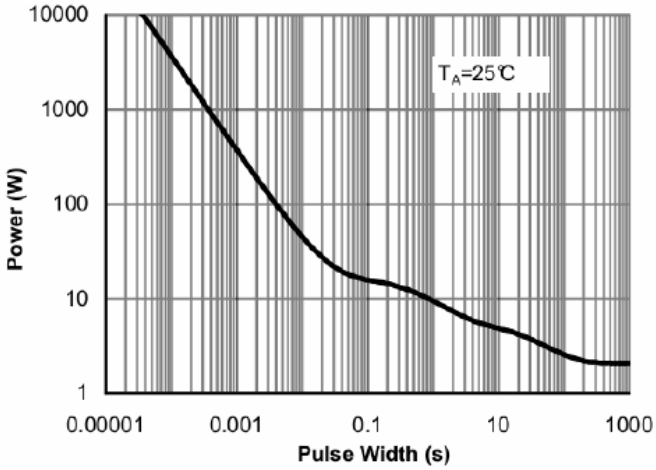


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

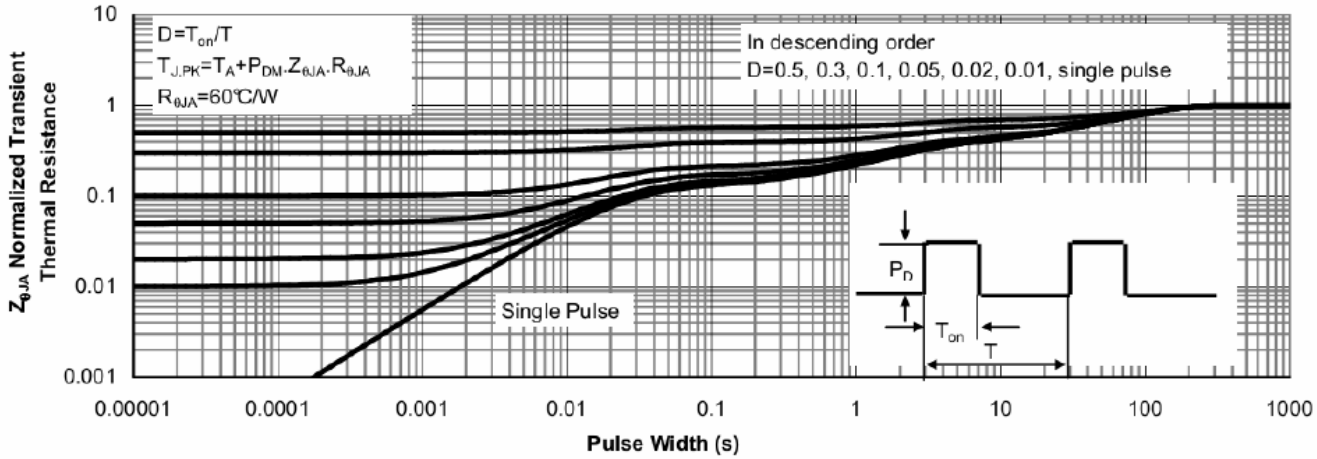
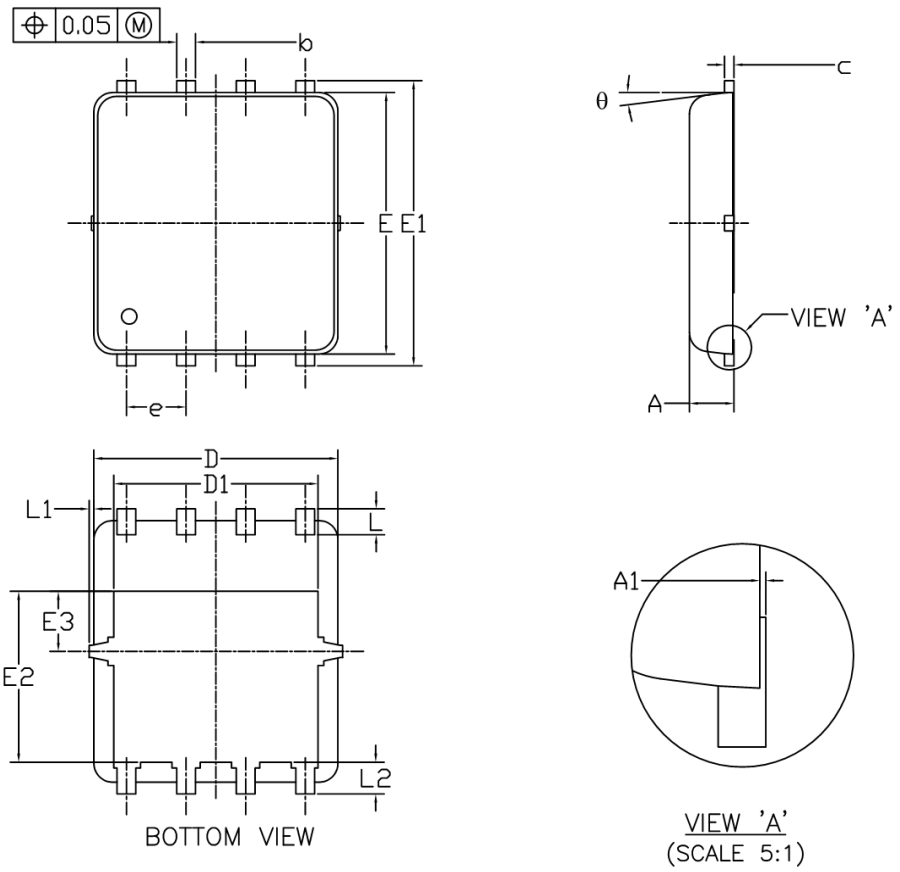


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

## Packing Information

### DFN5*6-8L-EP




| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.85 | 0.95 | 1.00 | 0.033 | 0.037 | 0.039 |
| A1 | 0.00 | —— | 0.05 | 0.000 | —— | 0.002 |
| b | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| c | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 5.20 BSC | | | 0.205 BSC | | |
| D1 | 4.35 BSC | | | 0.171 BSC | | |
| E | 5.55 BSC | | | 0.219 BSC | | |
| E1 | 6.05 BSC | | | 0.238 BSC | | |
| E2 | 3.625 BSC | | | 0.143 BSC | | |
| E3 | 1.275 BSC | | | 0.050 BSC | | |
| e | 1.27 BSC | | | 0.050 BSC | | |
| L | 0.45 | 0.55 | 0.65 | 0.018 | 0.022 | 0.026 |
| L1 | 0 | —— | 0.15 | 0 | —— | 0.006 |
| L2 | 0.68 REF | | | 0.027 REF | | |
| θ | 0° | —— | 10° | 0° | —— | 10° |

Notes

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.