Green-Mode PWM Controller with Frequency Swapping and Integrated Protections

Rev. 02a

General Description

The LD7536 is built-in with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the Frequency Swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

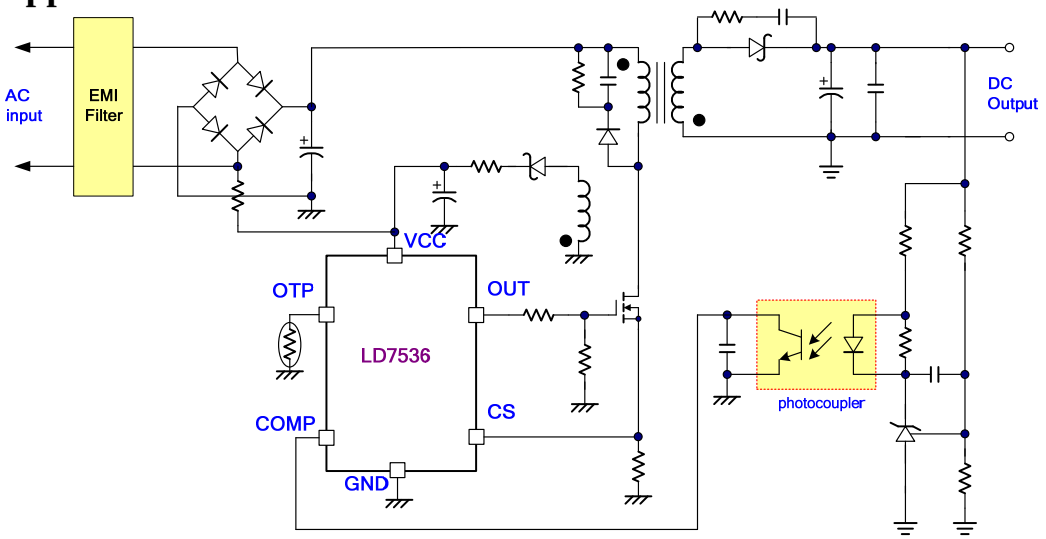
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<20μA)
- Current Mode Control
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- OTP (Over Temperature Protection) through a NTC
- OLP (Over Load Protection)
- 300mA Driving Capability

Applications

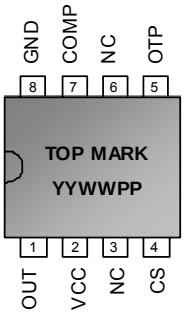
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application

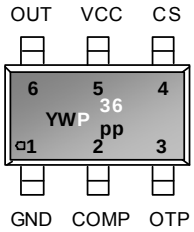


Pin Configuration

DIP-8 (TOP VIEW)



SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
P36 : LD7536

Ordering Information

Part number	Package		Top Mark	Shipping
LD7536 GL	SOT-26	Green Package	YWP/36	3000 /tape & reel
LD7536 GN	DIP-8	Green Package	LD7536 GN	3600 /tube /Carton

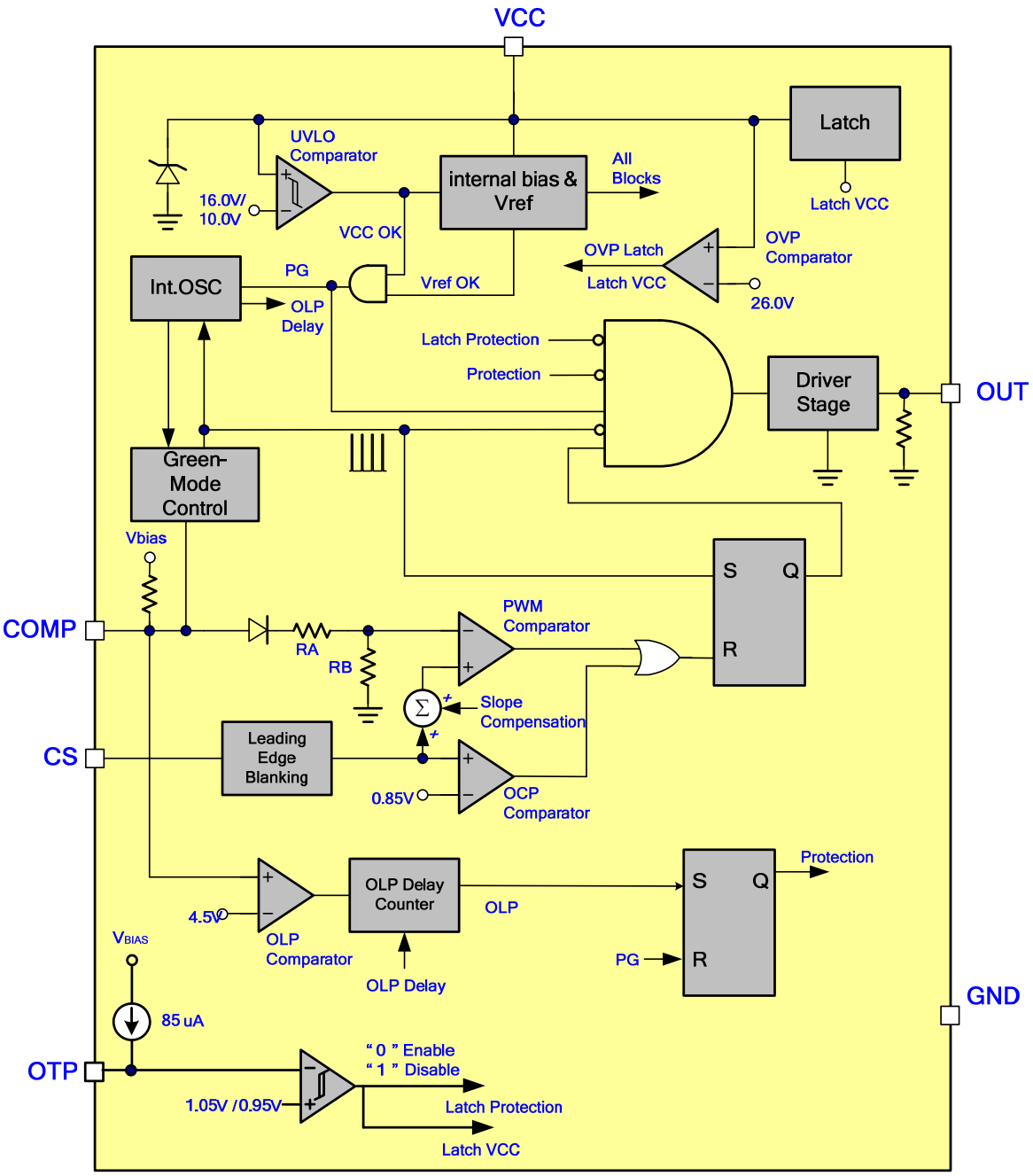
Protection Mode

Switching Freq.	VCC OVP	OLP	OTP Pin
65kHz	Latch	Auto recovery/ 65ms	Latch

Pin Descriptions

PIN SOT-26	PIN DIP-8	NAME	FUNCTION
1	8	GND	Ground
2	7	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation.
3	5	OTP	Pull this pin below 0.95V to shutdown the controller into latch mode until the AC resume power-on. Connecting this pin to ground with NTC will achieve OTP protection. Keep this pin float to disable the latch protection.
4	4	CS	Current sense pin, connect it to sense the MOSFET current
5	2	VCC	Supply voltage pin
6	1	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~29V
COMP, RT, CS	-0.3V ~6V
OUT	-0.3V ~Vcc+0.3V
Maximum Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Operating Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	250°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	300mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	11	24	V
Start-up resistor Value	540K	1.8 M	Ω

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current			12	20	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		1.0		mA
	V_{COMP}=3V		2.0		mA
	OLP Tripped/ Auto		0.4		mA
	OVP Tripped/Latch		0.85		mA
	OTP Pin Tripped/Latch		0.85		mA
Holding Current	Vcc=7V (latched)		430		μA
UVLO (off)		9	10	11	V
UVLO (on)		15	16	17	V
OVP Level		25	26	27	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		0.25		mA
Open Loop Voltage	COMP pin open		5.4		V
Green Mode Threshold VCOMP			2.2		V
Zero Duty Threshold VCOMP			1.4		V
Zero Duty Hysteresis			100		mV
Current Sensing (CS Pin)					
Maximum Input Voltage, V_{CS_OFF}		0.8	0.85	0.9	V
Leading Edge Blanking Time			230		ns
Internal Slope Compensation	0% to D_{MAX}. (Linearly increase)		300		mV
Input impedance		1			MΩ
Delay to Output			100		ns
Oscillator for Switching Frequency					
Frequency, FREQ		60	65	70	kHz
Green Mode Frequency, FREQG			22		kHz
Trembling Frequency			± 4.0		kHz
Temp. Stability	(-20°C ~85°C)		5		%
Voltage Stability	(VCC=11V-25V)			1	%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	8			V
Rising Time	Load Capacitance=1000pF	--	170	350	ns
Falling Time	Load Capacitance=1000pF		50	100	ns
Max. Duty			75		%
OLP (Over Load Protection)					
OLP Trip Level		4.3	4.5	4.7	V
OLP Delay Time		55	65	75	ms
OTP Pin Latch Protection (OTP Pin)					
OTP Pin Source Current		77	85	92	μA
Turn-On Trip Level		1.00	1.05	1.10	V
Turn-Off Trip Level		0.9	0.95	1.0	V
OTP pin de-bounce time			250		μs
On Chip OTP (Over Temperature)					
OTP Level			140		°C
OTP Hysteresis			30		°C
Soft Start Duration					
Soft Start Duration			2		ms

Typical Performance Characteristics

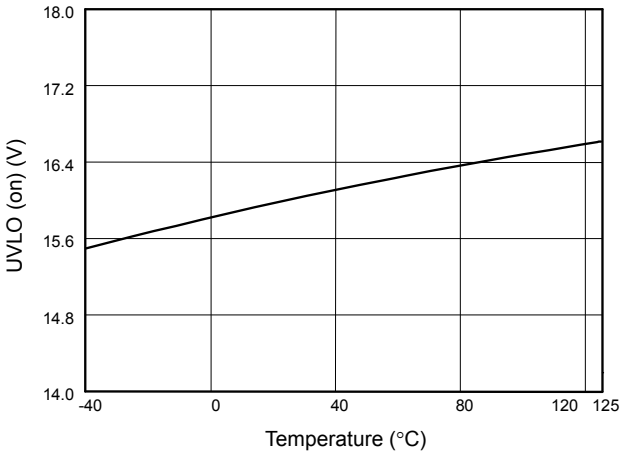


Fig. 1 UVLO (on) vs. Temperature

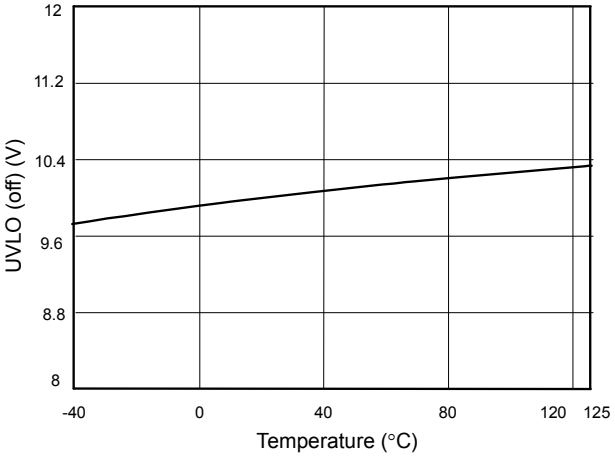


Fig. 2 UVLO (off) vs. Temperature

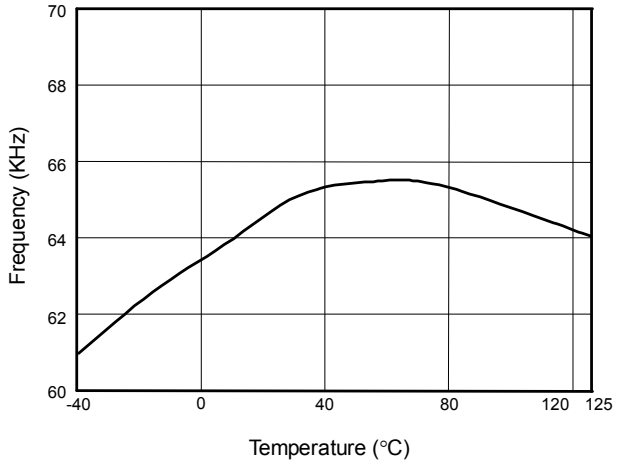


Fig. 3 Frequency vs. Temperature

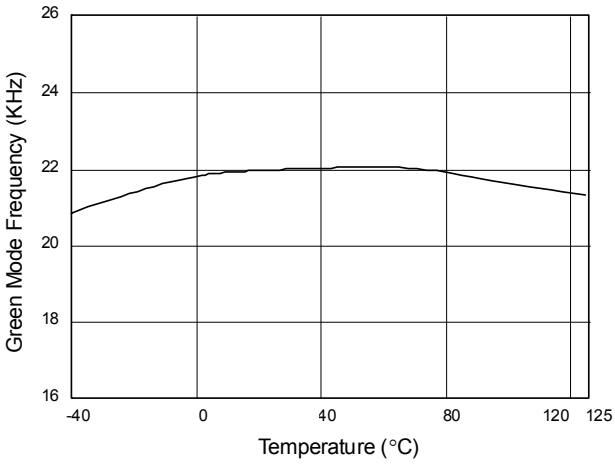


Fig. 4 Green Mode Frequency vs. Temperature

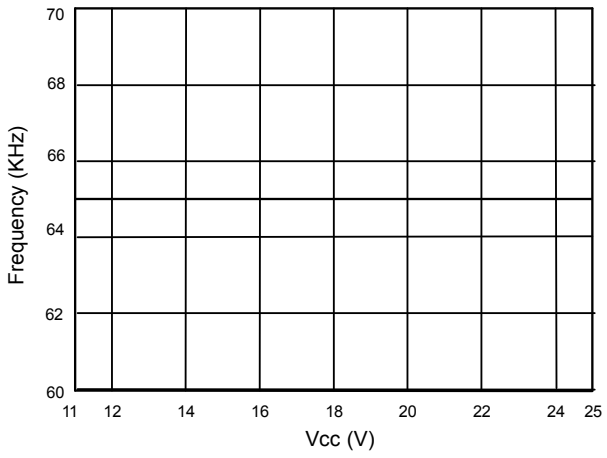


Fig. 5 Frequency vs. Vcc

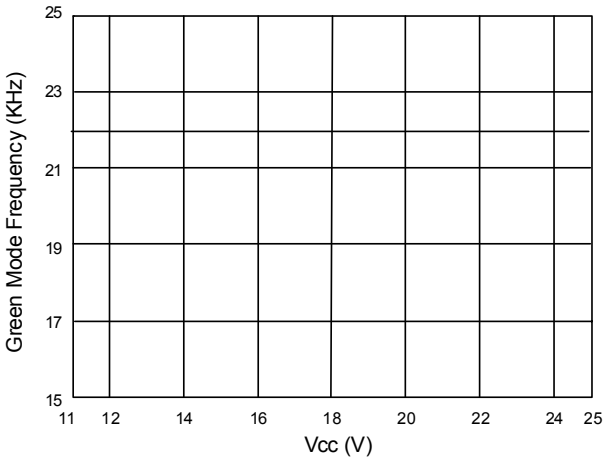


Fig. 6 Green Mode Frequency vs. Vcc

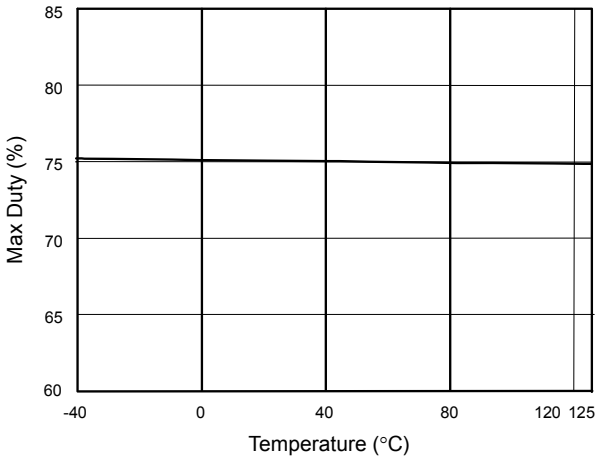


Fig. 7 Max Duty vs. Temperature

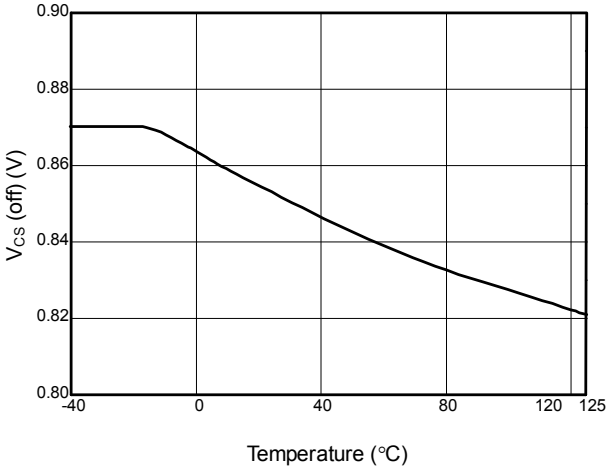


Fig. 8 V_{CS} (off) vs. Temperature

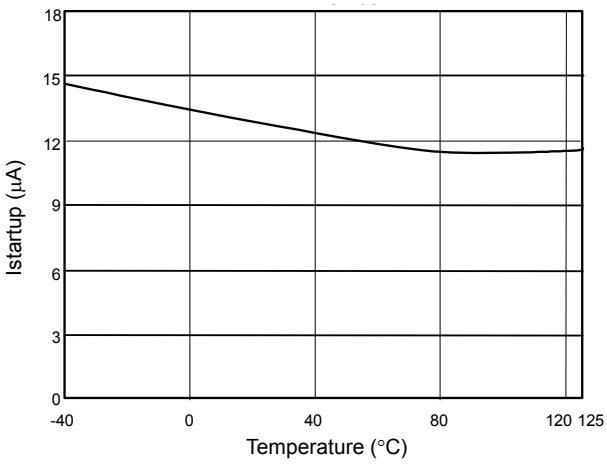


Fig. 9 Startup Current (Istartup) vs. Temperature

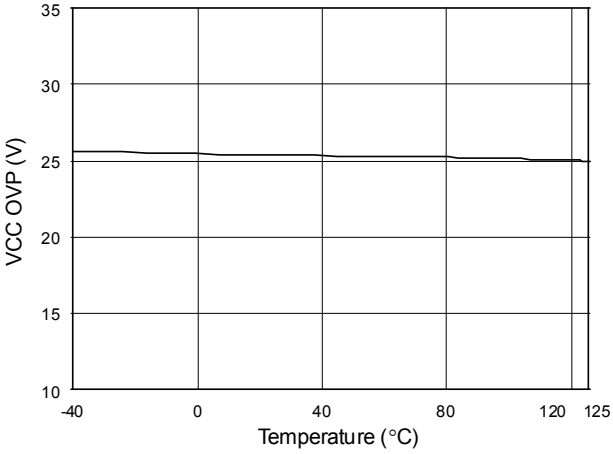


Fig. 10 VCC OVP vs. Temperature

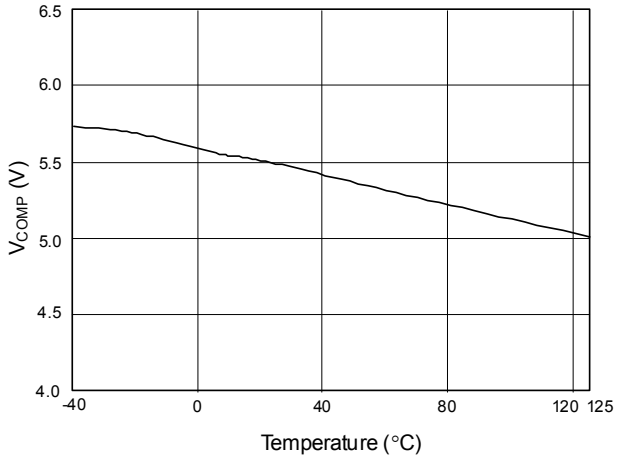


Fig. 11 V_{COMP} open loop voltage vs. Temperature

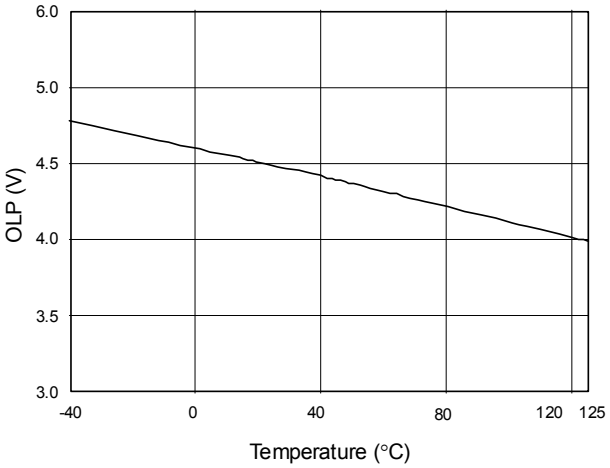


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

The LD7536 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7536 PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.0V and 10.0V, respectively.

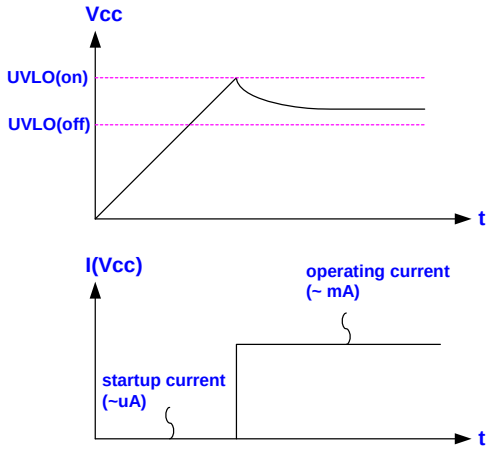


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate V_{CC} of the LD7536 is shown in Fig. 14. During the startup transient, the V_{CC} is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once V_{CC} obtain enough voltage to turn on the LD7536 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD7536 is only 20μA.

If a higher resistance value of the R1 is chosen, it will usually take more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

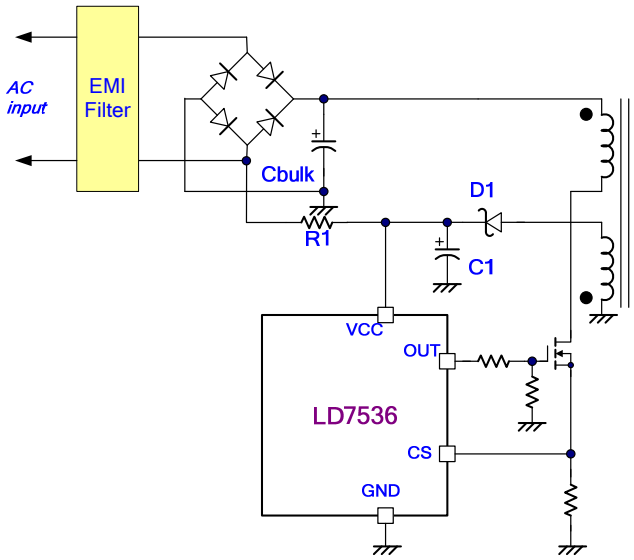


Fig. 14

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 15, the LD7536 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

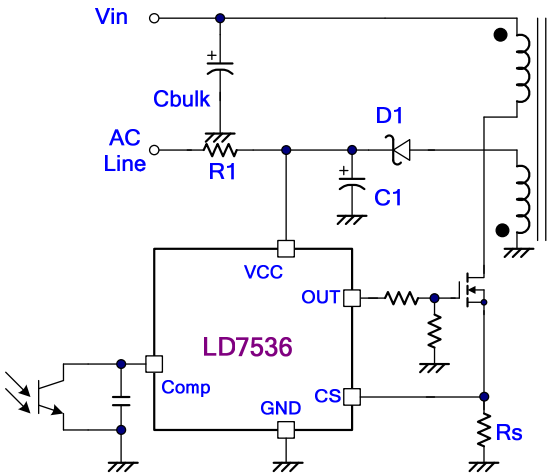


Fig. 15

A 230nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 230nS and the negative spike on the CS pin below -0.3V, the R-C filter is free to eliminate. (As shown in Fig.16).

However, the total pulse width of the turn-on spike is determined according to output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in Fig. 17) for larger power application to avoid the CS pin being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 300mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7536 is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD7536. Similar to UC3842, the LD7536 would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{RB}{RA + RB} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

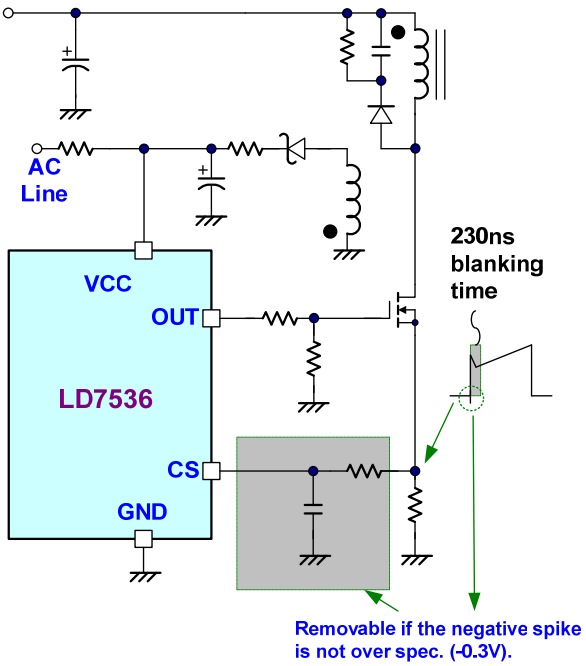


Fig. 16

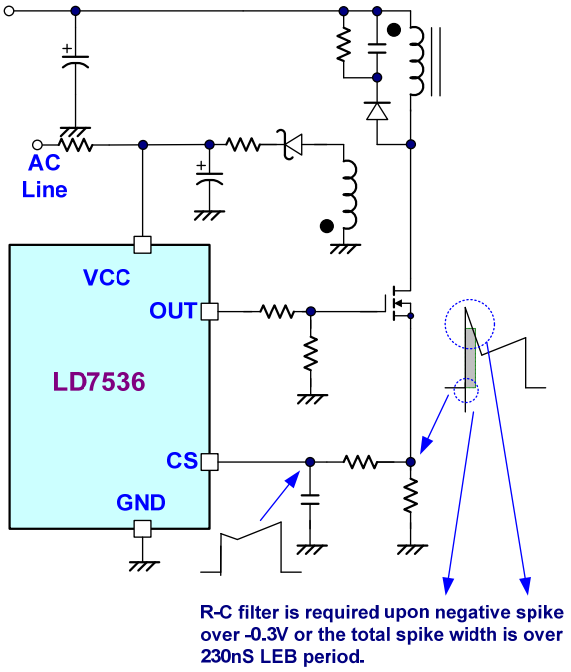


Fig. 17

Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD7536 since it has integrated it already.

On/Off Control

The LD7536 can be turned off by pulling COMP pin lower than 1.4V. The gate output pin of the LD7536 will be disabled immediately under such condition. The off-mode can be released when the pull-low signal is removed.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD7536 is implemented with smart OLP function. It also features auto recovery function, see Fig. 18 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 4.5V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

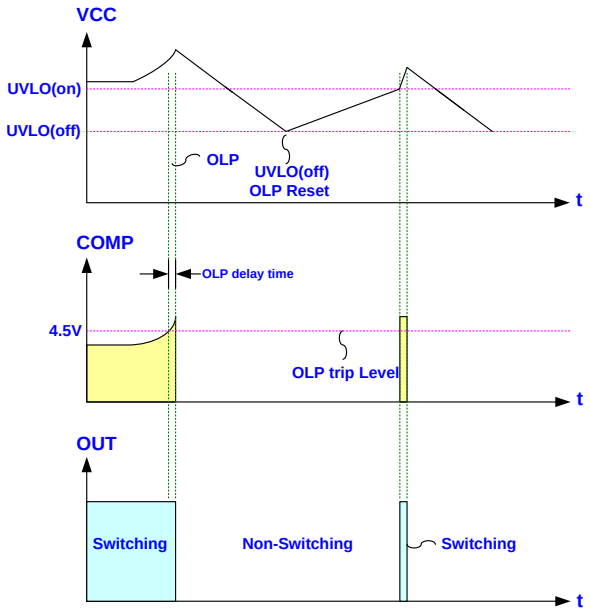


Fig. 18

OVP (Over Voltage Protection) on Vcc - Latch mode

The Vcc OVP function of LD7536 is in latch mode. As soon as the voltage of the Vcc pin rises above OVP threshold, the output gate drive circuit will be shutdown simultaneous to latch off the power MOSFET. On the contrast, if the voltage on Vcc pin drops below OVP threshold and starts AC-recycling again, it will soon resume to normal operation. Fig. 19 shows its operation.

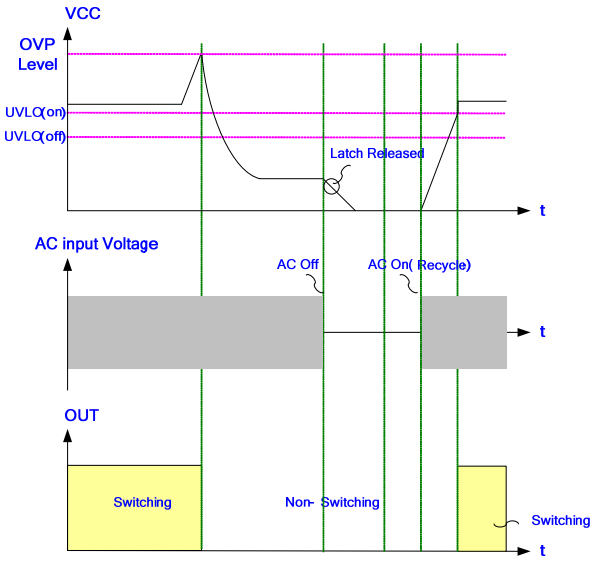


Fig. 19

OTP Pin --- Latched Mode Protection

To protect the power circuit from damage due to system failure, over temperature protection (OTP) is required. The OTP circuit is implemented to sense a hot-spot of power circuit like power MOSFET or output rectifier. It can be easily achieved by connecting a NTC with OTP pin of LD7536. As the device temperature or ambient temperature rises, the resistance of NTC decreases. So, the voltage on the OTP pin could be written as below.

$$V_{OTP} = 85\mu A \cdot R_{NTC}$$

When the V_{OTP} is below the defined voltage threshold (typ. 0.95V), LD7536 will shutdown the gate output and latch off the power supply. There are 2 conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise V_{OTP} up above 1.05V. Then, remove the AC power cord and restart AC power-on recycling.

Oscillator and Switching Frequency

The LD536 is implemented with Frequency Swapping function which helps the power supply designers to both optimize EMI performance and lower system cost. The switching frequency substantially centers at 65KHz, and swap between a range of ±4KHz.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

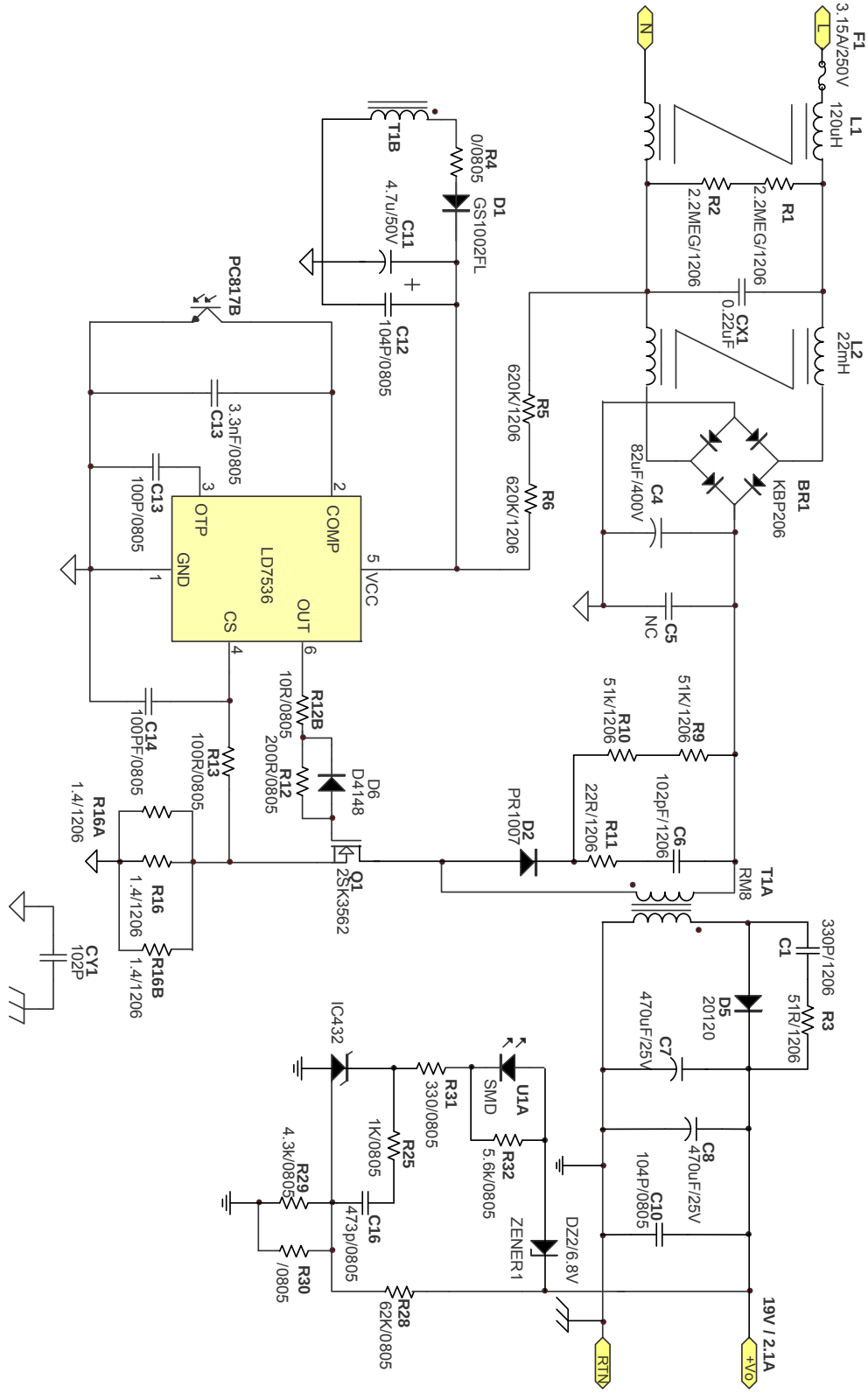
Fault Protection

There are several critical protections integrated in the LD7536 to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD7536.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

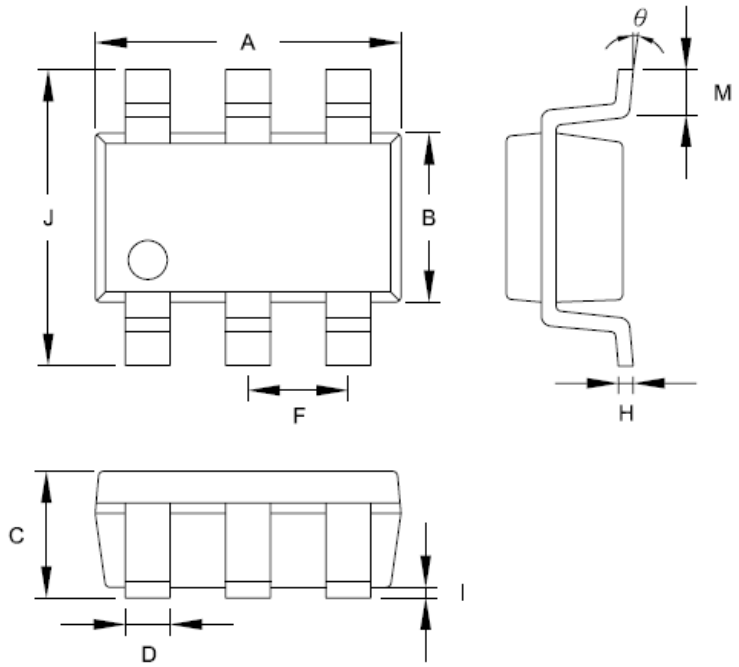
1. CS pin floating
2. COMP pin floating

Reference Application Circuit --- 40W (19V/2.1A) Adapter



Package Information

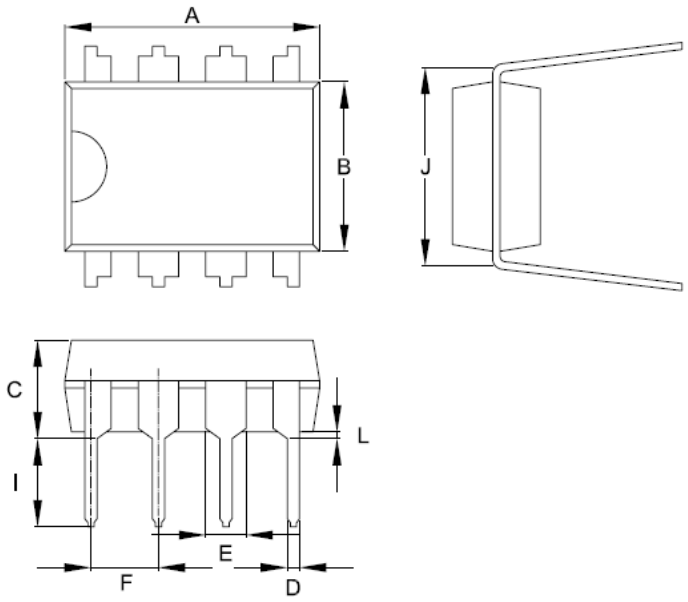
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	2/25/2010	Original Specification
00a	3/15/2010	Start-up resistor value (max): 1.8M OTP source current (min.) 77μA
02	7/1/2010	OLP trip level (min.) (max.)
02a	12/15/2011	OLP Delay Time (min.) (max.) Operating Ambient Temperature (min.)