PRELIMINARY

PD-97200B

International Rectifier

2N7628M1

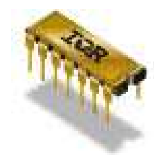
RADIATION HARDENED LOGIC LEVEL POWER MOSFET THRU-HOLE (MO-036AB)

IRHLG7970Z4 60V, Quad P-CHANNEL

R7™ TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHLG7970Z4	100K Rads (Si)	1.25Ω	-0.71A
IRHLG7930Z4	300K Rads (Si)	1.25Ω	-0.71A



MO-036AB

International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Light Weight
- Complimentary N-Channel Available - IRHLG770Z4

Absolute Maximum Ratings (Per Die) — Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = -4.5V, T_C=25°C	Continuous Drain Current	-0.71	A
I_D @ V_{GS} = -4.5V, T_C=100°C	Continuous Drain Current	-0.45	
I_{DM}	Pulsed Drain Current ①	-2.84	
P_D @ T_C = 25°C	Max. Power Dissipation	1.0	W
	Linear Derating Factor	0.01	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	21	mJ
I_{AR}	Avalanche Current ①	-0.71	A
E_{AR}	Repetitive Avalanche Energy ①	0.1	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-14	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)	
	Weight	1.3 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics For Each P-Channel Device @Tj = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.08	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.25	Ω	V_{GS} = -4.5V, I_D = -0.45A ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	V_{DS} = V_{GS}, I_D = -250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	3.07	—	mV/°C	
g_{fs}	Forward Transconductance	0.9	—	—	S	V_{DS} = -10V, I_{DS} = -0.45A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V_{DS}= -48V ,V_{GS}= 0V
		—	—	-10		V_{DS} = -48V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 10V
Q_g	Total Gate Charge	—	—	2.8	nC	V_{GS} = -4.5V, I_D = -0.71A
Q_{gs}	Gate-to-Source Charge	—	—	1.7		V_{DS} = -30V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	0.8		
$t_{d(on)}$	Turn-On Delay Time	—	—	17	ns	V_{DD} = -30V, I_D = -0.71A,
t_r	Rise Time	—	—	20		V_{GS} = -5.0V, R_G = 24Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	27		
t_f	Fall Time	—	—	23		
$L_S + L_D$	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.)with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	138	—	pF	V_{GS} = 0V, V_{DS} = -25V
C_{oss}	Output Capacitance	—	39	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	6.7	—		
R_g	Gate Resistance	—	52.4	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.71	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-2.84		
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_j = 25°C, I_S = -0.71A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	30	ns	T_j = 25°C, I_F = -0.71A, di/dt ≤ -100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	11	nC	V_{DD} ≤ -25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJA}	Junction-to-Ambient	—	—	125	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available International Rectifier Website.

For footnotes refer to the last page

PRELIMINARY

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each P-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 300K Rads (Si)[1]		Units	Test Conditions
		Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V_{GS} = 0V, I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0		V_{GS} = V_{DS}, I_D = -250μA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V_{GS} = -10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	100		V_{GS} = 10V
I_{DSS}	Zero Gate Voltage Drain Current	—	-1.0	μA	V_{DS}= -48V, V_{GS}= 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	1.20	Ω	V_{GS} = -4.5V, I_D = -0.45A
$R_{DS(on)}$	Static Drain-to-Source On-state ④ Resistance (MO-036)	—	1.25	Ω	V_{GS} = -4.5V, I_D = -0.45A
V_{SD}	Diode Forward Voltage ④	—	-5.0	V	V_{GS} = 0V, I_D = -0.71A

1. Part numbers IRHLG7970Z4, IRHLG7930Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area (Per Die)

Ion	LET (MeV/(mg/cm^2))	Energy (MeV)	Range (μm)	VDS (V) @VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V	@VGS= 8V	@VGS= 10V
Br	37	305	39	-60	-60	-60	-60	-60	-50	-35	-25
I	60	370	34	-60	-60	-60	-60	-60	-20	-	-
Au	84	390	30	-60	-60	-60	-60	-	-	-	-

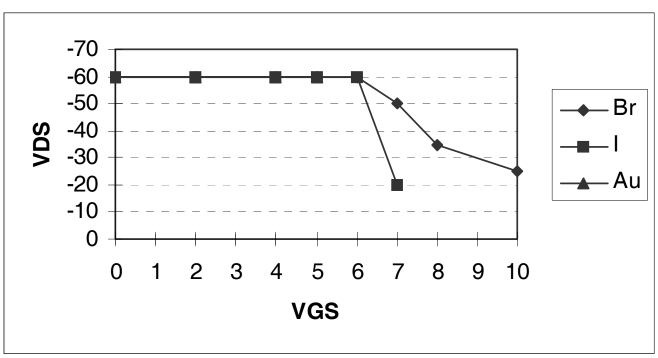


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

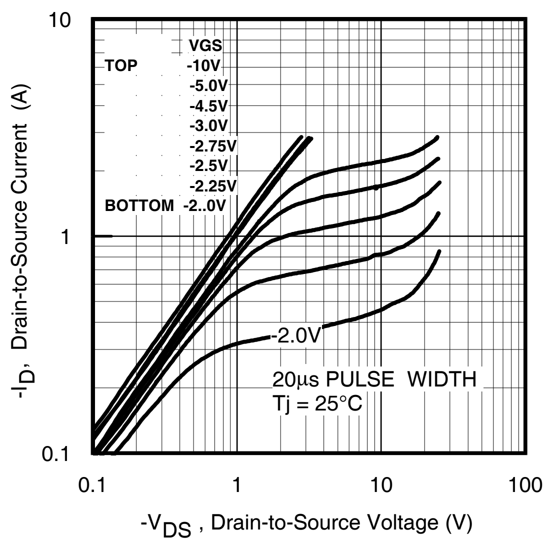


Fig 1. Typical Output Characteristics

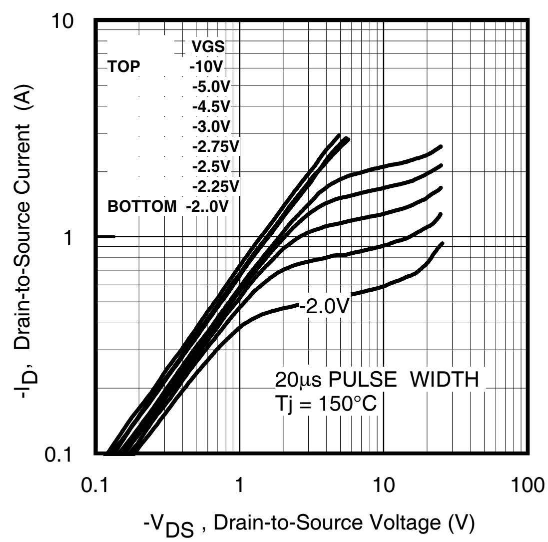


Fig 2. Typical Output Characteristics

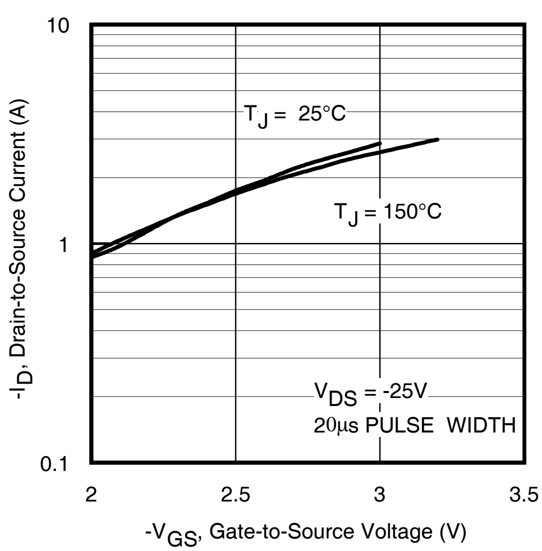


Fig 3. Typical Transfer Characteristics

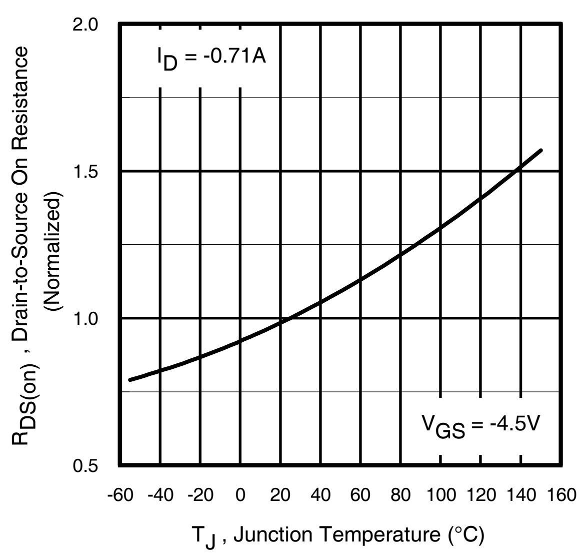


Fig 4. Normalized On-Resistance
Vs. Temperature

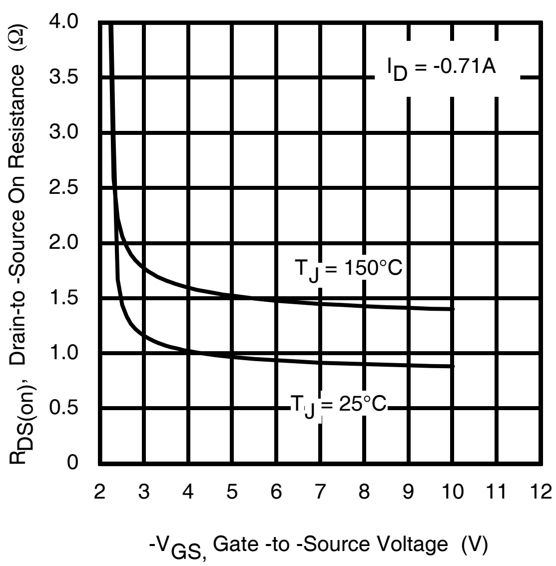


Fig 5. Typical On-Resistance Vs Gate Voltage

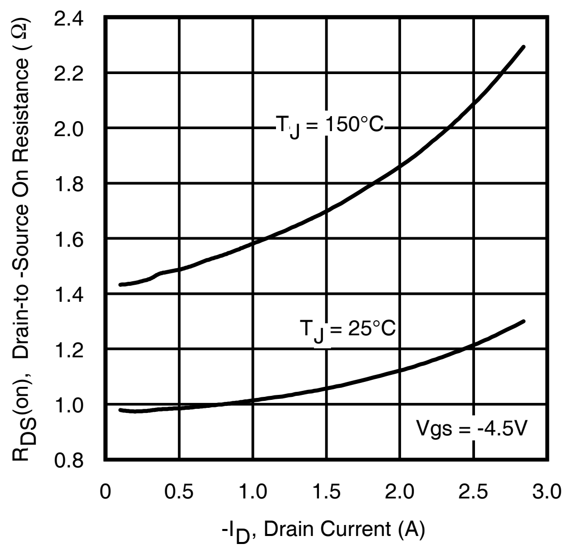


Fig 6. Typical On-Resistance Vs Drain Current

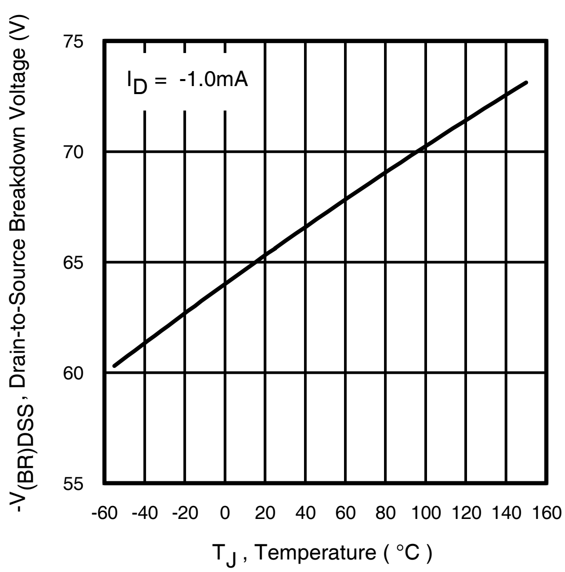


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

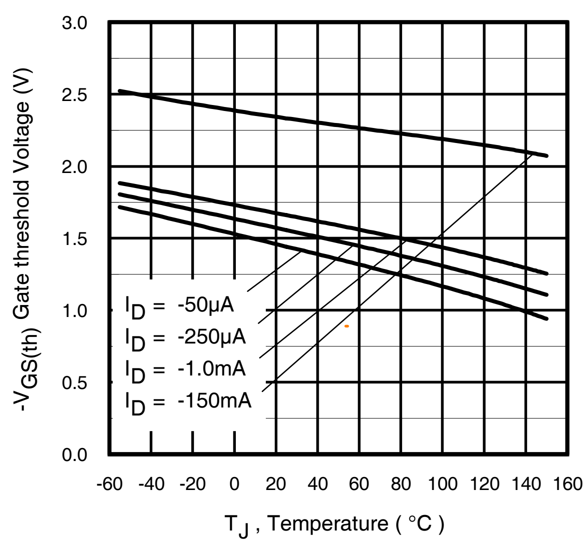


Fig 8. Typical Threshold Voltage Vs Temperature

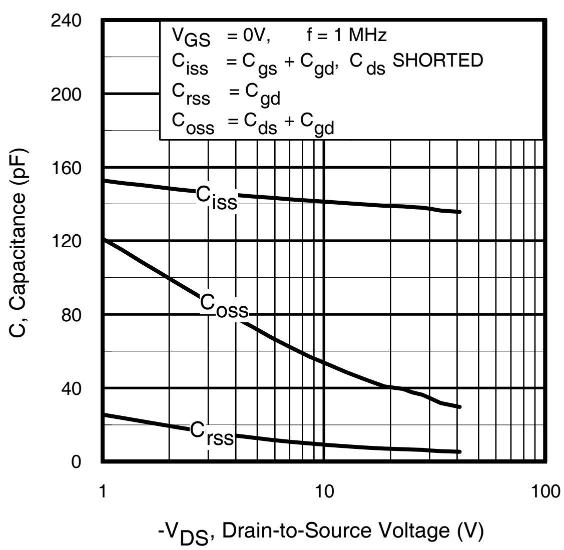


Fig 9. Typical Capacitance Vs.Drain-to-Source Voltage

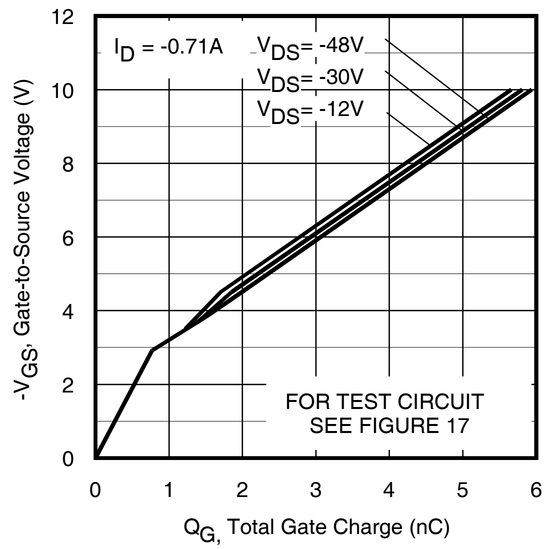


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

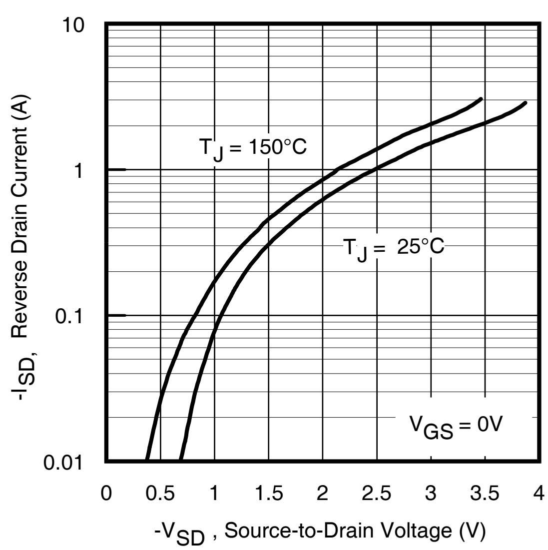


Fig 11. Typical Source-Drain Diode Forward Voltage

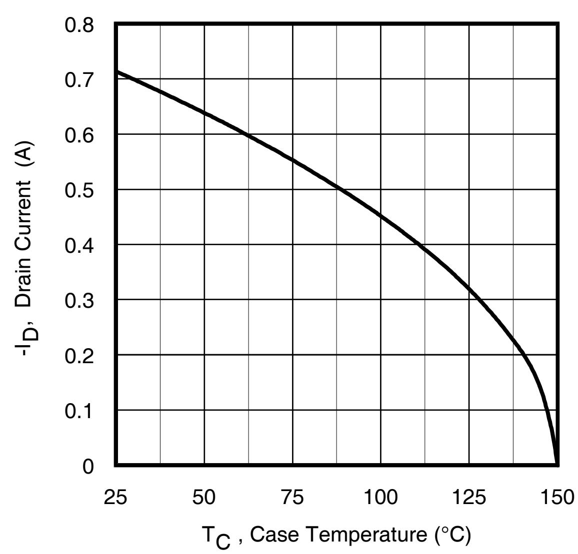


Fig 12. Maximum Drain Current Vs. Case Temperature

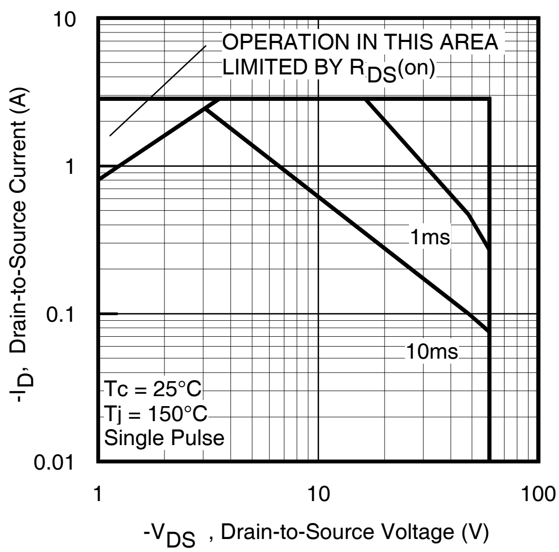


Fig 13. Maximum Safe Operating Area

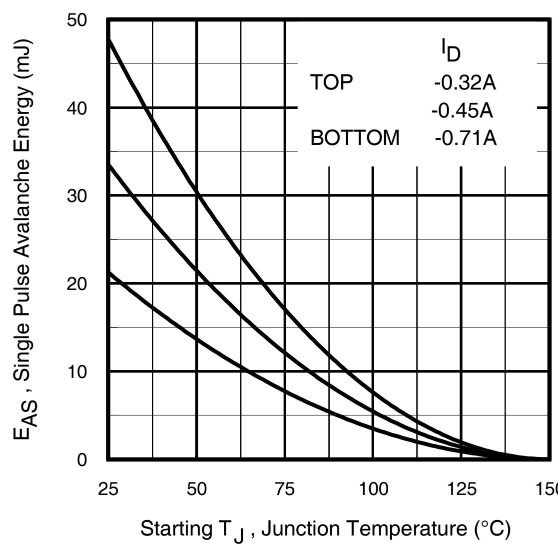


Fig 14. Maximum Avalanche Energy Vs. Drain Current

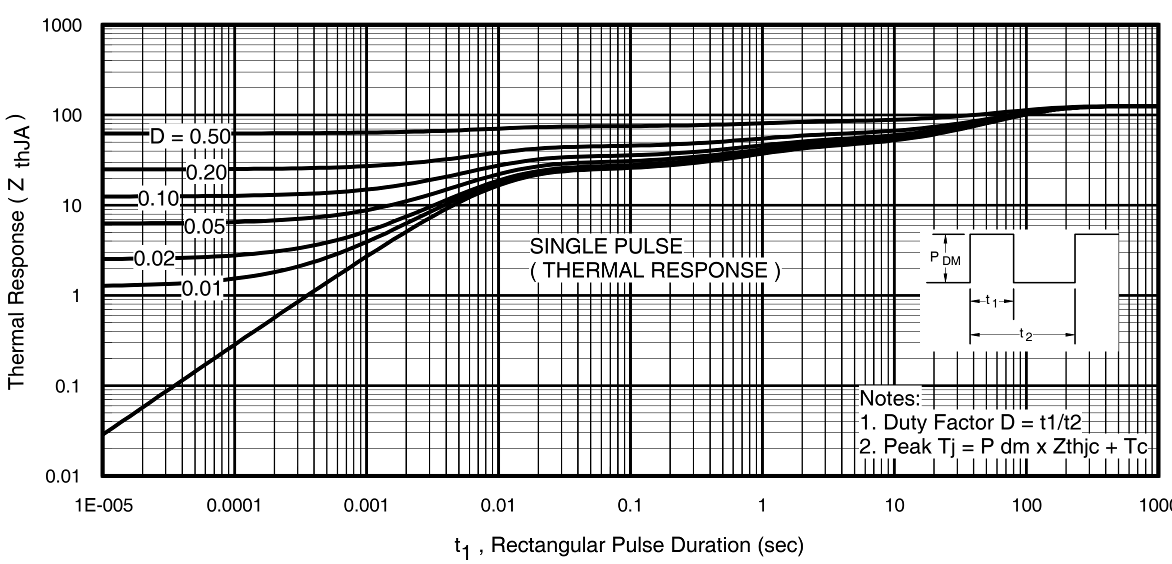


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

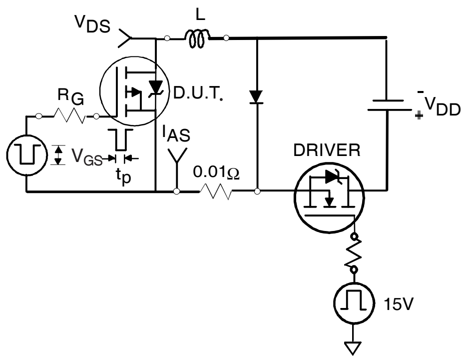


Fig 16a. Unclamped Inductive Test Circuit

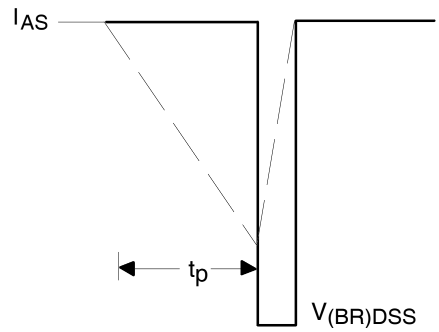


Fig 16b. Unclamped Inductive Waveforms

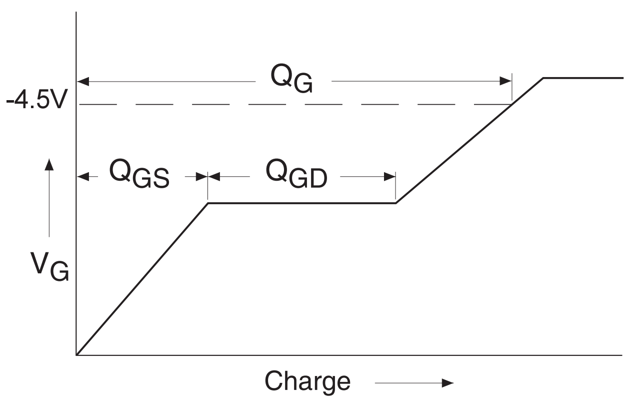


Fig 17a. Basic Gate Charge Waveform

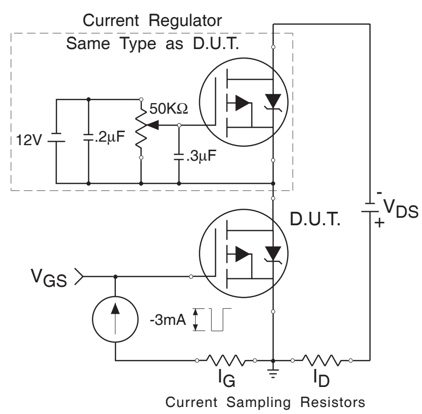


Fig 17b. Gate Charge Test Circuit

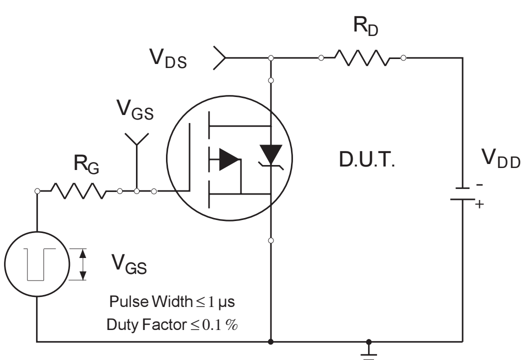


Fig 18a. Switching Time Test Circuit

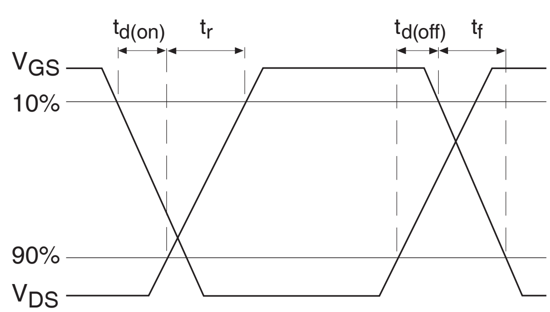


Fig 18b. Switching Time Waveforms

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -25V, starting T_J = 25°C, L= 85mH Peak I_L = -0.71A, V_{GS} = -10V

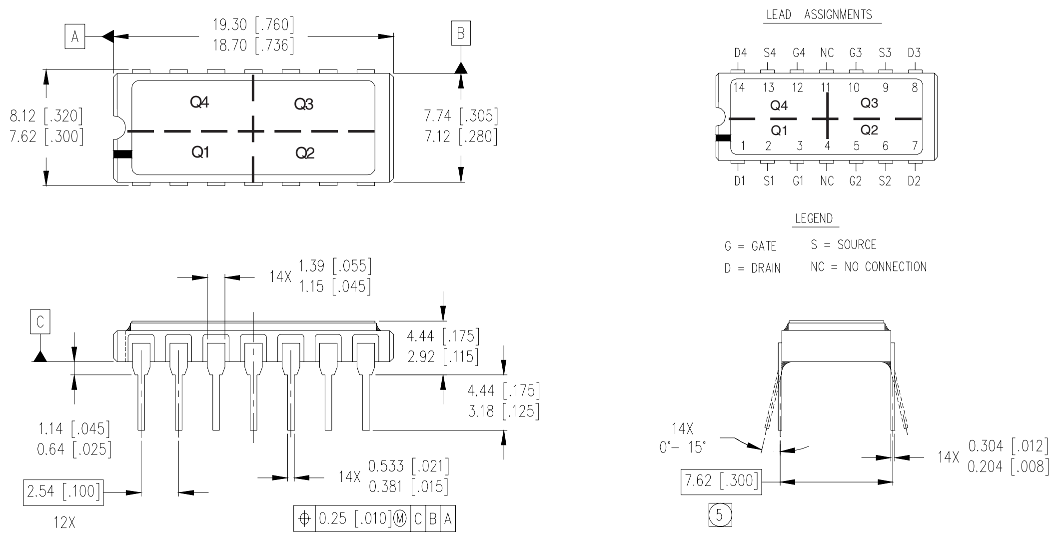
③ $I_{SD} \leq$ -0.71A, di/dt $\leq$ -164A/µs, $V_{DD} \leq$ -60V, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300 µs; Duty Cycle $\leq$ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** -10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** -48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — MO-036AB



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO–036AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International IOR Rectifier

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Data and specifications subject to change without notice. 03/2011