High Speed CMOS Logic – 54HC02

Quad 2-Input NOR Gates in bare die form

Rev 1.0
22/04/19

Description

The 54HC02 2-Input NOR Gate is fabricated on a .35µm advanced CMOS process combining high speed LSTTL performance with CMOS low power. The device performs the Boolean function $Y = (\overline{A + B})$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic. Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. The product die size is significantly smaller than industry peers due to its re-design and production using a more advanced CMOS process.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- Function compatible with 54LS02
- High Noise Immunity CMOS process
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

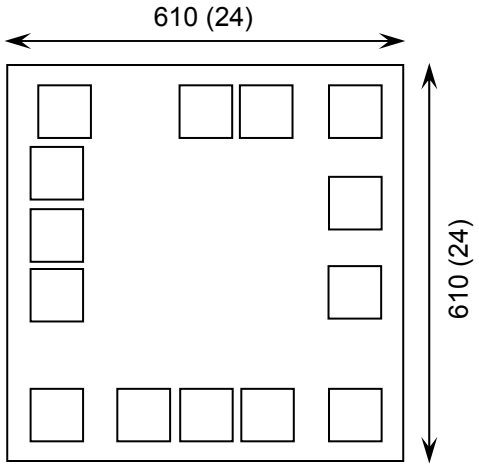
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	610 x 610 24 x 24	µm mils
Minimum Bond Pad Size	85 x 85 3.35 x 3.35	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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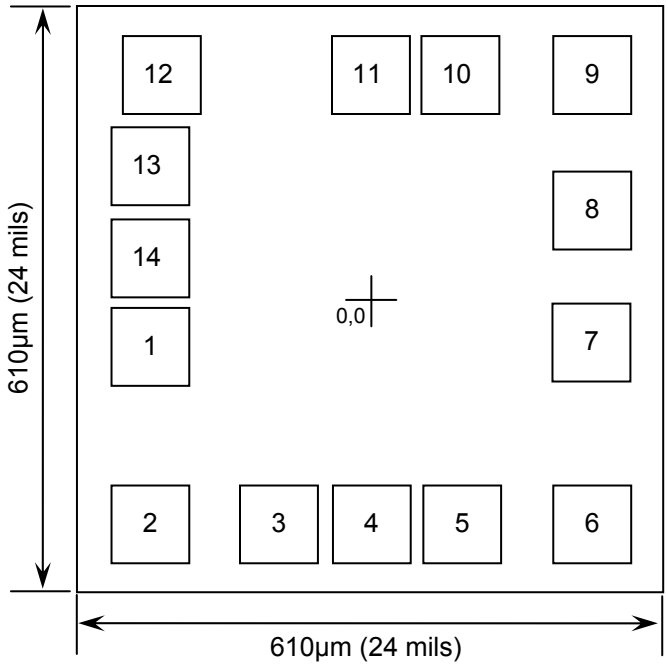
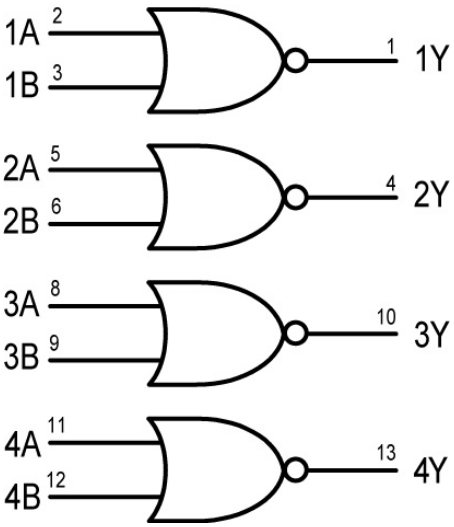
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	1Y	-230	-52
2	1A	-230	-230
3	1B	-95	-230
4	2Y	0	-230
5	2A	95	-230
6	2B	230	-230
7	GND	230	-45
8	3A	230	95
9	3B	230	230
10	3Y	95	230
11	4A	0	230
12	4B	-220	230
13	4Y	-230	140
14	V_{CC}	-230	45
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 14 = V_{CC}
Pad 7 = GND

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L
H = High level (steady state) L = Low level (steady state)		

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±50	mA
Power Dissipation in Still Air	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions[2] (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_A		-55	+125	°C
Input Rise or Fall Times	t_r, t_f	V_{CC} = 2V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6.0V	0	400	

2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				-55°C to 25°C	≤ 85°C	≤ 125°C	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				-55°C to 25°C	≤ 85°C	≤ 125°C	
Minimum High-Level Output Voltage	V_{OH}	2.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 2.4mA$	2.48	2.34	2.20	V
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	3.98	3.84	3.70	
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 5.2mA$	5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IL}$ or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{IL}$ or V_{IL} $\lvert I_{OUT} \rvert \le 2.4mA$	0.26	0.33	0.40	V
		4.5V	$V_{IN} = V_{IL}$ or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	0.26	0.33	0.40	
		6.0V	$V_{IN} = V_{IL}$ or V_{IL} $\lvert I_{OUT} \rvert \le 5.2mA$	0.26	0.33	0.40	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Leakage Current[3]	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	1	10	40	µA

AC Electrical Characteristics[3]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				-55°C to 25°C	≤ 85°C	≤ 125°C	
Maximum Propagation Delay, Input A or B to Output Y (Figure 1,2)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	75	95	110	ns
		3.0V		30	40	55	
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Output Rise and Fall Time, Any Output (Figure 1,2)	t_{TLH}, t_{THL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	75	95	110	ns
		3.0V		30	40	55	
		4.5V		15	19	22	
		6.0V		13	16	19	

3. Not production tested in die form, characterized by chip design and tested in package LAT.
4. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

AC Electrical Characteristics Continued[3]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				-55°C to 25°C	≤ 85°C	≤ 125°C	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[4]	C_{PD}	-	T_A = 25°C, V_{CC} =5.0V	TYPICAL			pF
				22			

3. Not production tested in die form, characterized by chip design and tested in package LAT.
4. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform

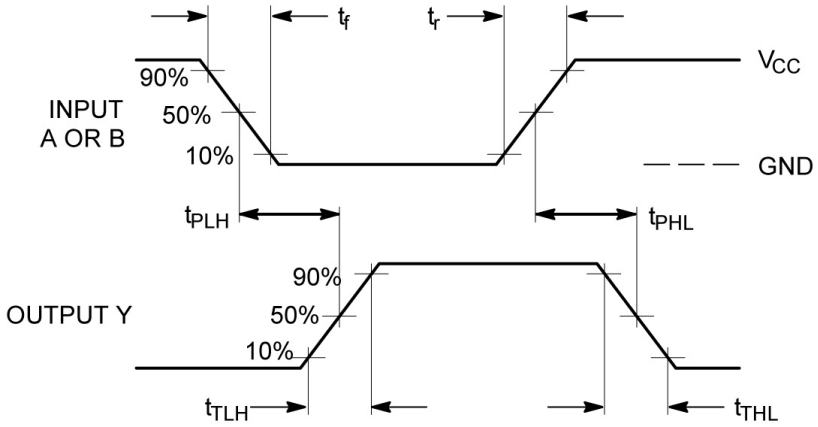
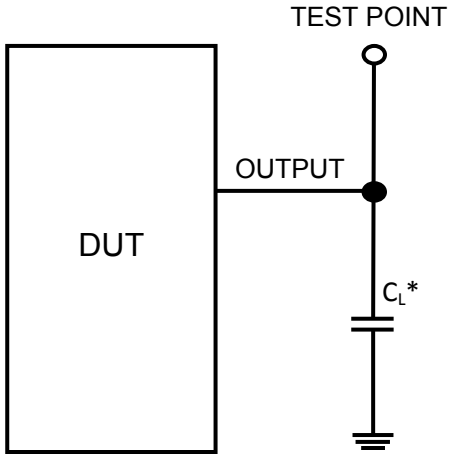


Figure 1 – Propagation Delay & Output Transition Time

Test Circuit



* Includes all probe and jig capacitance

Figure 2