



# CMOS 16-BIT 3.3V TO 5V LEVEL SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

IDT74ALVC164245

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{SK(O)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CCA} = 2.7V$  to 3.6V
- $V_{CCB} = 5V \pm 0.5V$
- CMOS power levels (0.4 $\mu$  W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP and TSSOP packages

## DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Suitable for heavy loads

## DESCRIPTION:

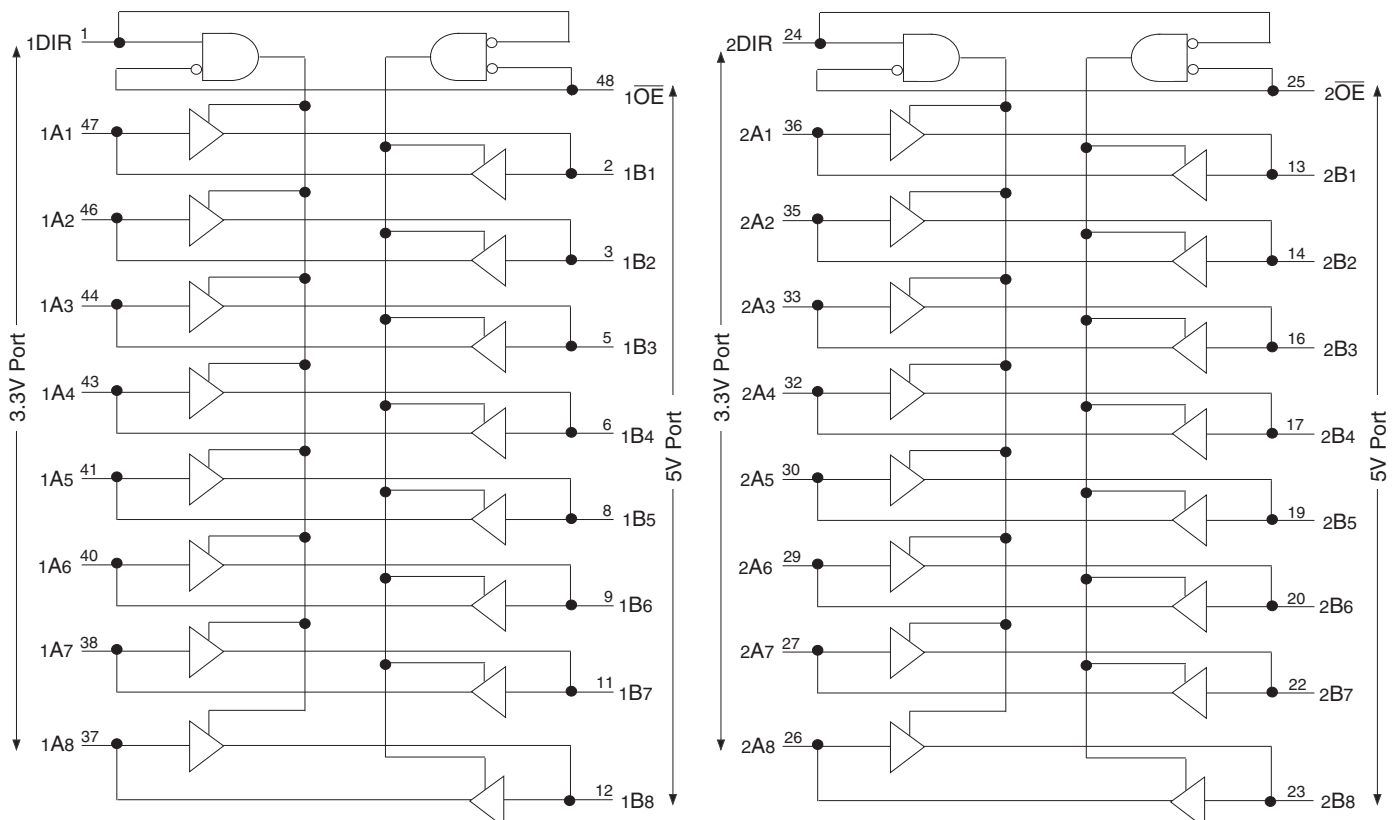
This 16-bit 3.3V to 5V level shifting transceiver is manufactured using advanced dual metal CMOS technology. The ALVC164245 contains two separate supply rails; B port has  $V_{CCB}$ , which is set at 5V, and A port has  $V_{CCA}$ , which is set to operate at 3.3V. This allows for translation from a 3.3V to 5V environment and vice-versa. This device is designed for asynchronous communication between data buses.

The ALVC164245 has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

## APPLICATIONS:

- Mixed 3.3V and 5V High Speed Systems
- 5V PCI Interface to 3.3V PC Bus Structures
- Telecommunication Legacy Systems with transitions from 5V to 3.3V

## FUNCTIONAL BLOCK DIAGRAM

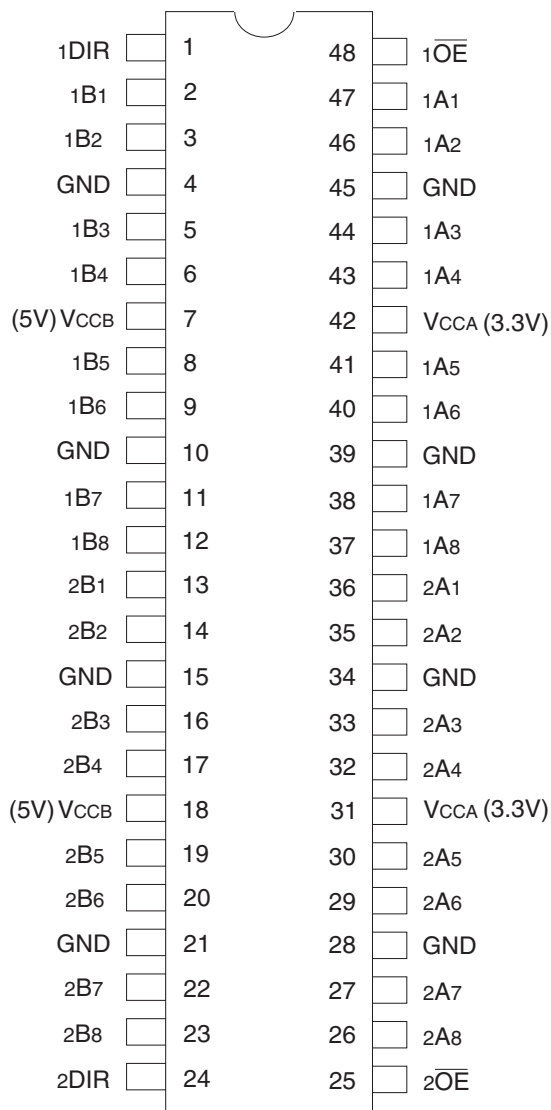


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**INDUSTRIAL TEMPERATURE RANGE**

**JULY 2018**

## PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PAG48	PAG
SSOP	PVG48	PVG

## PIN DESCRIPTION

Pin Names	Description
$\overline{xOE}^{(1)}$	Output Enable Inputs (Active LOW)
$xDIR^{(1)}$	Direction Output Controls
$xAx$	Port A Inputs or 3-State Outputs
$xBx$	Port B Inputs or 3-State Outputs

**NOTE:**  
1. All control inputs are powered off  $V_{CCA}$ .

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to +6	V
TSTG	Storage Temperature	-65 to +150	°C
$I_{OUT}$	DC Output Current	-50 to +50	mA
$I_{IK}$	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	±50	mA
$I_{OK}$	Continuous Clamp Current, $V_O < 0$	-50	mA
$I_{CC}$ $I_{SS}$	Continuous Current through each $V_{CC}$ or GND	±100	mA

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- $V_{CC}$  terminals.
- All terminals except  $V_{CC}$ .

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $F = 1.0\text{MHz}$ , $V_{CCA} = 3.3\text{V}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
$C_{IN}$	A Port Input Capacitance	$V_{IN} = 0\text{V}$	6.5	—	pF
$C_{I/O}$	A Port I/O Capacitance	$V_{IN} = 0\text{V}$	8.5	—	pF

**NOTE:**

- As applicable to the device type.

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $F = 1.0\text{MHz}$ , $V_{CCB} = 5\text{V}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
$C_{IN}$	B Port Input Capacitance	$V_{IN} = 0\text{V}$	6.5	—	pF
$C_{I/O}$	B Port I/O Capacitance	$V_{IN} = 0\text{V}$	6.5	—	pF

**NOTE:**

- As applicable to the device type.

## FUNCTION TABLE (EACH 8-BIT SECTION)<sup>(1)</sup>

Inputs		Outputs
$\overline{xOE}$	$xDIR$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (B PORT)<sup>(1)</sup>

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CCB} = 4.5\text{V}$ to $5.5\text{V}$	2	—	—	V
$V_{IL}$	Input LOW Voltage Level	$V_{CCB} = 4.5\text{V}$ to $5.5\text{V}$	—	—	0.8	V
$I_{IH}$	Input HIGH Current	$V_{CCB} = 5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{CCB} = 5.5\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current	$V_{CCB} = 5.5\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OZL}$	(3-State Output pins)		—	—	$\pm 10$	
$V_H$	Input Hysteresis	$V_{CCB} = 4.5\text{V}$	—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CCB} = 5.5\text{V}$ $V_{IN} = \text{GND}$ or $V_{CCB}$	—	0.1	40	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $3.4\text{V}$ , other inputs at $V_{CCB}$ or $\text{GND}$	—	—	750	$\mu\text{A}$

**NOTES:**

- $V_{CCA} = 2.7\text{V}$  to  $3.6\text{V}$ .
- Typical values are at  $V_{CC} = 5\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT)<sup>(1,2)</sup>

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(3)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CCA} = 2.7\text{V}$ to $3.6\text{V}$	2	—	—	V
$V_{IL}$	Input LOW Voltage Level	$V_{CCA} = 2.7\text{V}$ to $3.6\text{V}$	—	—	0.8	V
$I_{IH}$	Input HIGH Current	$V_{CCA} = 3.6\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{CCA} = 3.6\text{V}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current	$V_{CCA} = 3.6\text{V}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OZL}$	(3-State Output pins)		—	—	$\pm 10$	
$V_H$	Input Hysteresis	$V_{CCA} = 3.3\text{V}$	—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CCA} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or $V_{CCA}$	—	0.1	40	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CCA} - 0.6\text{V}$ , other inputs at $V_{CCA}$ or $\text{GND}$	—	—	750	$\mu\text{A}$

**NOTES:**

- $V_{CCB} = 5\text{V} \pm 0.5\text{V}$ .
- Control inputs  $\overline{\text{XDIR}}$ ,  $\overline{\text{OE}}$  are supplied from  $V_{CCA}$ .
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

### OUTPUT DRIVE CHARACTERISTICS, $V_{CCA} = 3.3V \pm 0.3V$ (A PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage (B Port to A Port)	$V_{CCA} = 2.7V$ to $3.6V$	$I_{OH} = -0.1mA$	$V_{CCA} - 0.2$	—	V
		$V_{CCA} = 2.7V$	$I_{OH} = -12mA$	2.2	—	
		$V_{CCA} = 3V$		2.4	—	
		$V_{CCA} = 3V$	$I_{OH} = -24mA$	2	—	
VOL	Output LOW Voltage (B Port to A Port)	$V_{CCA} = 2.7V$ to $3.6V$	$I_{OL} = 0.1mA$	—	0.2	V
		$V_{CCA} = 2.7V$	$I_{OL} = 12mA$	—	0.4	
		$V_{CCA} = 3V$	$I_{OL} = 24mA$	—	0.55	

**NOTE:**  
1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  
 $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $V_{CCA} = 3.3V \pm 0.3V$ .

### OUTPUT DRIVE CHARACTERISTICS, $V_{CCB} = 5V \pm 0.5V$ (B PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage (A Port to B Port)	$V_{CCB} = 4.5V$	$I_{OH} = -0.1mA$	4.3	—	V
		$V_{CCB} = 5.5V$		5.3	—	
		$V_{CCB} = 4.5V$	$I_{OH} = -24mA$	3.7	—	
		$V_{CCB} = 5.5V$		4.7	—	
VOL	Output LOW Voltage (A Port to B Port)	$V_{CCB} = 4.5V$	$I_{OL} = 0.1mA$	—	0.2	V
		$V_{CCB} = 5.5V$		—	0.2	
		$V_{CCB} = 4.5V$	$I_{OL} = 24mA$	—	0.55	
		$V_{CCB} = 5.5V$		—	0.55	

**NOTE:**  
1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  
 $T_A = -40^\circ C$  to  $+85^\circ C$ ;  $V_{CCB} = 5V \pm 0.5V$ .

## OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CCA} = 3.3\text{V}, V_{CCB} = 5\text{V}$		Unit
			Typical		
CPD	Power Dissipation Capacitance, Outputs enabled (A port or B port)	$C_L = 0\text{pF}, f = 10\text{MHz}$	56		pF
CPD	Power Dissipation Capacitance, Outputs disabled (A port or B port)		6		

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	$V_{CCB} = 5\text{V} \pm 0.5\text{V}$				Unit
		$V_{CCA} = 2.7\text{V}$		$V_{CCA} = 3.3\text{V} \pm 0.3\text{V}$		
		Min.	Max.	Min.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay xAx to xBx	—	5.9	1	5.8	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay xBx to xAx	—	6.7	1.2	5.8	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{xOE}$ to xBx	—	9.3	1	8.9	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{xOE}$ to xAx	—	10.2	2	9.1	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{xOE}$ to xBx	—	9.2	2.1	9.4	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{xOE}$ to xAx	—	9	2.9	8.6	ns

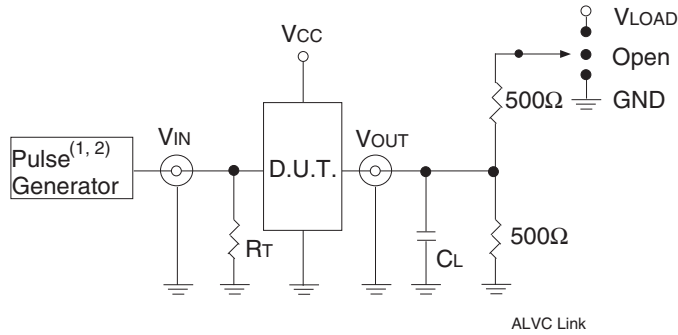
**NOTE:**

1. See TEST CIRCUITS AND WAVEFORMS.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

TEST CIRCUITS AND WAVEFORMS FOR  $V_{CCA} = 3.3V \pm 0.3V$  AND  $V_{CCA} = 2.7V$

TEST CONDITIONS

Symbol	$V_{CCA} = 3.3V \pm 0.3V$	$V_{CCA} = 2.7V$	Unit
$V_{LOAD}$	6	6	V
$V_{IH}$	3	3	V
$V_T$	1.5	1.5	V
$V_{LZ}$	300	300	mV
$V_{OH} - V_{HZ}$	300	300	mV
$C_L$	50	50	pF



Test Circuit for All Outputs

DEFINITIONS:

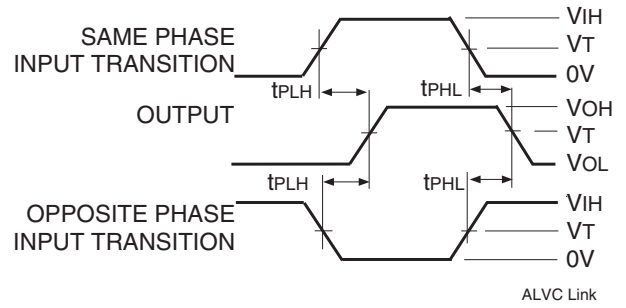
$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator.

NOTE:

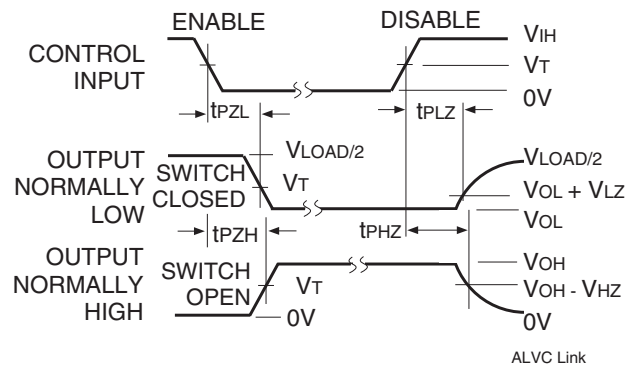
1. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .

SWITCH POSITION

Test	Switch
Disable Low Enable Low	$V_{LOAD}$
Disable High Enable High	GND
All Other Tests	Open



Propagation Delay



Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

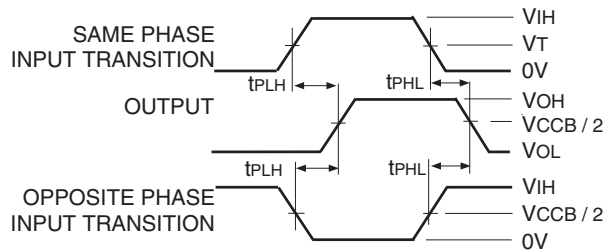
TEST CIRCUITS AND WAVEFORMS FOR  $V_{CCB} = 5V \pm 0.5V$

TEST CONDITIONS (USE  $V_{CCA}$  TEST CIRCUIT)

Symbol	$V_{CCB}^{(1)} = 5V \pm 0.2V$	Unit
$V_{LOAD}$	$2 \times V_{CCB}$	V
$V_{IH}$	2.7	V
$V_T$	$1.5 \text{ or } V_{CCB} / 2$	V
$V_{LZ}$	20% of $V_{CCB}$	mV
$V_{HZ}$	80% of $V_{CCB}$	mV
$C_L$	50	pF

NOTE:

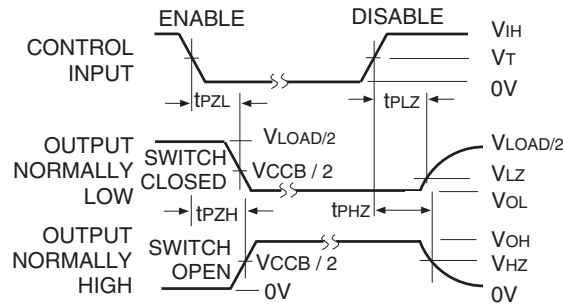
1. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_f \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .



Propagation Delay

NOTES:

1. For  $t_{sk(o)}$  OUTPUT1 and OUTPUT2 are any two outputs.
2. For  $t_{sk(b)}$  OUTPUT1 and OUTPUT2 are in the same bank.

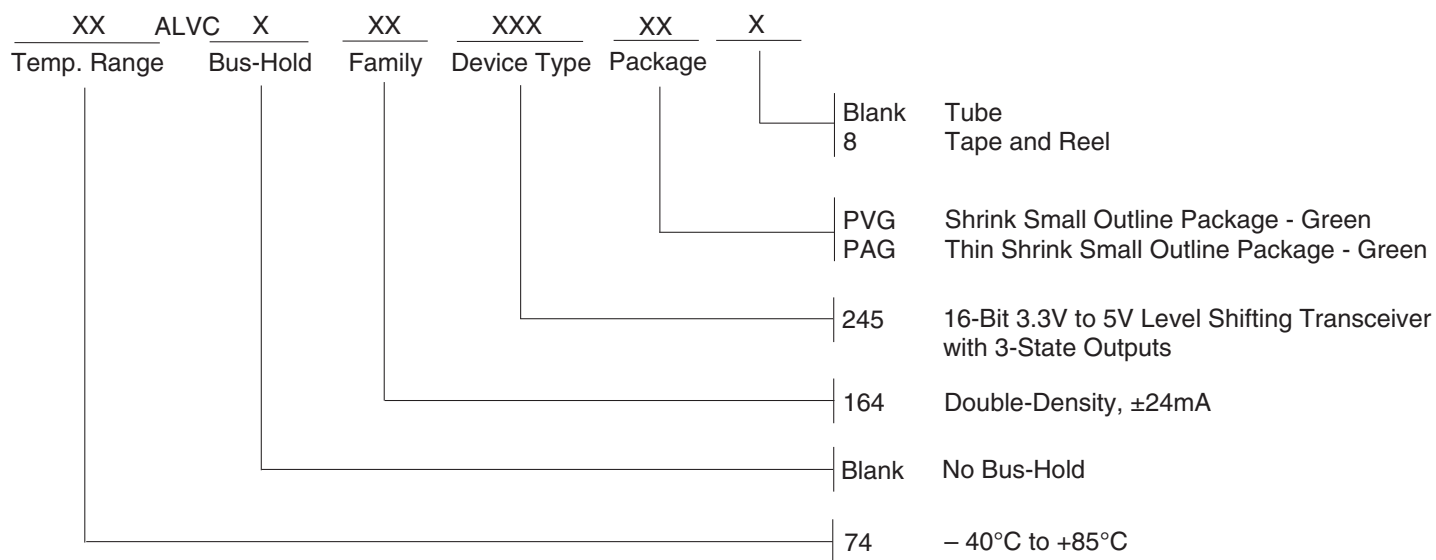


Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

## ORDERING INFORMATION



## Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
	74ALVC164245PAG	PAG48	TSSOP	C
	74ALVC164245PAG8	PAG48	TSSOP	C
	74ALVC164245PVG	PVG48	SSOP	C
	74ALVC164245PVG8	PVG48	SSOP	C

## Datasheet Document History

07/30/2018 Pg. 2, 8

Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram adding Tube, Tape and Reel. Added new table of orderable part information.



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
www.idt.com

**for Tech Support:**  
logichelp@idt.com