19-3208; Rev 1; 8/10

EVALUATION KIT AVAILABLE

12-Bit, 4.0Gsps High-Dynamic Performance Wideband DAC

MAX19693

General Description

The MAX19693 12-bit, 4.0Gsps digital-to-analog converter (DAC) enables direct digital synthesis of high-frequency and wideband signals. The DAC has been optimized for wideband communications, radar, and instrumentation applications. The MAX19693 provides excellent spurious and noise performance and can be used for synthesis of wideband signals in the frequency range from DC to nearly 2GHz. The 4.0Gsps update rate enables digital synthesis of signals with more than 1.5GHz bandwidth.

The MAX19693 includes four 12-bit multiplexed low-voltage differential signaling (LVDS) input ports, each operating at up to 1GHz in double data rate (DDR) or quad data rate (QDR) mode. The DAC accepts a clock at 1/2 the DAC update rate, as conversion is triggered on both rising and falling clock edges. The input data rate is 1/4 the DAC update rate (1/2 the clock rate). The MAX19693 provides an LVDS data clock output to simplify interfacing to FPGA or ASIC devices.

The MAX19693 is a current-steering DAC with an integrated, self-calibrated 50Ω differential output termination to ensure optimum dynamic performance. The MAX19693 operates from 3.3V and 1.8V power supplies and consumes 1180mW at 4.0Gsps. The MAX19693 is specified over the extended temperature range (-40°C to +85°C) and is available in a compact 11mm x 11mm, 169 CSBGA package.

Applications

Radar Waveform and LO Signal Synthesis

Digital IF Generation in X-Band Transmitters

Electronic Warfare

Arbitrary Waveform Generators

Direct Digital Synthesis

Automatic Test Equipment

Features

- **4.0Gsps Output Update Rate**
- **Industry-Leading Dynamic Performance**
  - **SFDR* = 76dBc at f_{OUT} = 400MHz**
  - **SFDR* = 70dBc at f_{OUT} = 800MHz**
  - **Wideband Noise Spectral Density = -164dBm/Hz**
- **Low-Power Operation**
  - **770mW (f_{DAC} = 2000Msps)**
  - **1180mW (f_{DAC} = 4000Msps)**
- **4:1 Multiplexed LVDS Inputs**
  - **Up to 1000Mwps each port**
- **Internal 50Ω Differential Output Termination**
- **Input Register Scan Mode for In-Circuit Continuity Verification**
- **Compact 11mm x 11mm, 169 CSBGA Package**
- **Evaluation Kit Available (Order MAX19693EVKIT)**

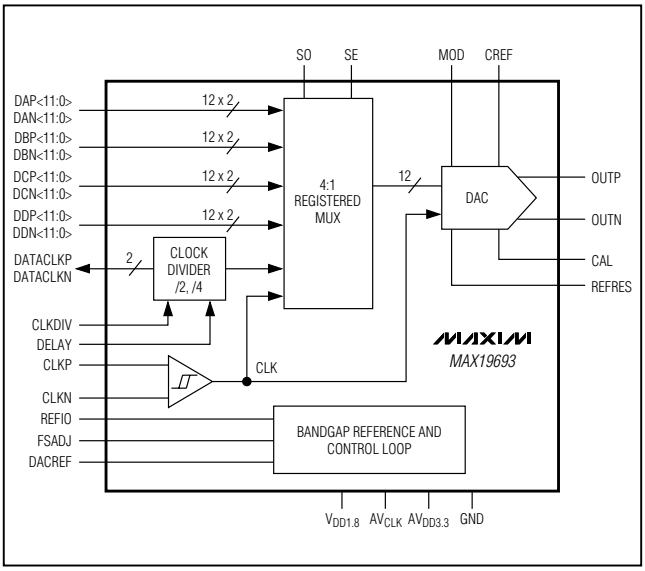
**Excludes $f_{DAC}/2$, $f_{DAC}/4$, and $f_{DAC}/2$ - f_{OUT} spurs, which are specified separately.*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX19693EXW-D	-40°C to +85°C	169 CSBGA
MAX19693EXW+D	-40°C to +85°C	169 CSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.
D = Dry pack.

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

12-Bit, 4.0Gsps High-Dynamic Performance Wideband DAC

ABSOLUTE MAXIMUM RATINGS

$AV_{DD3.3}$ to GND, DACREF .....-0.3V to +3.9V
$V_{DD1.8}$, AV_{CLK} to GND, DACREF .....-0.3V to +2.1V
REFIO, FSADJ to GND, DACREF .....-0.3V to ($AV_{DD3.3}$ + 0.3V)
OUTP, OUTN to GND, DACREF .....-0.3V to ($AV_{DD3.3}$ + 1.0V)
SE, SO, CREF to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
MOD, DELAY, CLKDIV, REFRES,
CAL to GND, DACREF.....-0.3V to ($AV_{DD3.3}$ + 0.3V)
CLKP, CLKN to GND, DACREF.....-0.3V to (AV_{CLK} + 0.3V)
DAP0–DAP11, DBP0–DBP11,
DCP0–DCP11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DDP0–DDP11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DAN0–DAN11, DBN0–DBN11,
DCN0–DCN11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DDN0–DDN11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DATACLKP, DATACLKN to GND,
DACREF .....-0.3V to ($V_{DD1.8}$ + 0.3V)
DATACLKP, DATACLKN, SO Continuous Current.....8mA
Continuous Power Dissipation (T_A = +70°C)
169-Pin CSBGA (derate 33.3mW/°C above +70°C) ..2666.7mW
Thermal Resistance θ_{JA} (Note 1).....+18°C/W
Operating Temperature Range.....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Note 1: Thermal resistance based on a 4.5in x 5.5in multilayer board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution				12		Bits
Integral Nonlinearity	INL	Measured differentially		±1.2		LSB
Differential Nonlinearity	DNL	Measured differentially		±0.8		LSB
Offset Voltage Error	OS	Measured differentially, no external load resistors	-0.5	±0.1	+0.5	%FS
Offset Drift				±10		ppm/°C
Full-Scale Output Current	I_{OUT}	(Note 3)	8		20	mA
Output-Current Gain Error	GE		-4		+4	%FS
Output-Voltage Gain Drift		Internal reference		-0.003		dB/°C
		External reference		-0.0025		
Maximum CW Output Power	P_{OUT}	Differential, into 50Ω load		-2.6		dBm
Output Resistance	R_{OUT}	Differential, $V_{CAL} \geq 0.7 \times AV_{DD3.3}$ (Note 4)		50		Ω
Output Return Loss	S_{11}	f_{OUT} = 500MHz (Note 5)		20		dB

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Notes 5, 6)							
Minimum Clock Rate	f_{CLK}					10	MHz
Maximum Clock Rate	f_{CLK}			2000			MHz
Minimum Output Update Rate	f_{DAC}					20	Msps
Maximum Output Update Rate	f_{DAC}			4000			Msps
Wideband Noise Spectral Density	NSD	f_{DAC} = 2000Msps, f_{OUT} = 200MHz, -6dBFS			-165		dBm/Hz
		f_{DAC} = 4000Msps, f_{OUT} = 200MHz, -6dBFS			-164		
Spurious-Free Dynamic Range over Nyquist (Note 7)	SFDR	f_{DAC} = 1000Msps	f_{OUT} = 50MHz, -3dBFS		76		dBc
			f_{OUT} = 100MHz, -3dBFS		76		
			f_{OUT} = 200MHz, -3dBFS		76		
			f_{OUT} = 300MHz, -3dBFS		76		
		f_{DAC} = 2000Msps	f_{OUT} = 200MHz, -3dBFS		73		
			f_{OUT} = 400MHz, 0dBFS	62	69		
			f_{OUT} = 600MHz, -3dBFS		75		
			f_{OUT} = 800MHz, -3dBFS		70		
		f_{DAC} = 3000Msps	f_{OUT} = 200MHz, -3dBFS		75		
			f_{OUT} = 500MHz, -3dBFS		70		
			f_{OUT} = 900MHz, -3dBFS		71		
			f_{OUT} = 1200MHz, -3dBFS		68		
		f_{DAC} = 4000Msps	f_{OUT} = 200MHz, -3dBFS		75		
			f_{OUT} = 400MHz, -6dBFS	62	69		
			f_{OUT} = 800MHz, -3dBFS		63		
			f_{OUT} = 1500MHz, -3dBFS		62		
$f_{DAC}/4$ Clock Spur		f_{DAC} = 1000Msps	f_{OUT} = 200MHz, 0dBFS		-87		dBm
		f_{DAC} = 2000Msps			-98		
		f_{DAC} = 3000Msps			-81		
		f_{DAC} = 4000Msps			-81		
$f_{DAC}/2$ Clock Spur		f_{DAC} = 1000Msps	f_{OUT} = 200MHz, 0dBFS		-57		dBm
		f_{DAC} = 2000Msps			-50		
		f_{DAC} = 3000Msps			-54		
		f_{DAC} = 4000Msps			-50		
$f_{DAC}/2$ - f_{OUT} Spur		f_{DAC} = 1000Msps	f_{OUT} = 400MHz, -6dBFS		-40		dBc
		f_{DAC} = 2000Msps			-40		
		f_{DAC} = 3000Msps			-40		
		f_{DAC} = 4000Msps			-40		
Minimum Output Bandwidth	BW_{-3dB}	(Note 8)			1500		MHz

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ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Two-Tone IMD	TTIMD	f_{DAC} = 2000Msps	f_{OUT1} = 200MHz, -7dBFS, f_{OUT2} = 210MHz, -7dBFS		-81		dBc
		f_{DAC} = 2000Msps	f_{OUT1} = 400MHz, -7dBFS, f_{OUT2} = 410MHz, -7dBFS		-82		
		f_{DAC} = 2000Msps	f_{OUT1} = 600MHz, -7dBFS, f_{OUT2} = 610MHz, -7dBFS		-73		
		f_{DAC} = 4000Msps	f_{OUT1} = 800MHz, -7dBFS, f_{OUT2} = 810MHz, -7dBFS		-62		
REFERENCE							
Internal Reference Voltage Range	V_{REFIO}			1.1	1.2	1.3	V
Reference Input Compliance Range	V_{REFIOR}			0.50		1.25	V
Reference Input Resistance	R_{REFIO}				10		kΩ
Reference Voltage Drift	TCO_{REF}				-50		ppm/°C
ANALOG OUTPUT TIMING (Note 9)							
Output Fall Time	t_{FALL}	90% to 10%			270		ps
Output Rise Time	t_{RISE}	10% to 90%			270		ps
Settling Time	t_S	Settling to 0.1%			3.5		ns
		Settling to 0.025%			4.5		
Output Propagation Delay	t_{PD}				1.3		ns
TIMING CHARACTERISTICS (Note 10)							
Data-to-Clock Setup Time	t_{SETUP}	Referenced to rising edge of data clock		1.41			ns
Data-to-Clock Hold Time	t_{HOLD}	Referenced to rising edge of data clock		-0.88			ns
LVDS LOGIC INPUTS (DAP11–DAP0, DAN11–DAN0, DBP11–DBP0, DBN11–DBN0, DCP11–DCP0, DCN11–DCN0, DDP11–DDP0, DDN11–DDN0)							
Differential Input Logic-High	V_{IH}			100			mV
Differential Input Logic-Low	V_{IL}					-100	mV
Common-Mode Voltage Range	V_{COM}			1.125		1.375	V
Differential Input Resistance	R_{IN}			85		130	Ω
Input Capacitance	C_{IN}				1.5		pF

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V CMOS LOGIC INPUTS (CLKDIV, DELAY, MOD)						
Input Logic-High	$V_{IH3.3}$		0.7 x $AV_{DD3.3}$			V
Input Logic-Low	$V_{IL3.3}$				0.3 x $AV_{DD3.3}$	V
Input Leakage Current	$I_{IN3.3}$		-5		+5	µA
Input Capacitance	$C_{IN3.3}$			3		pF
1.8V CMOS LOGIC INPUT (SE)						
Input Logic-High	$V_{IH1.8}$		0.7 x $V_{DD1.8}$			V
Input Logic-Low	$V_{IL1.8}$				0.3 x $V_{DD1.8}$	V
Input Leakage Current	$I_{IN1.8}$		-5		+5	µA
Input Capacitance	$C_{IN1.8}$			3		pF
1.8V CMOS LOGIC OUTPUT (SO)						
Output Logic-High	$V_{OH1.8}$	I_{SOURCE} = 100µA	0.7 x $V_{DD1.8}$			V
Output Logic-Low	$V_{OL1.8}$	I_{SINK} = 100µA			0.3 x $V_{DD1.8}$	V
CLOCK INPUTS (CLKP, CLKN)						
Minimum Clock Input Power (Note 11)	P_{CLK}	f_{DAC} ≤ 3Gsps		0		dBm
		f_{DAC} > 3Gsps		9		
Maximum Clock Input Power	P_{CLK}	(Note 11)		15		dBm
Common-Mode Voltage Range	V_{COMCLK}		0.55	AV_{CLK}/3	0.65	V
Input Resistance	R_{CLK}	Differential		100		Ω
Input Capacitance	C_{CLK}			2		pF
DATA CLOCK OUTPUTS (DATACLKP, DATACLKN)						
Differential Output	V_{DCLK}	With 100Ω differential termination	±0.25	±0.35	±0.45	V
Output Rise and Fall Time	t_R, t_F	With 100Ω differential termination		0.5		ns
Common-Mode Voltage Range	V_{COM}		1.125	1.25	1.375	V

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ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

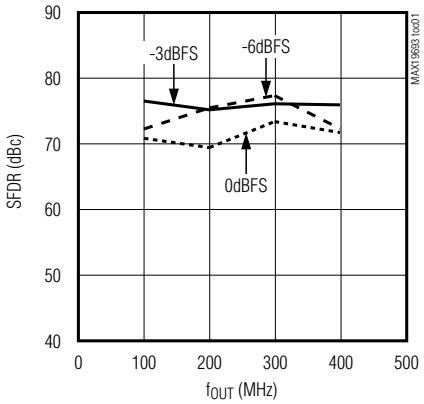
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Analog Supply Voltage Range	$AV_{DD3.3}$			3.1	3.3	3.5	V
1.8V Supply Voltage Range	$V_{DD1.8}$			1.7	1.8	1.9	V
Clock Supply Voltage Range	AV_{CLK}			1.7	1.8	1.9	V
Analog Supply Current	$I_{AVDD3.3}$	f_{DAC} = 2000Msps	f_{OUT} = 100MHz, 0dBFS		106		mA
		f_{DAC} = 4000Msps			106	118	
1.8V Supply Current	$I_{VDD1.8}$	f_{DAC} = 2000Msps			74		mA
		f_{DAC} = 4000Msps			148	190	
Clock Supply Current	I_{AVCLK}	f_{DAC} = 2000Msps			157		mA
		f_{DAC} = 4000Msps			313	390	
Power Dissipation	P_{DISS}	f_{DAC} = 2000Msps			770		mW
		f_{DAC} = 4000Msps			1180	1435	

Note 2: All specifications are 100% tested at $T_A \geq$ +25°C. Specifications at $T_A <$ +25°C are guaranteed by design and characterization.
Note 3: Nominal full-scale current $I_{OUT} = 32 \times I_{REF}$.
Note 4: R_{OUT} can be set to 50Ω as described in the *Output Resistor Calibration* section.
Note 5: Transformer-coupled output (Figure 13, $V_{CAL} \geq 0.7 \times AV_{DD3.3}$).
Note 6: CLK input = +10dBm, AC-coupled sine wave.
Note 7: Excludes $f_{DAC}/2$, $f_{DAC}/4$, and $f_{DAC}/2 - f_{OUT}$ spurs, which are specified separately.
Note 8: Excludes sinc rolloff inherent in the DAC. Measured single-ended into 50Ω termination.
Note 9: Measured differentially into a 50Ω termination resistor.
Note 10: Guaranteed by design and characterization.
Note 11: Transformer-coupled clock input (Figure 5).

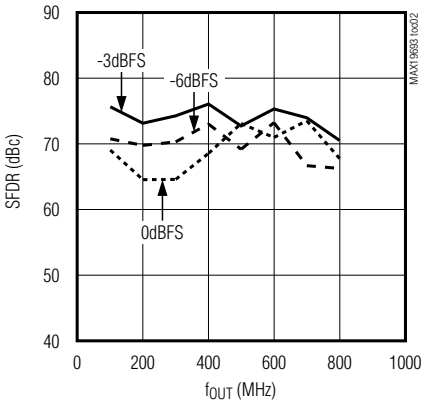
Typical Operating Characteristics

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 510Ω, R_{SET} = 2kΩ, P_{CLK} = +10dBm, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output (Figure 13), I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

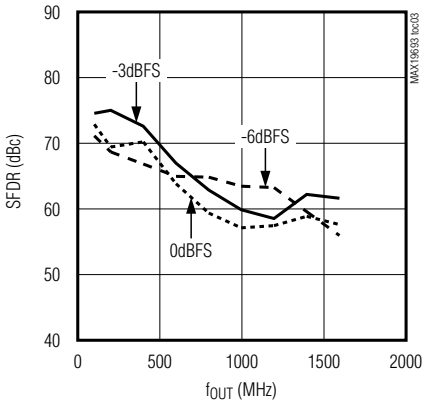
SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 1000Msps)



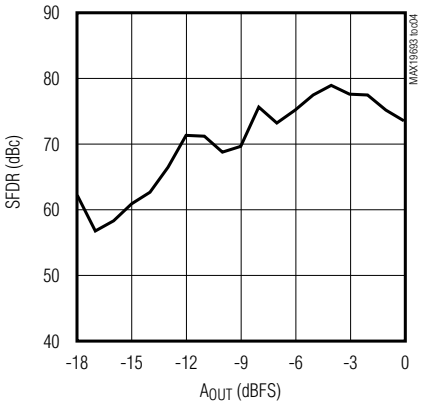
SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 2000Msps)



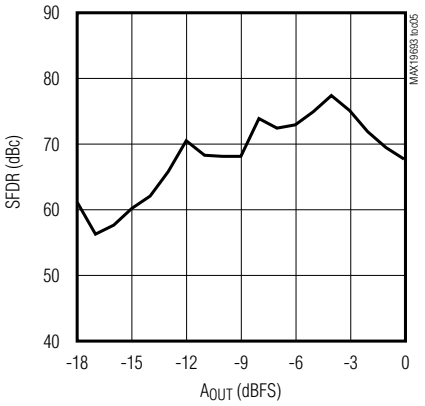
SFDR vs. OUTPUT FREQUENCY (f_{DAC} = 4000Msps)



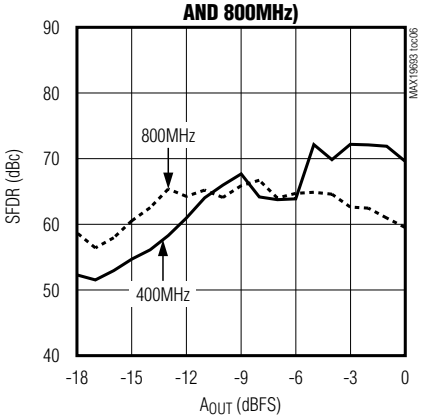
SFDR vs. OUTPUT AMPLITUDE (f_{DAC} = 1000Msps, f_{OUT} = 200MHz)



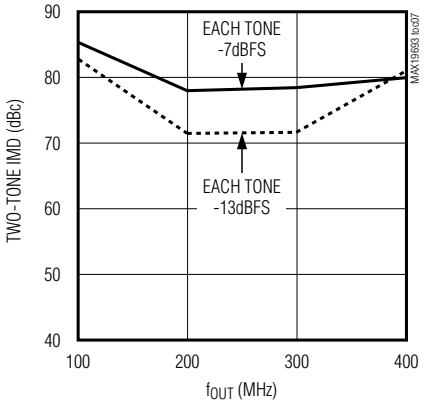
SFDR vs. OUTPUT AMPLITUDE (f_{DAC} = 2000Msps, f_{OUT} = 400MHz)



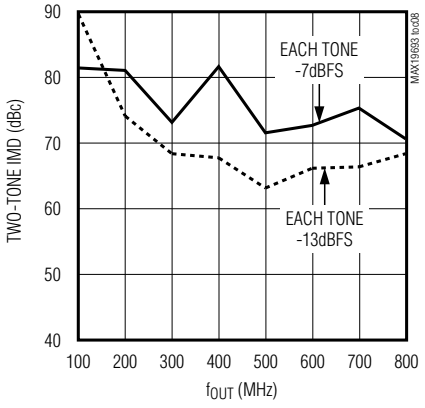
SFDR vs. OUTPUT AMPLITUDE (f_{DAC} = 4000Msps, f_{OUT} = 400MHz AND 800MHz)



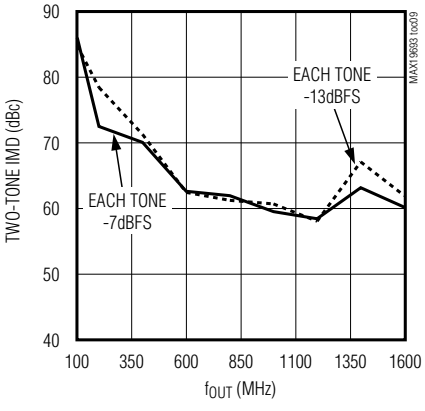
TWO-TONE IMD vs. OUTPUT FREQUENCY (f_{DAC} = 1000Msps)



TWO-TONE IMD vs. OUTPUT FREQUENCY (f_{DAC} = 2000Msps)



TWO-TONE IMD vs. OUTPUT FREQUENCY (f_{DAC} = 4000Msps)



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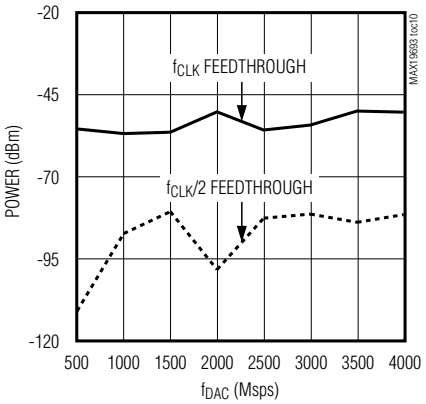
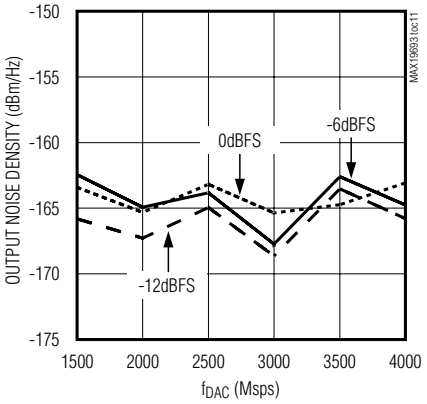
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 510Ω, R_{SET} = 2kΩ, P_{CLK} = +10dBm, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output (Figure 13), I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

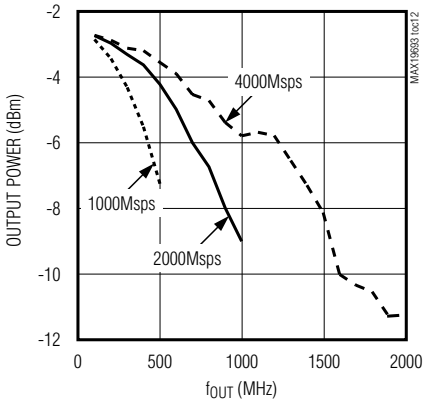
CLOCK FEEDTHROUGH vs. DAC UPDATE RATE (f_{OUT} = 200MHz, A_{OUT} = 0dBFS)



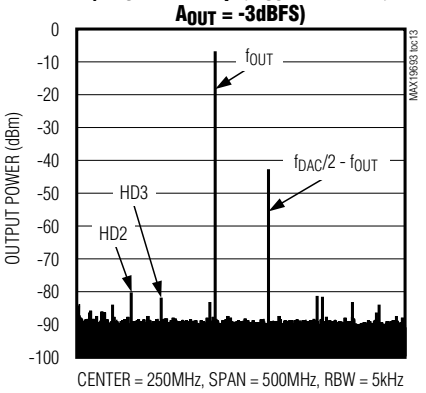
OUTPUT NOISE DENSITY vs. DAC UPDATE RATE (f_{OUT} = 200MHz)



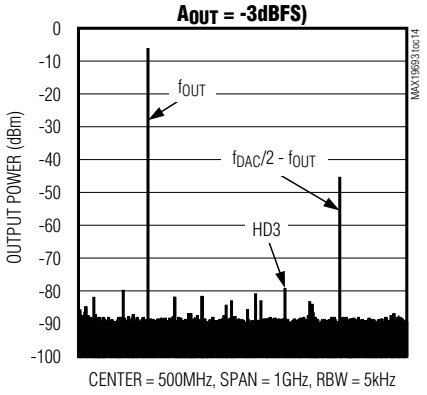
OUTPUT POWER vs. OUTPUT FREQUENCY (A_{OUT} = 0dBFS)



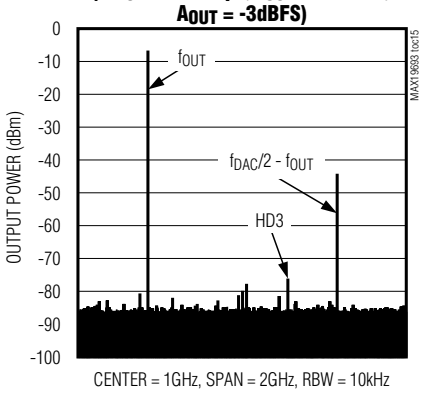
SFDR SPECTRAL PLOT (f_{DAC} = 1000Msps, f_{OUT} = 209MHz, A_{OUT} = -3dBFS)



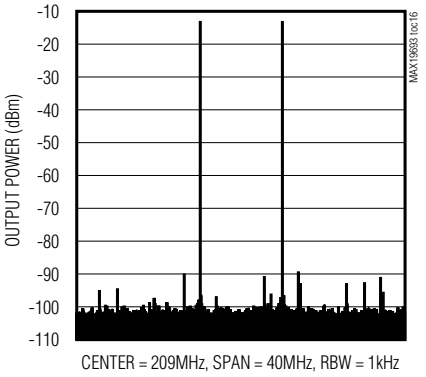
SFDR SPECTRAL PLOT (f_{DAC} = 2000Msps, f_{OUT} = 209MHz, A_{OUT} = -3dBFS)



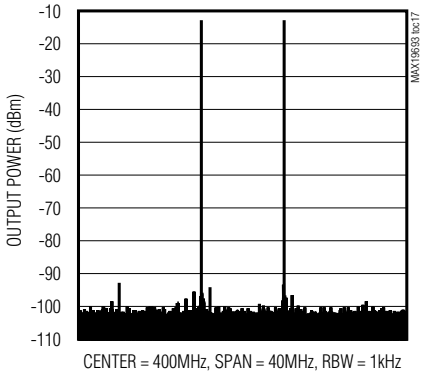
SFDR SPECTRAL PLOT (f_{DAC} = 4000Msps, f_{OUT} = 425MHz, A_{OUT} = -3dBFS)



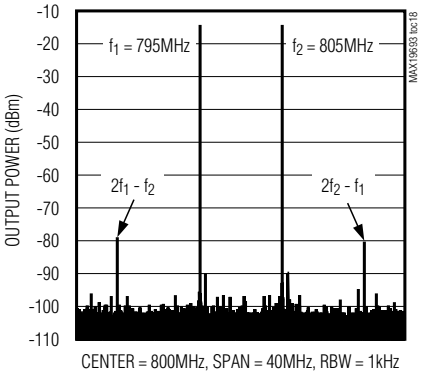
TWO-TONE IMD SPECTRAL PLOT (f_{DAC} = 1000Msps, f_1 = 204MHz AND f_2 = 214MHz, A_{OUT} = -3dBFS)



TWO-TONE IMD SPECTRAL PLOT (f_{DAC} = 2000Msps, f_1 = 395MHz AND f_2 = 405MHz, A_{OUT} = -3dBFS)



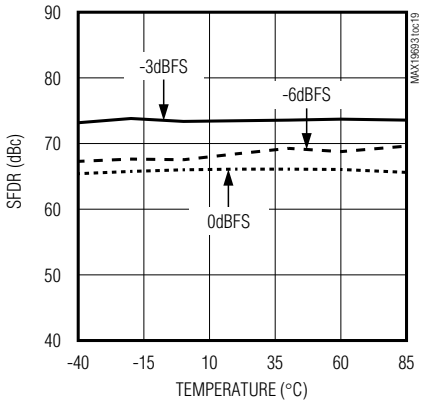
TWO-TONE IMD SPECTRAL PLOT (f_{DAC} = 4000Msps, f_1 = 795MHz AND f_2 = 805MHz, A_{OUT} = -3dBFS)



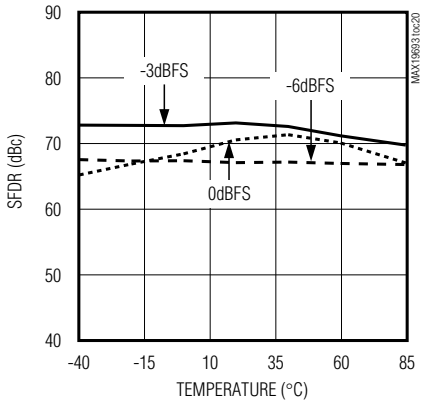
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 510Ω, R_{SET} = 2kΩ, P_{CLK} = +10dBm, V_{REFIO} = external 1.25V, V_{CAL} = 3.3V, V_{MOD} = 0V, transformer-coupled differential output (Figure 13), I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

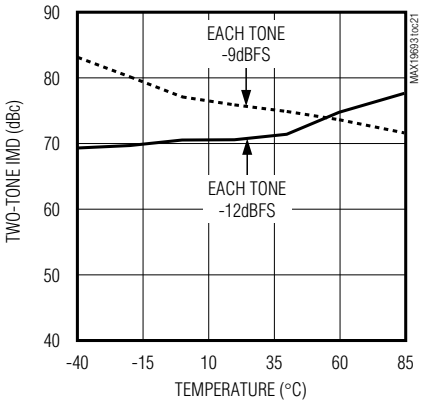
SFDR vs. TEMPERATURE (f_{DAC} = 2000Msps, f_{OUT} = 200MHz)



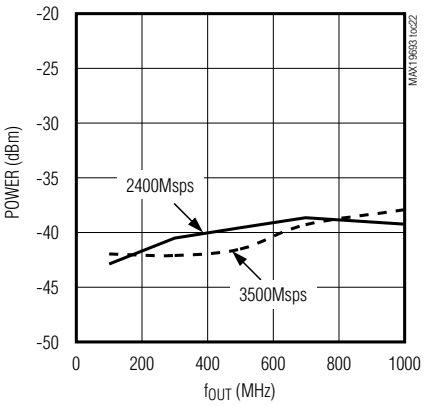
SFDR vs. TEMPERATURE (f_{DAC} = 4000Msps, f_{OUT} = 400MHz)



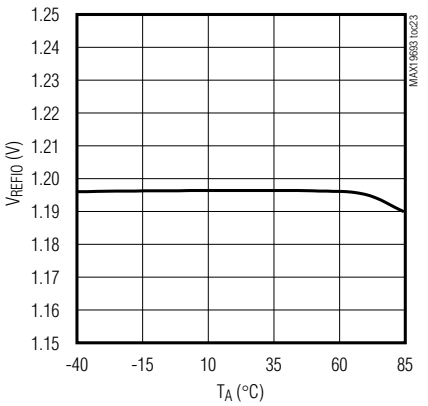
TWO-TONE IMD vs. TEMPERATURE (f_{DAC} = 4000Msps, f_{OUT} = 400MHz)



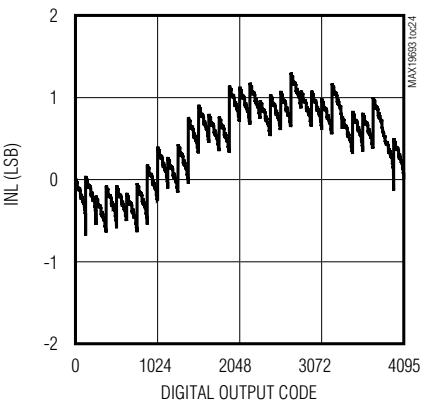
$f_{CLK}/2$ - f_{OUT} SPUR vs. OUTPUT FREQUENCY (A_{OUT} = 0dBFS, CLKDIV = 0)



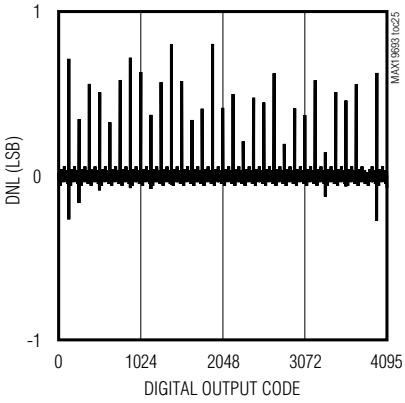
INTERNAL REFERENCE (REFIO) VOLTAGE vs. TEMPERATURE



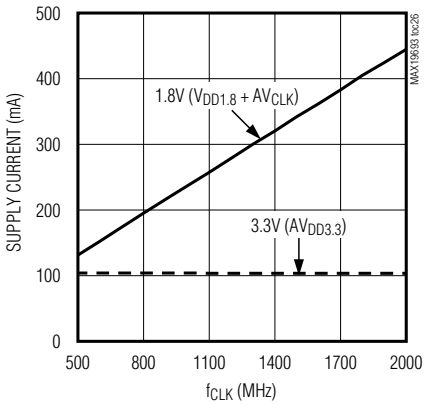
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



SUPPLY CURRENT vs. CLK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = 0dBFS)



12-Bit, 4.0Gsps High-Dynamic Performance Wideband DAC

Pin Description

PIN	NAME	FUNCTION
A1	REFIO	Reference Input/Output. Internal 1.2V bandgap reference output. REFIO has a 10kΩ series resistance and can be driven using an external reference. Connect a 1µF capacitor between REFIO and DACREF.
A2	FSADJ	Full-Scale Adjust Input. Sets the full-scale output current of the DAC. To obtain a 20mA full-scale output current using the internal reference, connect a 1.92kΩ resistor between FSADJ and DACREF.
A3	DACREF	Current-Set Resistor Return Path. To obtain a 20mA full-scale output current using the internal reference, connect a 1.92kΩ resistor between FSADJ and DACREF. DACREF is internally connected to AGND. **DO NOT CONNECT DACREF TO EXTERNAL GROUND.**
A4, A5, A7, A9	$AV_{DD3.3}$	Analog 3.3V Supply Voltage. Accepts a 3.1V to 3.5V supply voltage range. Connect 0.047µF bypass capacitors between each $AV_{DD3.3}$ node and GND.
A6	OUTP	Positive Terminal of Differential DAC Output. An internal calibrated 25Ω resistor connects OUTP to $AV_{DD3.3}$.
A8	OUTN	Negative Terminal of Differential DAC Output. An internal calibrated 25Ω resistor connects OUTN to $AV_{DD3.3}$.
A10, B10, C2, C3, C10, E1–E4, E10–E13, F13	$V_{DD1.8}$	Analog 1.8V Supply Voltage. Accepts a 1.7V to 1.9V supply voltage range. Connect 0.047µF bypass capacitors between each $V_{DD1.8}$ node and GND.
A11, A13, B5–B9, B11, C4–C9, C11, D1–D11, D13, E5–E9, G13	GND	Ground. Connect GND to the ground plane with minimum inductance.
A12, B12, C12, D12	AV_{CLK}	Clock 1.8V Supply Voltage. Accepts a 1.7V to 1.9V supply voltage range. Connect 0.047µF bypass capacitors between each AV_{CLK} node and GND.
B1	CREF	Noise Bypass Node. A 1µF capacitor between CREF and DACREF band limits the phase noise.
B2	REFRES	Calibration Reference Resistor Input. Connect a 510Ω resistor between REFRES and $AV_{DD3.3}$. The internal analog output resistors are calibrated to this external resistor.
B3	N.C.	No Connection. **Leave unconnected, or connect to ground.**
B4	MOD	$f_{DAC}/2$ or f_{CLK} Modulation Control Input. MOD = 1: Modulation ON MOD = 0: Modulation OFF MOD is a 3.3V CMOS input with an internal pulldown resistor.
C13	CLKP	Converter Clock Positive Input. An internal 100Ω termination resistor connects CLKP to CLKN.
B13	CLKN	Converter Clock Negative Input. An internal 100Ω termination resistor connects CLKP to CLKN.
C1	CAL	DAC Output Resistance Calibration Input. Calibration of the internal output resistors is initiated by a rising edge on CAL. CAL = 1: Output resistor calibration is held CAL = 0: Output resistors are uncalibrated CAL is a 3.3V CMOS input with an internal pulldown resistor. The clock must be operating to calibrate and to hold calibration. Leakage current is less than ±5µA.

Pin Description (continued)

PIN	NAME	FUNCTION
F6–F3, F1, F2, H6–H1	DAP11–DAP0	A-Channel Positive LVDS Data Inputs. DAP11 is the MSB. Input coding in offset binary format.
G6–G3, G1, G2, J6–J1	DAN11–DAN0	A-Channel Negative LVDS Data Inputs
K1–K4, M1–M4, K5, M5, K6, M6	DBP11–DBP0	B-Channel Positive LVDS Data Inputs. DBP11 is the MSB. Input coding in offset binary format.
L1–L4, N1–N4, L5, N5, L6, N6	DBN11–DBN0	B-Channel Negative LVDS Data Inputs
M7, K7, M8, K8, M9–M12, K9, K10, K11, L12	DCP11–DCP0	C-Channel Positive LVDS Data Inputs. DCP11 is the MSB. Input coding in offset binary format.
N7, L7, N8, L8, N9–N12, L9, L10, L11, K12	DCN11–DCN0	C-Channel Negative LVDS Data Inputs
G7, J7, J12–J8, G12–G8	DDP11–DDP0	D-Channel Positive LVDS Data Inputs. DDP11 is the MSB. Input coding in offset binary format.
F7, H7, H12–H8, F12–F8	DDN11–DDN0	D-Channel Negative LVDS Data Inputs
J13	DATACLKP	LVDS Data Clock Positive Output
H13	DATACLKN	LVDS Data Clock Negative Output
K13	DELAY	Data Clock Delay Mode Input. Adjusts the delay of the output data clock. DELAY = 0: No delay added DELAY = 1: Add delay of 1/2 input data period (one DAC clock cycle) DELAY is a 3.3V CMOS input with an internal pulldown resistor.
L13	CLKDIV	Data Clock Divide Mode Input. CLKDIV = 1: (DDR mode) Data clock rate = input data rate/2 ($f_{CLK}/4$) CLKDIV = 0: (QDR mode) Data clock rate = input data rate/4 ($f_{CLK}/8$) CLKDIV is a 3.3V CMOS input with an internal pulldown resistor.
M13	SE	Scan Enable Input. SE is a 1.8V CMOS logic input. During normal operation, SE is internally connected to GND. When SE is high (1.8V), the parallel input register is configured as a shift register, allowing the contents of the input register to be shifted out on the scan output (SO).
N13	SO	Scan Output. SO is a 1.8V CMOS logic output and active when scan enable (SE) is high.

12-Bit, 4.0Gsps High-Dynamic Performance Wideband DAC

Detailed Description

The MAX19693 is a high-performance, high-speed, 12-bit current-steering DAC with an integrated 50Ω differential output termination. The DAC is capable of operating with a clock rate (f_{CLK}) of up to 2.0GHz. Since the output is latched on both rising and falling clock edges, a 2.0GHz clock results in a DAC update rate (f_{DAC}) of 4.0Gsps.

The converter consists of an edge-triggered 4:1 input data multiplexer followed by a current-steering circuit. This circuit is capable of generating differential full-scale currents from 8mA to 20mA. Internal 25Ω resistors on each output, in combination with an external termination, convert the differential current into a voltage. The internal resistors are terminated to the 3.3V analog supply ($AV_{DD3.3}$). The internal termination resistors can be calibrated to an external 510Ω precision resistor. A calibration cycle can be run every time the converter is powered up, or at any other time as long as the clock is operating. An integrated 1.2V bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale range.

Reference Input/Output

The MAX19693 supports operation with the on-chip 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source, and as the output if the DAC is operating with the internal reference. For stable operation with the internal reference, decouple REFIO to DACREF with a 1µF capacitor. Since REFIO has a 10kΩ series resistance, buffer REFIO with an external amplifier to drive external loads.

The MAX19693's reference circuit (Figure 1) employs a control amplifier designed to regulate the full-scale current (I_{OUT}) for the differential current outputs of the DAC. The output current can be calculated as follows:

$$I_{OUT} = 32 \times I_{REF} \times 4095/4096$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$) and I_{OUT} is the full-scale output current of the DAC. Located between FSADJ and DACREF, R_{SET} is typically set to 1.92kΩ, resulting in a full-scale current of 20mA and a maximum of -2.6dBm output power for a CW signal if the internal reference is used. Generally, the dynamic performance of the DAC improves with increasing full-scale current.

REFIO can be driven by an externally applied reference voltage for gain adjustment/level-control purposes. The bandwidth of the control amplifier in Figure 1 is typically less than 100kHz, and the input resistance at REFIO is 10kΩ.

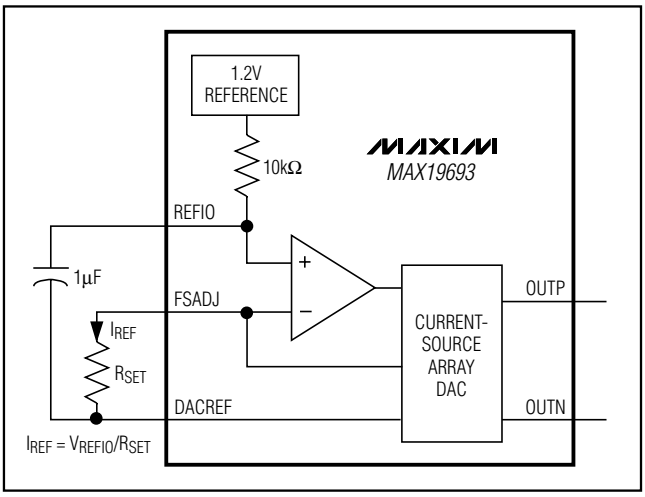


Figure 1. Reference Architecture, Internal Reference Configuration

Analog Outputs

The MAX19693 is a differential current-steering DAC with built-in, self-calibrated output-termination resistors to optimize performance. The outputs are terminated to $AV_{DD3.3}$, and are calibrated to provide a 50Ω differential output resistance. In addition to the signal current, a constant 10mA current sink is connected to each DAC output. Typically, the outputs are used with a 50Ω balun transformer. If the transformer is center-tapped, it is recommended that the center tap be connected to $AV_{DD3.3}$. If the transformer is not center-tapped, inductors can be used to pull up the outputs, as shown in Figure 13. Figure 2 shows an equivalent circuit of the internal output structure of the MAX19693.

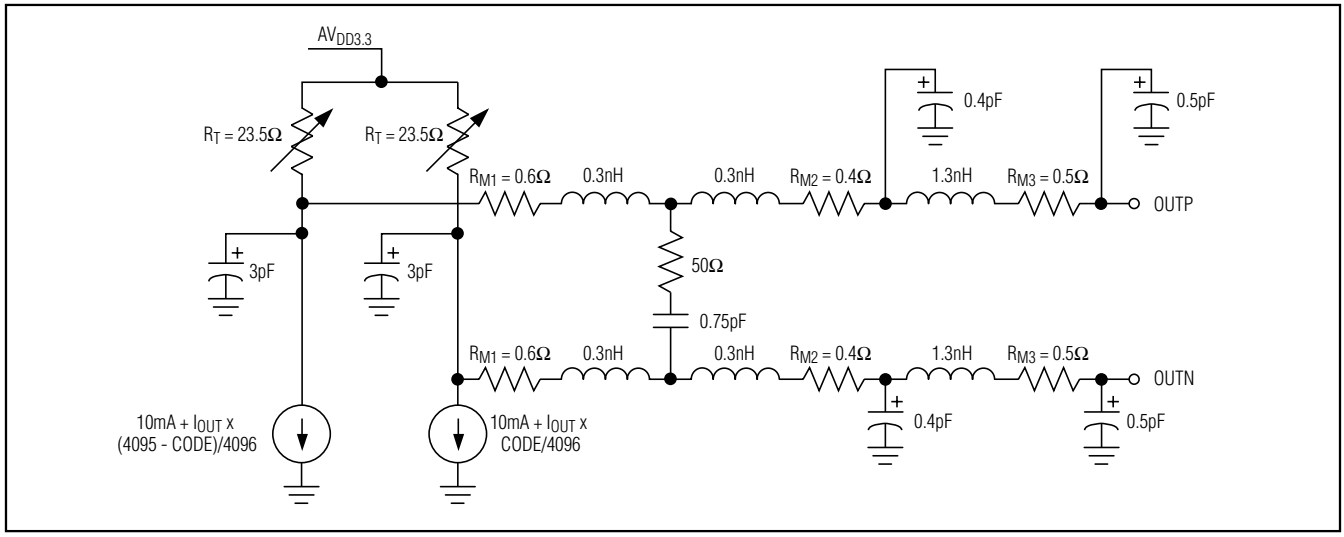


Figure 2. Equivalent Output Circuit

The output termination resistors (R_T) are calibrated to 23.5Ω. R_M (R_{M1} + R_{M2} + R_{M3}) is the resistance of the DAC output traces and bond wires, and is not calibrated. The output resistance is equal to $2R_T$ + $2R_M$, and is nominally 50Ω. The MAX19693 is normally used with an external differential 50Ω load (R_L). For this case, the peak differential output voltage is calculated as follows:

$$V_{OUT} = I_{OUT} \times R_L \, R_T/(R_L + 2\,R_M + 2\,R_T)$$

where I_{OUT} is the full-scale current, typically set to 20mA. With R_L = 50Ω, R_T = 23.5Ω, and R_M = 1.5Ω, V_{OUT} is 0.235V. This corresponds to an output power of -2.6dBm. As shown in Figure 2, the output circuit has some resistive, capacitive, and inductive elements. These elements limit the output bandwidth to 1.5GHz with a resistive differential load of 50Ω.

Output Resistor Calibration

The integrated termination resistor (R_T) must be calibrated to have an accurately known DAC output resistance and voltage. The termination resistors are calibrated to the external reference resistor (R_{REFRES}) connected between REFRES and $AV_{DD3.3}$. R_{REFRES} is nominally 500Ω. A plot showing the typical relation between the DAC output resistance and R_{REFRES} is shown in Figure 3.

The calibration cycle is initiated with a rising edge on CAL. While the clock is running, CAL must be asserted and held high after the supply voltages and the reference voltage have reached steady state. Input data should not be switching while the calibration is running. The duration of the calibration cycle is shorter than 65,536 DAC clock cycles (less than 32.8µs if the converter is operated with a 2GHz clock rate). CAL must be held high for the output resistors to remain calibrated. If the clock is stopped, or if power is cycled, a new calibration cycle must run.

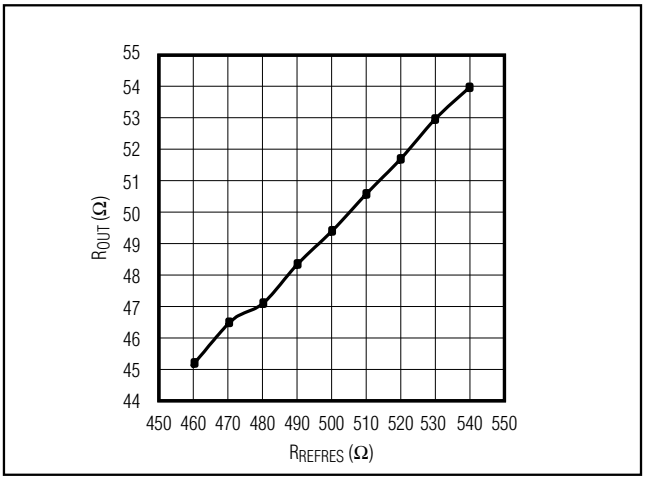


Figure 3. Output Resistance vs. REFRES Resistor

12-Bit, 4.0Gsps High-Dynamic Performance Wideband DAC

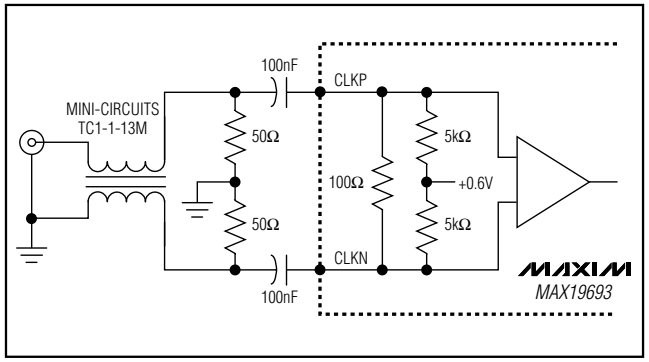


Figure 4. Typical Clock Application Circuit

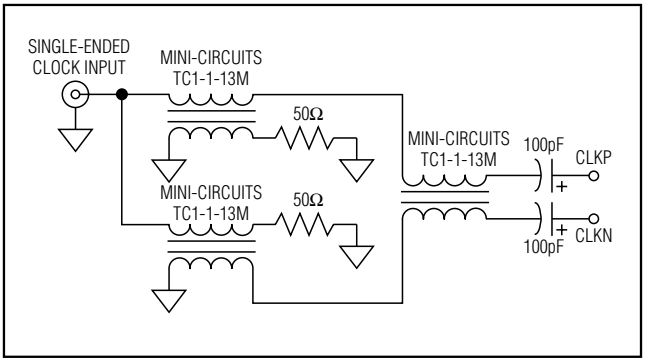


Figure 5. Clock Application Circuit with Improved Symmetry

Clock Inputs

The MAX19693 features a flexible differential clock input (CLKP, CLKN) operating from a separate supply (AV_{CLK}) to achieve the best possible jitter performance. The two clock inputs can be driven from a single-ended or a differential clock source. A sine wave or a square wave can be used. For single-ended operation, drive CLKP with a logic source, and bypass CLKN to GND with a 0.1µF capacitor.

Driving the clocks differentially is recommended for optimum jitter performance. Choose a clock amplitude that is as large as possible (without the clock voltage at the CLKN and CLKP going more than 300mV below ground or above the AV_{CLK} supply voltage) to minimize jitter. For an AC-coupled, differential sine-wave clock, using the input circuit of Figure 4 or 5, clock power should not be higher than 15dBm.

The MAX19693 can be used with a sinusoidal clock amplitude as low as $0.6V_{P-P}$ (0dBm) below 3Gsps. For higher update rates, a clock amplitude between 10dBm and 12dBm is recommended for optimum noise performance.

The CLKP and CLKN are internally biased to 0.6V with resistors. This allows AC-coupling of clock sources directly to the device without external resistors to define the DC level.

An internal 100Ω termination resistor connects CLKP to CLKN. Add an external 100Ω termination resistor when using a 50Ω clock source. See Figure 4 for a convenient way to apply a differential signal created from a single-ended source and a wideband transformer.

The clock circuit in Figure 4 provides amplitude asymmetry at update rates above 3Gsps due to transformer loss, which may cause the clock duty cycle to deviate from 50% for clock rates close to 2GHz. This may cause the image spur at $f_{DAC}/2 - f_{OUT}$ to increase by several decibels (dB). Figure 5 shows a clock interface circuit with improved symmetry using three balun transformers. This clock interface circuit provides symmetric and balanced clock signals for frequencies up to the maximum update rate of the MAX19693. An equivalent circuit model for the clock inputs is shown in Figure 6.

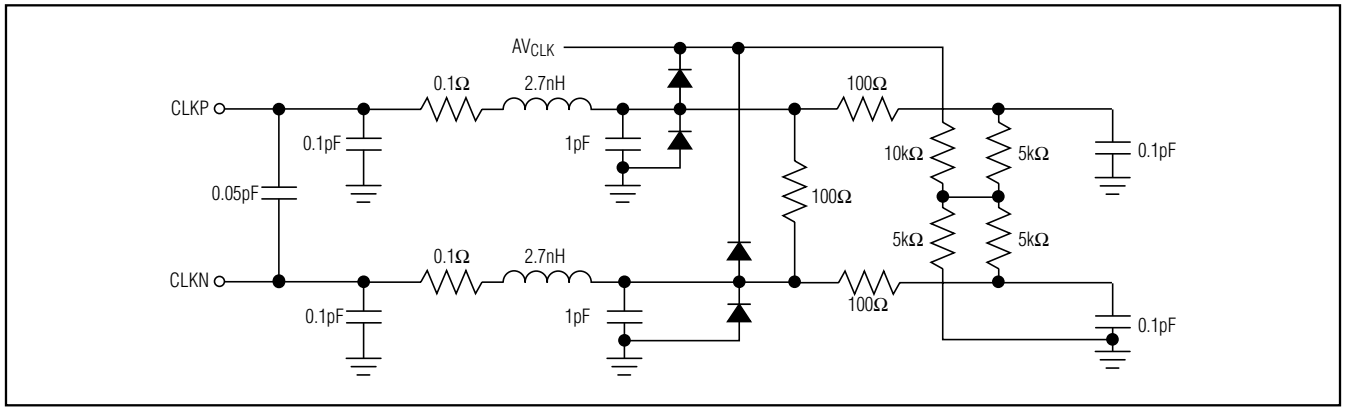


Figure 6. Clock Input Equivalent Circuit

Clock Duty Cycle

The DAC output is updated on both the rising and falling clock edges. Use a clock with a duty cycle as close to 50% as possible. When using an AC-coupled sine-wave clock, the clock duty cycle is automatically close to 50%.

Deviation from a balanced duty cycle contributes to an image in the output spectrum. The magnitude of the image is dependent on the deviation from an ideal 50% duty cycle. This artifact occurs at the following frequency:

$$f_{IMAGE} = \frac{f_{DAC}}{2} \pm f_{OUT}$$

Another artifact resulting from updating the DAC output on both edges is the generation of a spur at the clock frequency, or 1/2 the DAC update rate. Note that this spur is not related to the duty cycle:

$$f_{SPUR} = \frac{f_{DAC}}{2}$$

$f_{DAC}/2$ Modulation (MOD)

The MAX19693 MOD input (B4 node) provides $f_{DAC}/2$ (or f_{CLK}) modulation as shown in Figure 7 when it is set to logic 1. MOD is a 3.3V CMOS logic input pin. Setting MOD to logic-high inverts data on ports B and D inside the MAX19693.

Using the MOD function improves IMD when synthesizing some high-frequency signals. To use the MOD function, set MOD to logic-high and invert data on ports B and D.

Data Inputs

Data inputs (DAP[11:0], DAN[11:0], DBP[11:0], DBN[11:0], DCP[11:0], DCN[11:0], DDP[11:0], DDN[11:0]) are LVDS receivers followed by edge-triggered flip-flops. Four 12-bit buses accept data in offset binary format. The LVDS inputs feature on-chip termination with differential 100Ω resistors. A 1.25V common-mode level with a standard LVDS differential swing can be applied to these inputs. See Figure 8 for an equivalent circuit of the LVDS inputs.

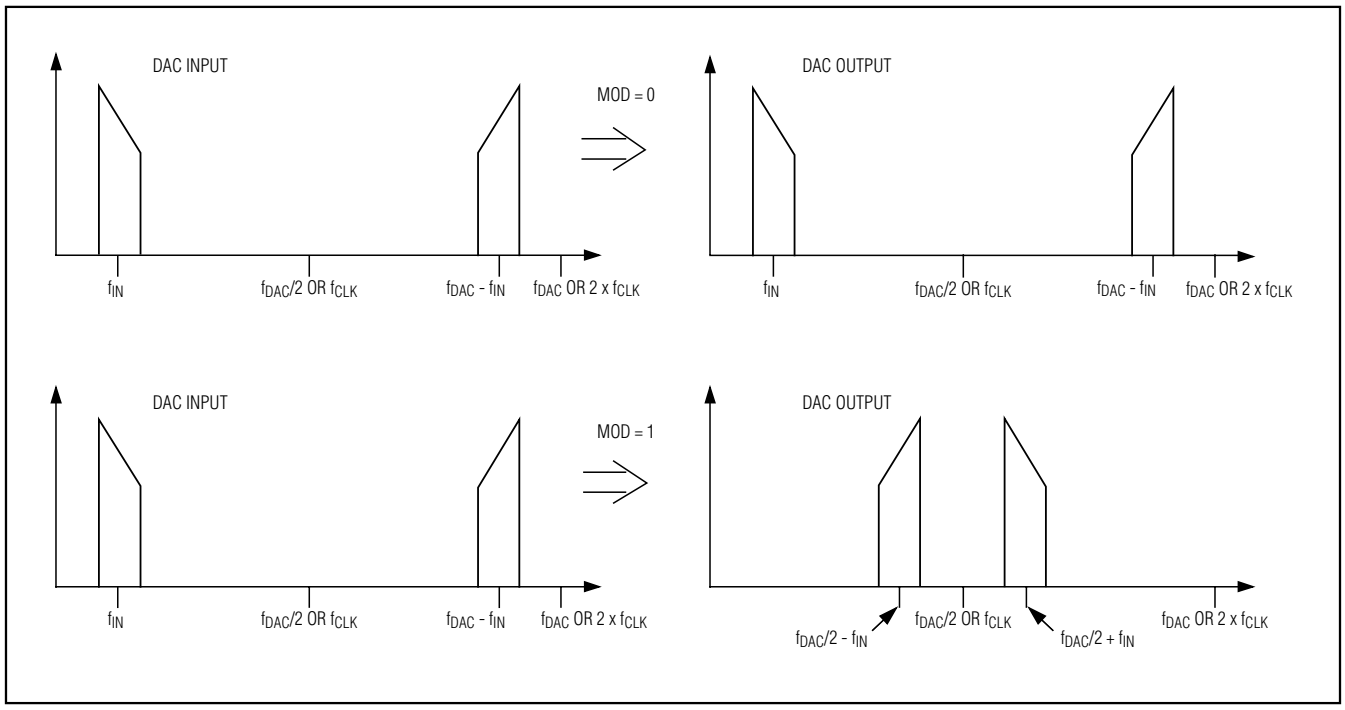


Figure 7. $f_{DAC}/2$ Modulation Using the MOD Input

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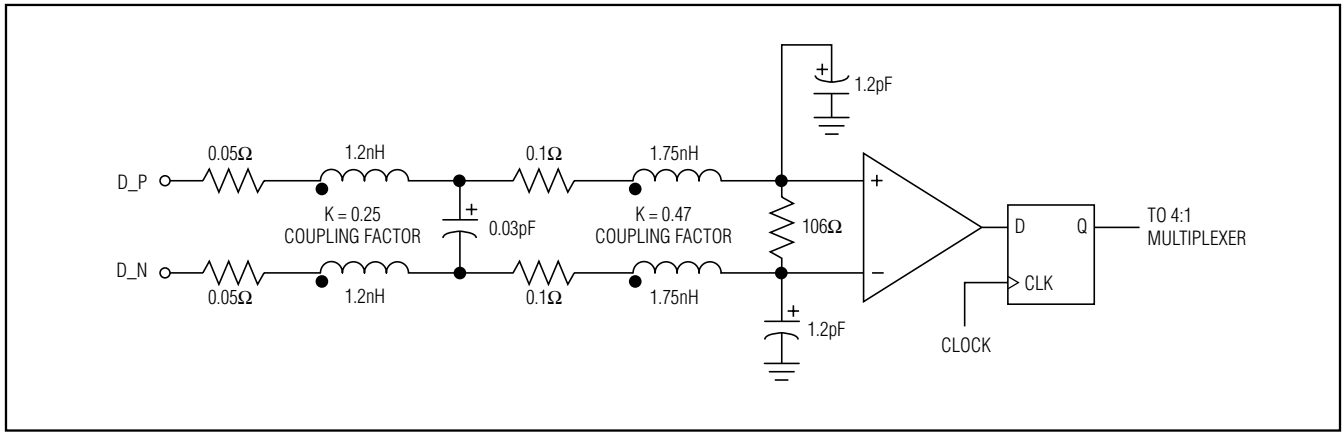

Figure 8. LVDS Input Equivalent Circuit

Data Timing Relationships

The timing of the LVDS inputs is defined with respect to the LVDS output DATACLK (DATACLKP, DATACLKN). The LVDS data inputs are latched at 1/2 the input clock frequency. The DATACLK output frequency is divided by another factor of 4 (CLKDIV = 0) or by 2 (CLKDIV = 1).

Define the 0° point of DATACLK as the rising edge.

For the case of CLKDIV = 1, data is latched at 0° and 180° of DATACLK, and setup and hold times must be satisfied for both these points in time.

For the case of CLKDIV = 0, data is latched at 0°, 90°, 180°, and 270° of DATACLK. Setup and hold times must be satisfied for all four of these points in time.

The DELAY input can skew DATACLK by 1/2 of the input data period, as shown in Figure 9. This eases interfacing to FPGAs where the clock to Q delay of the LVDS outputs is not adjustable. The clock driving the data input register is not delayed with DELAY. The setup and hold times are always referred to the case when DELAY = 0. Data-timing relationships are shown in Figure 10.

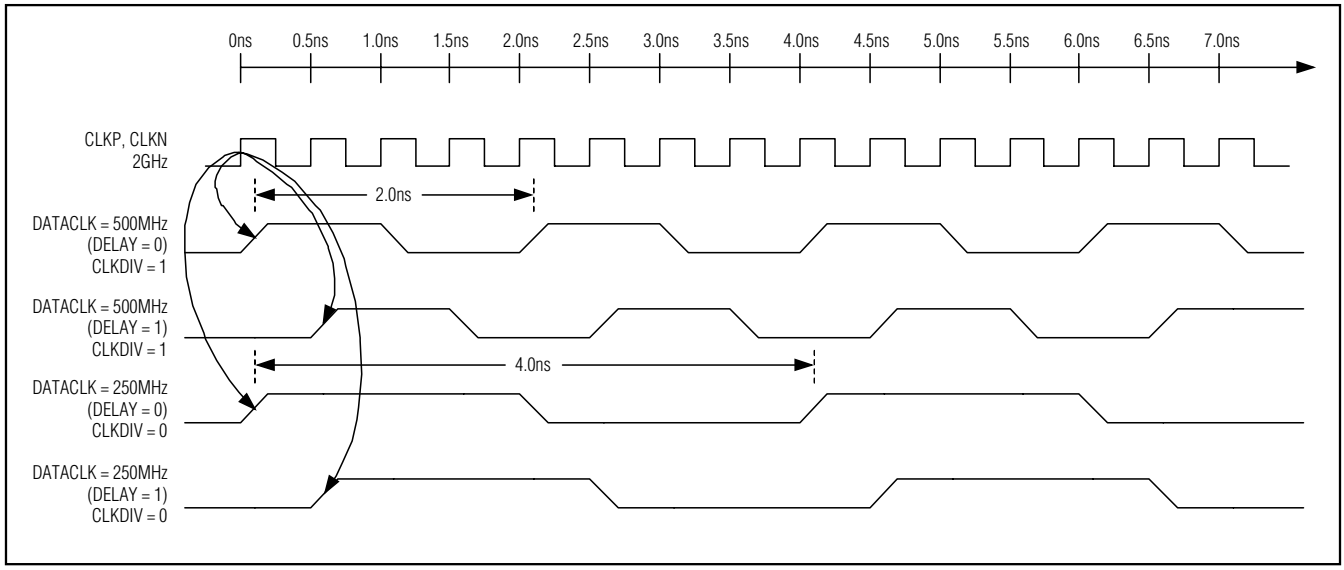

Figure 9. Effect of DELAY Input on Data Clock Output

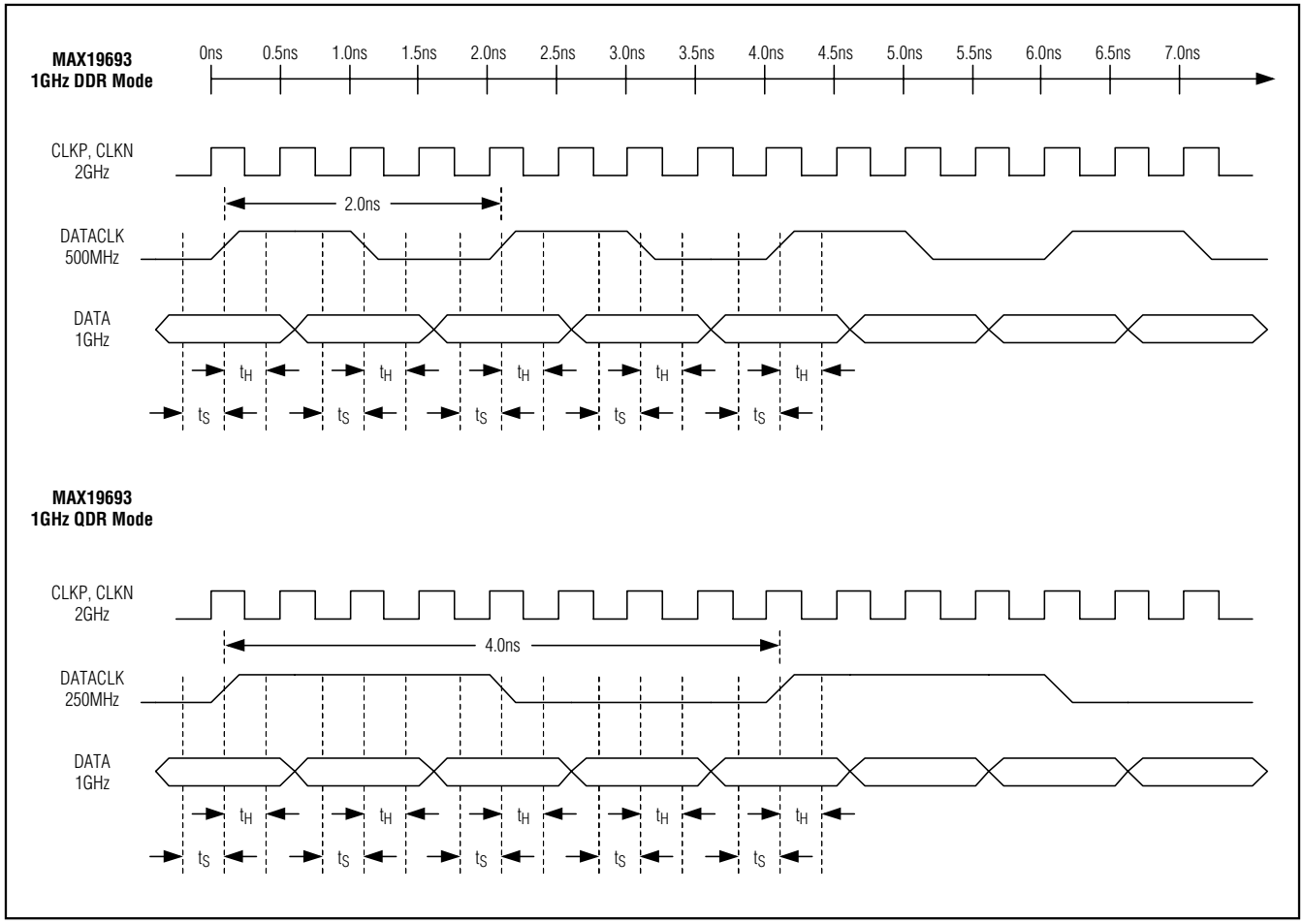

Figure 10. Setup (t_S) and Hold Time (t_H) for Data Input Interface

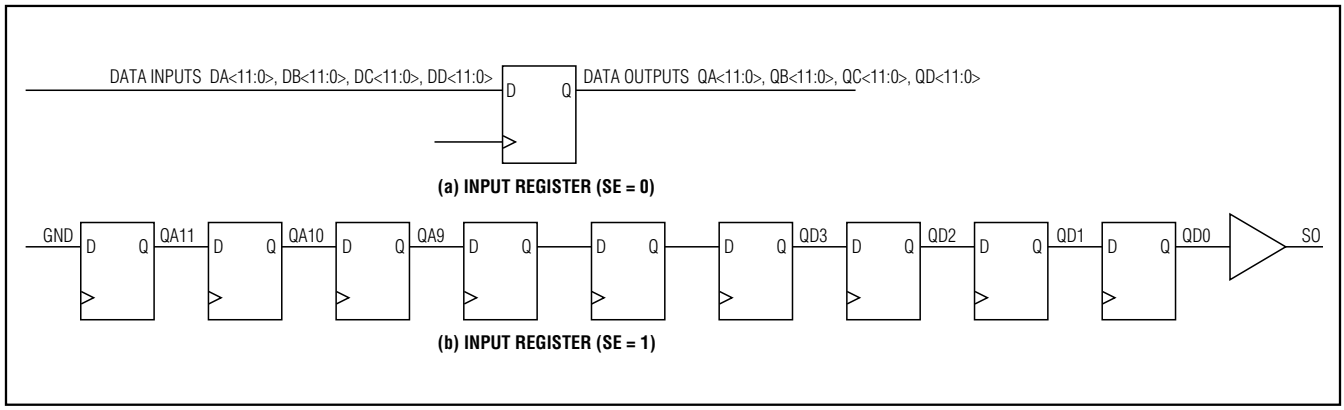

Figure 11. Input Register Flip Flops in Normal Operation (a) and Scan Mode (b)

12-Bit, 4.0Gsps High-Dynamic Performance Wideband DAC

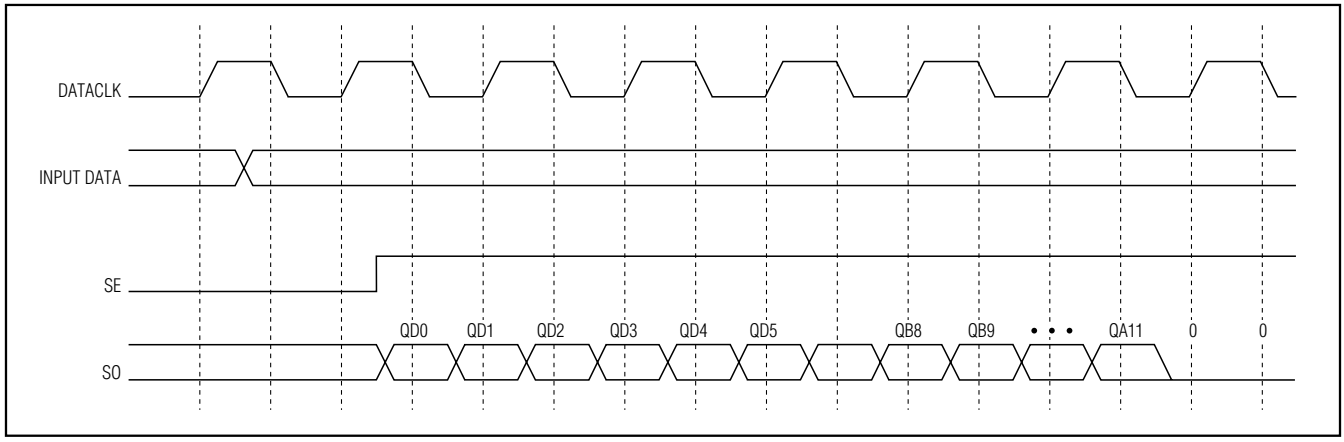

Figure 12. Timing Diagram, Scan Operation

Input Register Scan

The outputs of the data input register on the MAX19693 can be monitored on the SO (scan output) pin to allow verification of the connectivity of the data input pins. This function is enabled using the SE (scan enable) pin. When SE is logic 0 (0V), the input register operates normally, and SO is in a high-impedance state. When SE is logic 1 (1.8V), the input register flip-flops are reconfigured to be a 48-bit shift register, connected to the SO output as shown in Figure 11. Data is clocked out at the input register data rate.

A timing diagram for the operation is shown in Figure 12. Known input data is applied to the DAC data inputs on the first DATACLK pulse, and the input register is loaded in a parallel fashion. Note that the input data needs one clock cycle to propagate before SE can be set to logic 1. When SE is set to logic 1, the input register is configured as a 48-bit long shift register, outputting at SO. The order of the bit output on SO is QD<0:11>, QC<0:11>, QB<0:11>, and QA<0:11>, followed by constant low until SE is set low, which brings SO into high- impedance mode again.

The scan interface is a 1.8V CMOS logic interface.

Applications Information

Differential Coupling Using RF Transformers

The differential voltage between OUTP and OUTN can be converted to a single-ended voltage using a transformer or a differential amplifier configuration. Using a differential transformer-coupled output (CW output power is limited to -2.6dBm) optimizes the dynamic performance. Use bias tees built from discrete inductors and capacitors (Figure 13) for optimal performance. Pull up the DAC outputs to 3.3V. Not pulling up the outputs to 3.3V may result in some degradation of dynamic performance if the full-scale current is set to 20mA. A recommended output circuit is shown in Figure 13. To achieve the maximum bandwidth, minimize the inductance in the ground lead on the secondary side of the transformer. Use a very short trace and multiple vias for the connection to the ground plane. Alternatively, the DAC output can be AC-coupled into a wideband differential amplifier.

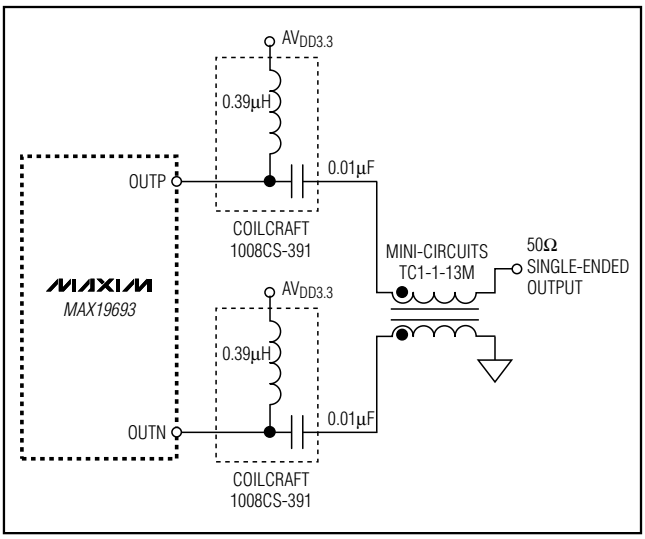

Figure 13. Differential to Single-Ended Conversion Circuit for MAX19693 Analog Output

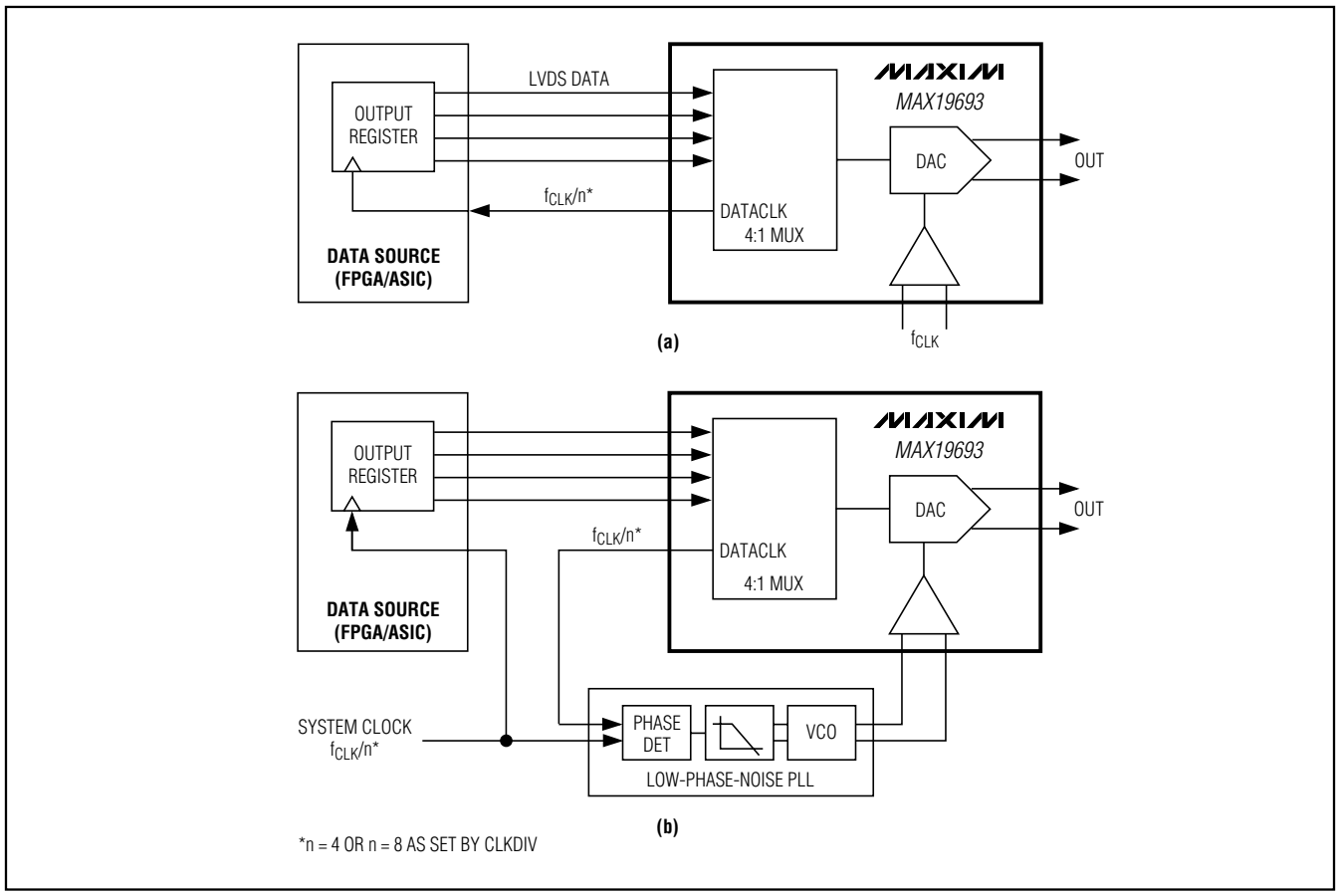

Figure 14. Data Source to DAC Interfacing

Data Synchronization

The DAC clock runs at twice the data rate of the data interface to the MAX19693. An LVDS level data clock output (DATACLKP, DATACLKN) helps to synchronize the data source and the DAC. The output data clock frequency can be set to 1/2 the input data rate or 1/4 the input data rate. When the DAC is operating at full speed, this allows the data clock to be interfaced directly to FPGAs without using an external clock divider. For example, if the DAC is updating at 4Gsps, the input data rate is 1Gwps. If the DAC is interfaced to an FPGA, the data clock can operate at 1/4 the data input rate; hence the data output clock frequency would be 250MHz. If the system clock is operating at the DAC clock rate, the scheme in Figure 14(a) can be used. In this case, the system is clocked using the data clock output from the DAC. The delays of the data and the clock depend upon line lengths and loading. Hence, clock deskewing using a phase-locked loop or delay-locked loop may be necessary to make this system work properly at high frequencies. When CLKDIV = 0, the data clock output can be phase-shifted by 45° using DELAY. When CLKDIV = 1, the data clock output can be phase-shifted by 90° using DELAY.

An alternative solution is shown in Figure 14(b). In this case, the system clock distribution is running at the data clock rate. A low-jitter, low-phase-noise phase-locked loop is used to generate the high-speed DAC clock. Using the data clock for feedback into the PLL ensures synchronization between data and clock. If more than one MAX19693 is used in a system, and the relative phases need to be defined, the divided data clock of each DAC should be phase locked to a system clock running at data rate/4 or data rate/2, equal to the DAC clock rate divided by 8 or 4, respectively.

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Grounding, Bypassing, Power-Supply, and Board-Layout Considerations

Grounding and power-supply decoupling can strongly influence the performance of the MAX19693. Unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections, affecting dynamic performance. Proper grounding and power-supply-decoupling guidelines for high-speed, high-frequency applications should be closely followed. This reduces EMI and internal crosstalk that can significantly affect the dynamic performance of the MAX19693.

Use of a multilayer PCB with separate ground and power-supply planes is required. It is recommended that the analog output and the clock input are run as controlled-impedance microstrip lines on the top layer of the board, directly above a ground plane, and that no vias are used for the clock input (CLKP, CLKN) and the analog output (OUTP, OUTN) signals. Depending on the length of the traces, and the operating condition, a low-loss dielectric material (such as ROGERS RO4003) as the top layer dielectric may be advisable. The data clock (DATACLKP, DATACLKN) must be routed so coupling into the clock input and the DAC output is minimized.

Digital input signals should be run as controlled-impedance strip lines between ground planes. Digital signals should be kept as far away from sensitive analog inputs, reference input sense lines, common-mode inputs, and clock inputs as practical. It is particularly important to minimize coupling between digital signals and the clock, to optimize dynamic performance for high output frequencies. A symmetric design of the clock input and analog output lines is critical to minimize distortion and optimize the DAC's dynamic performance.

Digital signal paths should be kept short and run lengths matched to avoid data-delay mismatch.

The MAX19693 supports three separate power-supply inputs for analog 3.3V ($AV_{DD3.3}$), switching ($V_{DD1.8}$), and clock (AV_{CLK}) circuits. Each $AV_{DD3.3}$, $V_{DD1.8}$, and AV_{CLK} input should at least be decoupled with a separate 0.047µF capacitor as close as possible to the input, and their opposite ends with the shortest possible connection to the corresponding ground plane to minimize loop inductance. All three power-supply voltages should also be decoupled at the point they enter the PCB with tantalum or electrolytic capacitors.

Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

The power-supply inputs ($V_{DD1.8}$ and AV_{CLK}) of the MAX19693 allow a 1.8V ±0.1V supply voltage range. The analog power-supply input ($AV_{DD3.3}$) allows a 3.3V ±0.2V supply voltage range. To optimize the dynamic performance of the MAX19693 over temperature at the highest update rates, it is important that the difference between $V_{DD1.8}$ and $AV_{DD3.3}$ is at least 1.4V. If $V_{DD1.8}$ is 1.9V and $AV_{DD3.3}$ is 3.1V, dynamic performance at these update rates degrades at higher temperatures.

The MAX19693 is packaged in a 169 CSBGA with 0.8mm ball pitch **(package code: X16911-1)**, providing design flexibility, thermal efficiency, and a small footprint for the DAC.

Static Performance Parameter Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from either a best straight-line fit (closest approximation to the actual transfer curve) or end-point fit (a line drawn between the end points of the transfer function, once offset and gain errors have been nullified). For a DAC, the deviations are measured at every individual step. The MAX19693 INL is specified using the end-point method.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification greater than -1 LSB guarantees a monotonic transfer function.

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a differential output DAC, the offset point is the average value at the output for the two mid-scale digital input codes with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles to its new output value to within the specified accuracy.

Noise Spectral Density

The DAC output noise is the sum of the quantization noise and other noise sources. Noise spectral density is the noise power in a 1Hz bandwidth.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of the largest distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

Two-/Four-Tone Intermodulation Distortion (IMD)

The two-/four-tone IMD is the ratio, expressed in dBc or dBFS, of the worst 3rd-order or higher IMD products to any output tone.

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Pin Configuration

TOP VIEW

MAXIM

MAX19693

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	REFIO A1	FSADJ A2	DACREF A3	$AV_{DD3.3}$ A4	$AV_{DD3.3}$ A5	OUTP A6	$AV_{DD3.3}$ A7	OUTN A8	$AV_{DD3.3}$ A9	$V_{DD1.8}$ A10	GND A11	AV_{CLK} A12	GND A13
B	CREF B1	REFRES B2	N.C. B3	MOD B4	GND B5	GND B6	GND B7	GND B8	GND B9	$V_{DD1.8}$ B10	GND B11	AV_{CLK} B12	CLKN B13
C	CAL C1	$V_{DD1.8}$ C2	$V_{DD1.8}$ C3	GND C4	GND C5	GND C6	GND C7	GND C8	GND C9	$V_{DD1.8}$ C10	GND C11	AV_{CLK} C12	CLKP C13
D	GND D1	GND D2	GND D3	GND D4	GND D5	GND D6	GND D7	GND D8	GND D9	GND D10	GND D11	AV_{CLK} D12	GND D13
E	$V_{DD1.8}$ E1	$V_{DD1.8}$ E2	$V_{DD1.8}$ E3	$V_{DD1.8}$ E4	GND E5	GND E6	GND E7	GND E8	GND E9	$V_{DD1.8}$ E10	$V_{DD1.8}$ E11	$V_{DD1.8}$ E12	$V_{DD1.8}$ E13
F	DAP7 F1	DAP6 F2	DAP8 F3	DAP9 F4	DAP10 F5	DAP11 F6	DDN11 F7	DDN0 F8	DDN1 F9	DDN2 F10	DDN3 F11	DDN4 F12	$V_{DD1.8}$ F13
G	DAN7 G1	DAN6 G2	DAN8 G3	DAN9 G4	DAN10 G5	DAN11 G6	DDP11 G7	DDP0 G8	DDP1 G9	DDP2 G10	DDP3 G11	DDP4 G12	GND G13
H	DAP0 H1	DAP1 H2	DAP2 H3	DAP3 H4	DAP4 H5	DAP5 H6	DDN10 H7	DDN5 H8	DDN6 H9	DDN7 H10	DDN8 H11	DDN9 H12	DATACLKN H13
J	DAN0 J1	DAN1 J2	DAN2 J3	DAN3 J4	DAN4 J5	DAN5 J6	DDP10 J7	DDP5 J8	DDP6 J9	DDP7 J10	DDP8 J11	DDP9 J12	DATACLKP J13
K	DBP11 K1	DBP10 K2	DBP9 K3	DBP8 K4	DBP3 K5	DBP1 K6	DCP10 K7	DCP8 K8	DCP3 K9	DCP2 K10	DCP1 K11	DCN0 K12	DELAY K13
L	DBN11 L1	DBN10 L2	DBN9 L3	DBN8 L4	DBN3 L5	DBN1 L6	DCN10 L7	DCN8 L8	DCN3 L9	DCN2 L10	DCN1 L11	DCP0 L12	CLKDIV L13
M	DBP7 M1	DBP6 M2	DBP5 M3	DBP4 M4	DBP2 M5	DBP0 M6	DCP11 M7	DCP9 M8	DCP7 M9	DCP6 M10	DCP5 M11	DCP4 M12	SE M13
N	DBN7 N1	DBN6 N2	DBN5 N3	DBN4 N4	DBN2 N5	DBN0 N6	DCN11 N7	DCN9 N8	DCN7 N9	DCN6 N10	DCN5 N11	DCN4 N12	SO N13

The MAX19693 is packaged in a compact 11mm x 11mm, 169 CSBGA (package code X16911-1 (leaded) or X16911+1 (lead-free)). Ball pitch is 0.8mm.

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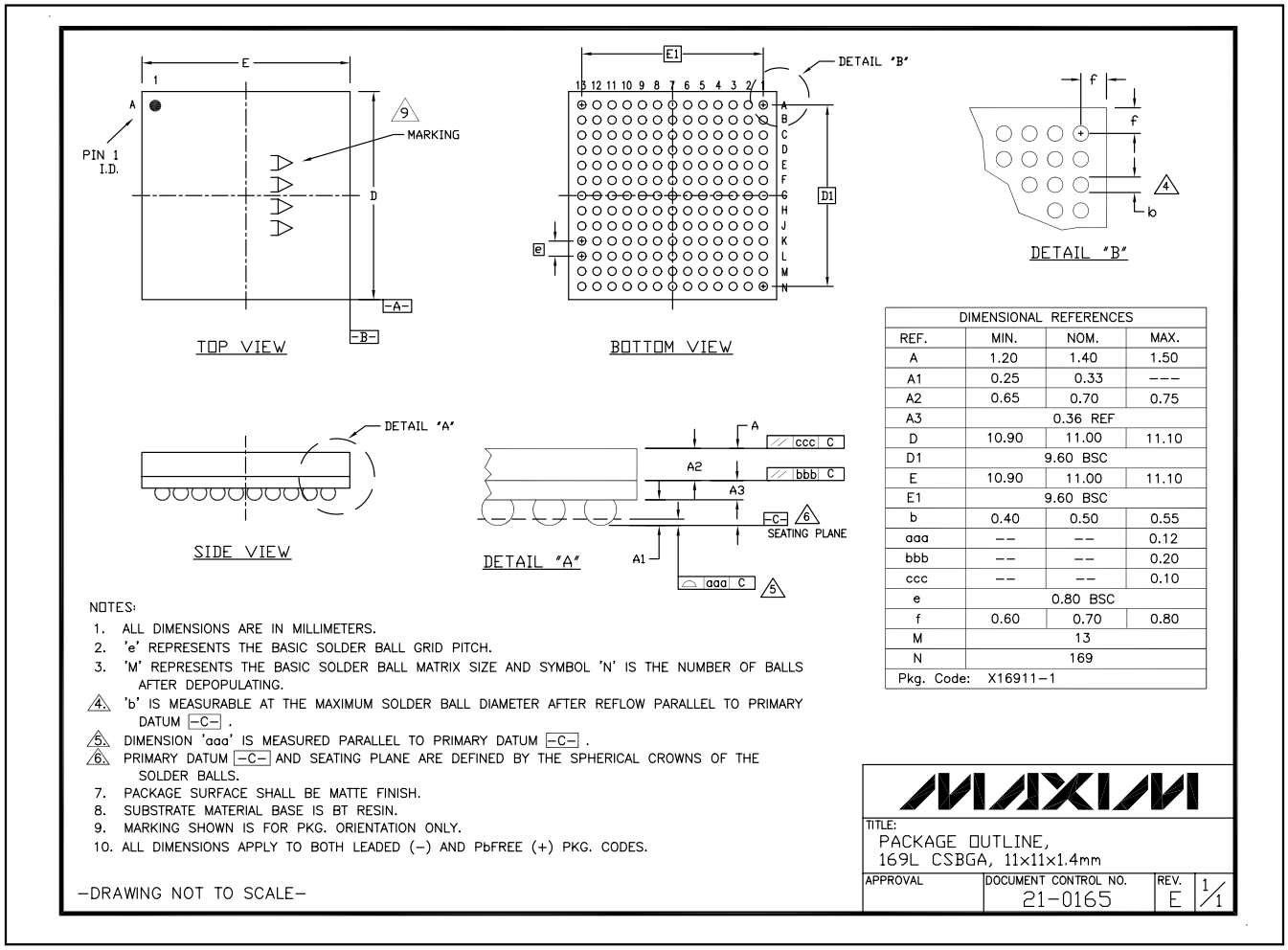
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
169 CSBGA	X16911+1	21-0165	90-0186



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.20	1.40	1.50
A1	0.25	0.33	---
A2	0.65	0.70	0.75
A3		0.36 REF	
D	10.90	11.00	11.10
D1		9.60 BSC	
E	10.90	11.00	11.10
E1		9.60 BSC	
b	0.40	0.50	0.55
aaa	--	--	0.12
bbb	--	--	0.20
ccc	--	--	0.10
e		0.80 BSC	
f	0.60	0.70	0.80
M		13	
N		169	
Pkg. Code:	X16911-1		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE AND SYMBOL 'N' IS THE NUMBER OF BALLS AFTER DEPOPULATING.
4. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW PARALLEL TO PRIMARY DATUM -C- .
5. DIMENSION 'aaa' IS MEASURED PARALLEL TO PRIMARY DATUM -C- .
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE MATTE FINISH.
8. SUBSTRATE MATERIAL BASE IS BT RESIN.
9. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
10. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 169L CSBGA, 11x11x1.4mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0165	E	1/1

12-Bit, 4.0Gsps High-Dynamic Performance Wideband DAC

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release	—
1	8/10	Add lead-free package, update *Absolute Maximum Ratings*	1, 2, 22, 23